The Design of Low-Power MIPI-Standard Serial-Link Transceiver for consumer Electronics Graduation Project

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List of Symbols and Abbreviations

Please insert here any symbols and abbreviations that you commonly use in your report.

Example:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmitter</td>
</tr>
<tr>
<td>Rx</td>
<td>Receiver</td>
</tr>
<tr>
<td>Vds</td>
<td>Voltage from drain to source</td>
</tr>
<tr>
<td>Vgs</td>
<td>Voltage from gate to source</td>
</tr>
<tr>
<td>Gm</td>
<td>Gain of the MOSFET</td>
</tr>
<tr>
<td>Av</td>
<td>Gain of the whole circuit</td>
</tr>
<tr>
<td>CDR</td>
<td>Clock and Data Recovery</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>PFD</td>
<td>Phase/Frequency Detector</td>
</tr>
<tr>
<td>BGR</td>
<td>Band gap reference</td>
</tr>
<tr>
<td>TC</td>
<td>Temperature Coefficient</td>
</tr>
<tr>
<td>K</td>
<td>Boltzmann’s Constant</td>
</tr>
<tr>
<td>T</td>
<td>Temperature</td>
</tr>
<tr>
<td>Q</td>
<td>Charge of an electron</td>
</tr>
<tr>
<td>Gnd</td>
<td>Ground</td>
</tr>
<tr>
<td>res.</td>
<td>Resistance</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable gain amplifier</td>
</tr>
<tr>
<td>SLVS</td>
<td>Scalable low voltage signaling</td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump</td>
</tr>
<tr>
<td>LF</td>
<td>Loop Filter</td>
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<tr>
<td>PI</td>
<td>Phase Interpolator</td>
</tr>
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</table>
Acknowledgments

Our project has been a rich and rewarding experience, and we have many people to thank.

First and foremost, we’d like to thank our advisor,

Dr. Sameh Assem Ibrahim, He was more fair, understanding and patient than we could have ever hoped for. He challenged our intellect in every meeting, and encouraged us to think deeply and creatively. He will always be a role model for us.

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Eng. Ahmed Fakhry and MIPEX Company were our sponsors we are thankful for them for supporting us.

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Concerning VCO, After thanking ALLAH for supporting me in my first encounter with life (personally) throughout a whole year and over-passing it -technically-through a few days, My special thanks to my helpful friend, Eng. Ahmed Mohamed Ahmed, for having too much time discussing with me many ideas and concepts, although what he has been through. I wish you success in your life and having a full career where others can benefit from your knowledge. Also, I’d like to thank Eng. Ahmed Farag for my many and simple questions where he always guided me to how to self learn in addition to smart hints. And I’ve learned many new helpful methods through discussing problems with our teachers and Eng. Alaa Fathy Rezq. My heartly greeting to them all.
Introduction

Background

For transmitting or receiving data between integrated circuits and printed-circuit boards (PCBs), an electrical link is required. In its simplest form, an electrical link consists of a transmitter (TX), a communication channel and a receiver (RX). An electrical communication channel can be as simple as a PCB copper trace, or twisted-pair and coaxial cables, or as complex as a backplane consisting of multiple boards, connectors and traces. Advancement in integrated-circuits technology has been the driving force in the development of high-speed electrical links. Traditionally, high-speed links have used a single link whose speed was limited by the on-chip bandwidth. However, as shown in Fig. 1.1, in the 1990s, semiconductor technologies have improved and on-chip speeds increased as compared to off-chip bandwidth. This dictated the use of parallel links. In parallel links, both data and clock are sent from the TX to the RX.

![Diagram showing the evolution of high-speed I/O architecture](image)

Figure 1.1.1 High-speed I/O architecture evolution as a function of data rate and time
In the early 2000s, when data rates increased even more, parallel links suffered from multiplexing overhead, signal skews, difficulties in clock and data synchronization, crosstalk and interference. This resulted in a shift towards high-speed serial links aided by the increased on-chip bandwidth. In serial links, the clock is recovered rather than sent, removing the skew problem.

Recently, manufacturers of integrated circuits and networking equipment are seeking data rates in the range of 10 Gb/s and beyond. However at such high data-rates power consumption becomes prohibitively large that they cannot be used in portable/mobile consumer electronics because of their impact on battery life. The (Mobile Industry Processor Interface) MIPI alliance is a non-profit corporation aiming to benefit the entire mobile industry by establishing standards for hardware and software interfaces in mobile devices. As shown in Fig. 2, recent research shows that 6.2 billion MIPI-powered ICs will be in production in 2015. It also shows that MIPI specifications will reach 100% penetration of smartphones in 2013 and 90% penetration of other phones by 2015.

The main focus of the MIPI standard is to reduce power consumption while maintaining high performance at such high speeds. The power saving at the
consumer-electronic end product has a better impact on the worldwide energy crisis. Saving just 1% of power consumption on each handheld product can cause a huge impact due to the billions of products sold annually.

Project Description

In this project we will focus on the MIPI new physical layer standard M-PHY aiming to build a transceiver conforming to the standard. Data signaling at 10 Gb/s with as low power consumption as possible is not a trivial task. The block diagram of the proposed transceiver is shown in Fig. 3.

![Figure 1.1.3 Block diagram of the proposed MIPI transceiver](image)

The transmitter consists of 16-1 multiplexer, followed by 10-Gb/s pre-driver and a 10-Gb/s scalable low-voltage signaling (SLVS) driver. The receiver on the other hand consists of a variable gain amplifier (VGA), followed by a receiver equalizer, a slicer and a demultiplexer. The receiver equalizer consists of a linear equalizer followed by a decision feedback equalizer (DFE) to compensate for all the channel impairments at 10-Gb/s speed. The main challenge of the project is to achieve the $10^{-10}$ BER required with the lowest power consumption. That is why techniques like scalable supply and bias currents, current re-use, small TX output swing and optimized RX
sensitivity, and pulse amplitude modulation will be evaluated and used when necessary to achieve the target power efficiency of 5 pJ/bit or lower.

**Project Outcomes**

On the course of the project the students are expected to reach the following milestones:

- Read the MIPI standard specifications and convert them to system and circuit specifications.
- Do behavioral system-level modeling and simulation of the transmitter, the receiver, and the whole link.
- Design and implement the circuits of the different building blocks of the transceiver.
- Perform circuit and system level simulations.
- Implement the layout of the transceiver and do post-layout simulations.
- Do measurements of the transceiver after fabrication.

**Project Impact**

As stated earlier, no 10-Gb/s MIPI transceivers are available in literature or in the market yet. Many companies are targeting to implement the first-to-market MIPI transceiver, including our industrial partner Mipex. Provided that all the milestones are achieved, this gives great opportunity for patenting, publications and/or productization.
Chapter 1: Transmitter

1.1 Serializer

1.1.1 Concept Review

Multiplexing is serializing parallel input data to a serial output data line.

Multiplexer is used in serial link to serialize different inputs and de-serialize it after the link to the receiver point as shown in Figure 1.1.1

Serializer consists of many multiplexers so to serialize the inputs into single line so to use the same serial link for many signals and different chips.

Serializer and de-serializer are from the main blocks in serial links as serial link is not made for 1 connection or 2 data source but it’s made for several data sources combining them by multiplexer to go through the serial link to the desired output.
1.1.2 Circuit Review

There is much architecture found for multiplexer but what is more popular and usage is the Tree architecture:

At which the multiplexers are placed to form a tree shape until it get the required output, as shown in Fig 1.1.2

Also there are different logics as follows:

i. CML Logic:

CML architectures using current mode logic which consume much power as shown in Fig 1.1.3 CML inverter Static power consumption due to continuous tail current M5. So CML Nearly independent depends on of the operation frequency.
ii. CMOS Logic:

The CMOS logic uses power only when charging and discharging so. It has No static power consumption. When CMOS inverter Fig 1.1.4 operating at steady state there is no direct path from $V_{dd}$ and ground, but the power consumption is product of operating frequency and charging and discharging energy per unit switching, so it Depend directly on the operation frequency, it has Poor immunity against ISI.

1.1.3 Multiplexing topologies

i. Conventional

A conventional multiplexer unit stage consists of: 2-F.Fs, latch & 2:1 Selector.as shown in Fig 1.1.5

ii. Latches

Latch is a circuit that has two stable states and can be used to store state information so it is simply a data storage element. Latches is level triggered there is positive latch and negative latch as shown in Fig 1.1.6

Figure 1.1.4 CMOS inverter

Figure 1.1.5 conventional 2:1 mux

Figure 1.1.6 positive and negative latch
CMOS latches consist of 2 types:

a. Static latch:
It relies on transferring the input data to node A at high clock and then inverted to the output, while the clock is low the instantaneous data is held on parasitic capacitance $C_p$ as shown in Fig 1.1.7

b. Dynamic latch:
Fig 1.1.8 a dynamic latch relies on transmitting the input at clock high while clock is low unlike the parasitic capacitance on static latch but here on dynamic there is a loop which is periodically refreshed to overcome the losses on $C_p$ that results on error.
iii. **Flip Flops:** 2 latches can be connected as Master & slave to operate as a flip flop as shown in Fig 1.1.9 a positive edge flip flop where after master latch the data passes through the negative edge and the other holds, and after slave latch the data passes through positive edge and the other highs to get an edge triggered flip flop.

1.1.4 **Settled topology**

i. **Clocked Inverters:**

After all that topologies what I used is what called clocked inverters or CMOS square as shown in Fig 1.1.10 It is an Inverter that control its output by a clock ,If clk = 1 Inverter pass the input to output , If clk = 0 , it holds the data as a latch (high impedance ). By using that topology we can implement a 2:1 mux as shown in Fig 1.1.11 using 3 clocked inverters we can perform the operation of retiming and selection at the same time and power consumption is decreased by reducing the number of Switching components ,It is Level triggered 2:1 mux but it suffers a Node Floating after the D1 clocked inverter due to the high impedance of the output at high clock time .That problem is solved using an interstate latch is inserted at the floating node point so to hold the input level of 2nd tri state inverter and make it fixed point as shown in fig 1.1.12. In Table 1.1.1 shown input data D0 & D1 and clk wave forms and how it is multiplexed at the output with a delay of half cycle. The 2:1 mux shown in Fig 1.1.12 is the building unit for the Serializer,
by putting that into tree architecture the full block architecture is as shown on Fig 1.1.13. It consists of 2:1 MUXes and pre logic block to adjust the polarity of the inputs as there is inverted output at each stage so it is solved by putting pre-logic circuit after inputs exactly so at low frequency so not to consume much power.

![Figure 1.1.12 2:1 mux –based on Clocked inverter](image1)

![Figure 1.1.11 2:1 mux –based on Clocked inverter with interstate latch for node floating risk.](image2)

<table>
<thead>
<tr>
<th>Input data</th>
<th><img src="image3" alt="Waveform of 2:1 MUX" /></th>
</tr>
</thead>
<tbody>
<tr>
<td>Clkb</td>
<td><img src="image4" alt="Waveform of Clkb" /></td>
</tr>
<tr>
<td>Output</td>
<td><img src="image5" alt="Waveform of Output" /></td>
</tr>
</tbody>
</table>

Table 1.1.1 Input, clock bar and output waveform of 2:1 mux
Figure 1.1.13 Serializer Block of 16 inputs and 1 output at 11.6 GB/s data rate
1.1.5 **Final design Achieved**

The final design achieved is what is shown in Fig 1.1.13 where there are 16 input pseudo random bit stream with rate 725 Mb/s is multiplexed to one serial line of rate 11.6 GB/s. the inputs are numbered by how they will get at the output 0 – 8 – 2 -10 and so on, there is even 8:1 serializer and odd 8:1 serializer and the final mux that multiplex at high frequency of 5.8GHz.

The sizing of clocked inverters is to achieve the threshold of inverters at 0.5 volt. At which the NMOS width is 200n and PMOS width is 400n and all have minimum length 60 n.

The clock of each 2:1 multiplexer is adjusted by a delay time to make the clock level at the center of the bit to achieve best eye diagram and the data is multiplexed correctly without glitches as shown on Fig 1.1.14.

The static power for the whole serializer is 56.4uW which achieve a very low consumption power for an 11.6 GB/s serializer.

![delayed clock](image-url)

*Figure 1.1.14 delayed clock to get the level of clock at the center of the bit*
1.1.6 **Results**

a. final waveform of output data at rate 11.6 Gb/s as shown in Fig 1.1.15.

![Final waveform of 11.6 GB/s output data rate](image)

Figure 1.1.15 Final waveform of 11.6 GB/s output data rate

b. Output Eye-diagram in Fig 1.1.16 for simulation time of 100n sec, and the width of eye is 84ps.

![Final output Eye-diagram of rate 11.6 GB/s](image)

Figure 1.1.16 Final output Eye-diagram of rate 11.6 GB/s
c. We have run 30 corners of different types SS, FF, SF and FS and the design is adjusted to be validated at all corners and as shown the output Eye-diagram at FF Fig 1.1.17 and SF at Fig 1.1.18.

Figure 1.1.17 Final output Eye diagram of rate 11.6 GB/s at FF corner

Figure 1.1.18 Final output Eye diagram of rate 11.6 GB/s at SF corner
1.1.7 **Specifications Required and Met**

The Specifications was to MUX the high data rate 11.6GB/s and It’s done with the lowest possible power consumption so I used CMOS logic for all the circuit and do not go for the CML to get the lowest possible power consumption so achieved a static power of 51 uW for the whole serializer .

1.1.8 **Layout**

The layout of the clocked inverter alone is done as follows in Fig 1.19 by putting three of clocked inverters and route in between them with appropriate routing we get the layout of 2:1 mux as shown in Fig 1.20 .

![Figure 1.1.20 Layout of clocked inverter](image1)

![Figure 1.1.19 : Layout of 2:1 MUX](image2)

1.1.9 **Conclusion**

We achieved a high speed serializer that serialize 16 input each of 725 MHz into one single line of 11.6 GB/s data rate at a very low power consumption using CMOS logic of clocked inverters to be used on high speed serial data links M-PHY and it passed all corners simulations .
1.2 Pre-driver

1.2.1 Concept Review

Pre-driver is used in the transmitter between the driver and the multiplexer to drive the large input capacitance of the driver without loading on the small output capacitance of the multiplexer not to distort the signal output from the driver.

Pre-driver is a buffering stage so it is simply implemented using a series of buffers or inverters to drive the large load capacitance.

Buffers are critical in their design when delay is to be concerned, that delay that results from the parasitic gate capacitances of the buffer should be controlled through a proper sizing of the inverters used in the buffer stage.

We face a problem when using buffers in the pre-driver stage which is the power consumption; they are called power hungry since they sink a large current "short circuit current" that occurs when both transistors of an inverter are on together leading to a direct path between the supply and the ground and that is responsible for draining a huge power from the supply and then we can solve this problem by limiting the use of inverter stages in the buffering series as possible as we can.

1.2.2 Circuit Review

Different topologies used in the buffer stages used in the pre-driver:

1) Low power CMOS buffers.
2) CML buffers.
3) Tapered buffers.
1) **Low power CMOS buffers**

**Circuit**

![Circuit Diagram](image)

This is used in applications with restrictions on rise and fall times. It also saves power by tri-stating the output before every o/p signal transition.

**Theory of operation**

1) **Wave shaper**

![Wave Shaper Diagram](image)

It splits the input signal into two paths. It is constructed very simply by means of asymmetrical inverters.
For the PMOS output transistor path, the waveform shaping inverter (s1p) is a weak pull-down inverter, causing the output rising edge of the following inverter (s2p) to be delayed.

Similarly for the Nmos output transistor path, the waveform shaping inverter (s1n) is a weak pull-up inverter, causing the output falling edge of the following inverter (s2n) to be delayed.

The result of these delays is that the output P-MOS transistor is always turned off before the output N-MOS transistor is turned on, and similarly the output N-MOS transistor is always turned off before the output P-MOS transistor is turned on.

**Output stage PMOS/NMOS drivers.**

![Output-stage PMOS/NMOS drivers](image)

Figure 1.2.3 Output PMOS/NMOS drivers

Consists of two inverter chains that individually buffer the two signals from the waveform shaper, giving them enough strength to drive the output transistors.

The length of the inverter chains depends on the size of the output transistors, and hence the size of the load.
Output PMOS and NMOS transistors

Advantages

a) Minimize the power consumption than in the case of traditional tapered buffers.

Disadvantages

a) Do not focus on delay introduced.
   b) Presence of two paths for the clock can cause problem of mismatch.

2. CML buffers

Circuit:
Current-mode logic (CML) buffer is based on the differential architecture.

Minimizing the overall propagation delay of CML buffer increases the overall operation frequency of the buffer significantly.

They can also be tapered.

**Theory of operation**

ISS provides an input-independent biasing for the circuit.

$C_d$, that will diminish the effects of input-output coupling through the device overlap capacitance $C_{gd}$.

To achieve the best performance in a CML buffer, a complete current switching must take place, and the current produced by the tail current needs to flow through the ON branch only.

The load resistors should be small in order to reduce the RC delay and increase the bandwidth.

To guarantee a high-speed operation, NMOS transistors of the differential pair must operate only in the saturation.

**Advantages**

- a) CML circuits can operate with higher operating frequency at lower supply voltage than CMOS circuits can.
- b) The differential architecture of a CML buffer makes it functionally robust in the presence of environmental noise sources (e.g., crosstalk, power/ground noise).

**Disadvantages**

- a. The maximum output swing of a CML buffer is less than that of a CMOS inverter.
- b. CML circuits are power hungry.
3. **Tapered buffers:**

\[
\text{In} \quad \begin{array}{c}
\uparrow \vspace{0.5cm} \\
C_{g.1}
\end{array} \quad \begin{array}{c}
\uparrow \\
1
\end{array} \quad \begin{array}{c}
\uparrow \\
2
\end{array} \quad \begin{array}{c}
\quad \cdots \\
\quad N
\end{array} \quad \begin{array}{c}
\uparrow \\
C_L
\end{array} \quad \text{Out}
\]

Tapering is functional in reducing the loading effect when large capacitive loads are to be driven. Tapering holds the meaning of increasing the sizes of the inverter stages by a fixed ratio such that each inverter is larger in size than the one before it by a fan out.

When the fan out of all inverter stages is the same, this will cause each stage to have same delay as the others i.e the total delay is divided equally on the stages and hence the total delay will be minimum which is required.

The tapered train of inverters start with a stage that acts as a reference with minimum size so as to have a small input capacitance and prevents loading on the input signal.

Delay depends on number of stages used that in turn is function of the fan out used and the load capacitance to be driven.

Fan out has an optimum value which is 4, this value gets a minimum delay and this can be clarified through the following figures.

**Advantages**

1) Simple and easy design.
2) No mismatch problem.
3) Gives large swing at the output.

**Disadvantages**

1) High power consumption due to short circuit power.
2) Not a robust architecture against noise.
This is the used topology in our pre-driver design.

The design of the pre-driver buffer stages will be as follows:

Figure 1.2.9 Pre-driver Design
Table 1.2.1 Sizing of the upper branch

<table>
<thead>
<tr>
<th></th>
<th>pmos</th>
<th>nmos</th>
<th>length</th>
<th>width</th>
<th>Number of fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1\textsuperscript{st} inverter</td>
<td>60n</td>
<td></td>
<td>470n-200n</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2\textsuperscript{nd} inverter</td>
<td>60n</td>
<td></td>
<td>1.88u-800n</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3\textsuperscript{rd} inverter</td>
<td>60n</td>
<td></td>
<td>7.53u-3.2u</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1.2.2 Sizing of the lower branch

<table>
<thead>
<tr>
<th></th>
<th>pmos</th>
<th>nmos</th>
<th>length</th>
<th>width</th>
<th>Number of fingers</th>
</tr>
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<tbody>
<tr>
<td>1\textsuperscript{st} inverter</td>
<td>60n</td>
<td></td>
<td>470n-200n</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2\textsuperscript{nd} inverter</td>
<td>60n</td>
<td></td>
<td>470n-200n</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3\textsuperscript{rd} inverter</td>
<td>60n</td>
<td></td>
<td>1.88u-800n</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4\textsuperscript{th} inverter</td>
<td>60n</td>
<td></td>
<td>7.52u-3.2u</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1.2.10 Input Waveform
Figure 1.2.11 Output Waveform

Figure 1.2.12 Pre-driver Eye Diagram

Table 1.2.3 Pre-Driver Readings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1 V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>0.4 mA</td>
</tr>
<tr>
<td>Power</td>
<td>0.4 mW</td>
</tr>
</tbody>
</table>
1.3 Driver and Termination

1.3.1 Concept Review

![Schematics of (a) CML Driver, (b) SLVS Driver]

Figure 1.3.1 shows the schematics of differential CML driver and SLVS driver. It should be noted that both links have double termination structures.

**CML Driver**

Assuming the output swing is $V_{OUT}$, the current required of the CML driver is $(V_{OUT})/(R/2)$ because the current drives the two parallel termination resistors.

**SLVS Driver**

In contrast to the CML driver, the SLVS driver with differential-mode termination can deliver all the current to the channel and this current passes through the 2R termination resistor. With the same $V_{OUT}$, the current of the SLVS driver is $(V_{OUT}) / (2R)$. 


Conclusion
From this analysis, the theoretical power dissipation of the SLVS driver is approximately one-fourth of the CML driver. Therefore, The SLVS driver has lower power consumption than the CML driver.

1.3.2 Circuit Review

![One segment driver](image)

Figure 1.3.2 One segment driver

In high speed serial-links, the output impedance matching is important to reduce signal reflections. But the resistance provided by the mosfets varies across the process corners so we need to calibrate the termination to achieve good matching.

The termination circuit consists of 22 fixed segments and 78 controllable unit segments tied together for pull up network and 23 controllable unit segments tied together for pull down network. The fixed segments are always turned on, and other unit segments will be set by calibration.
Driver is working for two amplitudes, large amplitude at which $V_{dd} = 0.4V$ and small amplitude at which $V_{dd} = 0.2V$.

Driver implementation depends on output swing requirements but as supply voltage changes, the implementation does not change; only the number of segments differs to achieve matching.

Table 1.3.1 It shows the Mosfets sizing of the driver

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Width</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS up</td>
<td>300 nm</td>
<td>60 nm</td>
</tr>
<tr>
<td>NMOS down</td>
<td>260 nm</td>
<td>75 nm</td>
</tr>
</tbody>
</table>
1.3.3 **Settled topology**

The termination calibration is performed by applying a DC current to the driver output and comparing the driver output with a threshold through two comparators. This method calibrates pull-up and pull-down paths independently to achieve an optimum termination value for both cases.
1.3.4  **Final design Achieved**

First, Calibrating the pull up network independently by deactivating all the switches of the pull down network. To start calibration of the pull up, switch 0 will be off and switch 1 will be on. Then, according to the programmable bit; switches of the current source and $V_{ref}$ of SA (switch 2&4) or LA (switch 3&5) will be closed. After that, the output of the comparator is 0 logic when $V_{out} < V_{ref}$ and this means closing a segment. But, when the output of the comparator is 1 logic when $V_{out} > V_{ref}$ and this means opening a segment. The comparator will follow this scenario until its output is 101 or 010, and this indicates that
calibration of the pull up is finished then deactivate switches of current source and switch 1.

Second, Calibrating the pull down network will follow the same steps as that of the pull up.

Third, switch 0 & 6 will be on to feed the data into the driver.

1.3.5 **Specifications Required and Met**

a) $R_{SE_{TX}}$ (Single ended output resistance) in the range from 40 Ω up to 60 Ω.

b) $\Delta R_{SE_{TX}}$ (Output resistance mismatch) is 6 Ω.

![Figure 1.3.7 Single ended output resistance in case of SA](image)
Table 1.3.2 It shows the variation of the single ended output resistance across process corners and the number of the pull up and down segments in case of SA

Table 1.3.3 It shows the variation of the single ended output resistance across process corners

<table>
<thead>
<tr>
<th>Corner</th>
<th>Temp</th>
<th>Supply</th>
<th>RSE_TX Left</th>
<th>RSE_TX Right</th>
<th>Δ RSE_TX</th>
<th>No of Pull up Segment</th>
<th>No of Pull down Segment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>27</td>
<td>200</td>
<td>52.637</td>
<td>52.5203</td>
<td>0.1167</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>TT</td>
<td>27</td>
<td>205</td>
<td>53.2215</td>
<td>52.624</td>
<td>0.5975</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>TT</td>
<td>27</td>
<td>195</td>
<td>52.065</td>
<td>52.415</td>
<td>0.35</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>TT</td>
<td>-40</td>
<td>200</td>
<td>54.727</td>
<td>52.736</td>
<td>1.991</td>
<td>26</td>
<td>26</td>
</tr>
<tr>
<td>TT</td>
<td>85</td>
<td>200</td>
<td>53.3878</td>
<td>54.8075</td>
<td>1.4197</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>FF</td>
<td>27</td>
<td>200</td>
<td>50.334</td>
<td>53.258</td>
<td>2.924</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>FF</td>
<td>-40</td>
<td>200</td>
<td>50.725</td>
<td>52.445</td>
<td>1.72</td>
<td>22</td>
<td>22</td>
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<td>85</td>
<td>200</td>
<td>50.963</td>
<td>54.975</td>
<td>4.012</td>
<td>27</td>
<td>27</td>
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<tr>
<td>SS</td>
<td>27</td>
<td>200</td>
<td>53.857</td>
<td>49.195</td>
<td>4.662</td>
<td>38</td>
<td>38</td>
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<tr>
<td>SS</td>
<td>-40</td>
<td>200</td>
<td>52.56</td>
<td>47.66</td>
<td>4.9</td>
<td>36</td>
<td>34</td>
</tr>
<tr>
<td>SS</td>
<td>85</td>
<td>200</td>
<td>51.967</td>
<td>49.29</td>
<td>2.677</td>
<td>42</td>
<td>42</td>
</tr>
</tbody>
</table>

Figure 1.3.8 Single ended output resistance in case of LA
corners and the number of the pull up and down segments in case of LA

<table>
<thead>
<tr>
<th>Corner</th>
<th>Temp</th>
<th>Supply (mV)</th>
<th>( R_{SE_TX} ) up (ohm)</th>
<th>( R_{SE_TX} ) down (ohm)</th>
<th>( \Delta R_{SE_TX} ) (ohm)</th>
<th>No of Pull up Segment</th>
<th>No of Pull down Segment</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>-40</td>
<td>390</td>
<td>49.037</td>
<td>51.35</td>
<td>2.313</td>
<td>58</td>
<td>29</td>
</tr>
<tr>
<td>TT</td>
<td>-40</td>
<td>400</td>
<td>51.0537</td>
<td>51.503</td>
<td>0.4493</td>
<td>58</td>
<td>29</td>
</tr>
<tr>
<td>TT</td>
<td>-40</td>
<td>410</td>
<td>53.072</td>
<td>51.64</td>
<td>1.432</td>
<td>58</td>
<td>29</td>
</tr>
<tr>
<td>TT</td>
<td>27</td>
<td>390</td>
<td>49.638</td>
<td>47.903</td>
<td>1.731</td>
<td>56</td>
<td>35</td>
</tr>
<tr>
<td>TT</td>
<td>27</td>
<td>400</td>
<td>51.276</td>
<td>48.035</td>
<td>3.241</td>
<td>56</td>
<td>35</td>
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<tr>
<td>TT</td>
<td>27</td>
<td>410</td>
<td>52.938</td>
<td>48.16</td>
<td>4.778</td>
<td>56</td>
<td>35</td>
</tr>
<tr>
<td>TT</td>
<td>85</td>
<td>390</td>
<td>50.427</td>
<td>54.034</td>
<td>3.607</td>
<td>56</td>
<td>35</td>
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<tr>
<td>TT</td>
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<td>400</td>
<td>51.897</td>
<td>54.203</td>
<td>2.306</td>
<td>56</td>
<td>35</td>
</tr>
<tr>
<td>TT</td>
<td>85</td>
<td>410</td>
<td>53.384</td>
<td>54.373</td>
<td>0.989</td>
<td>56</td>
<td>35</td>
</tr>
<tr>
<td>FF</td>
<td>-40</td>
<td>390</td>
<td>51.242</td>
<td>51.9795</td>
<td>0.7375</td>
<td>36</td>
<td>24</td>
</tr>
<tr>
<td>FF</td>
<td>-40</td>
<td>400</td>
<td>52.979</td>
<td>52.153</td>
<td>0.826</td>
<td>36</td>
<td>24</td>
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<tr>
<td>FF</td>
<td>27</td>
<td>390</td>
<td>46.529</td>
<td>46.965</td>
<td>0.436</td>
<td>42</td>
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<tr>
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<td>27</td>
<td>400</td>
<td>47.886</td>
<td>47.107</td>
<td>0.779</td>
<td>42</td>
<td>30</td>
</tr>
<tr>
<td>FF</td>
<td>27</td>
<td>410</td>
<td>49.2945</td>
<td>47.245</td>
<td>2.0495</td>
<td>42</td>
<td>30</td>
</tr>
<tr>
<td>FF</td>
<td>85</td>
<td>390</td>
<td>56.524</td>
<td>52.71</td>
<td>3.814</td>
<td>36</td>
<td>30</td>
</tr>
<tr>
<td>FF</td>
<td>85</td>
<td>400</td>
<td>50.113</td>
<td>53.242</td>
<td>3.129</td>
<td>42</td>
<td>30</td>
</tr>
<tr>
<td>FF</td>
<td>85</td>
<td>410</td>
<td>51.4</td>
<td>53.43</td>
<td>2.03</td>
<td>42</td>
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<tr>
<td>SS</td>
<td>-40</td>
<td>390</td>
<td>52.69</td>
<td>49.23</td>
<td>3.46</td>
<td>90</td>
<td>36</td>
</tr>
<tr>
<td>SS</td>
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<td>400</td>
<td>52.274</td>
<td>51.33</td>
<td>0.944</td>
<td>98</td>
<td>35</td>
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<tr>
<td>SS</td>
<td>-40</td>
<td>410</td>
<td>55.224</td>
<td>51.3538</td>
<td>3.8702</td>
<td>95</td>
<td>35</td>
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<tr>
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<td>27</td>
<td>390</td>
<td>49.118</td>
<td>50.8625</td>
<td>1.7445</td>
<td>88</td>
<td>40</td>
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<tr>
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<td>27</td>
<td>400</td>
<td>50.908</td>
<td>50.993</td>
<td>0.085</td>
<td>88</td>
<td>40</td>
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<tr>
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<td>27</td>
<td>410</td>
<td>52.656</td>
<td>51.122</td>
<td>1.534</td>
<td>88</td>
<td>40</td>
</tr>
<tr>
<td>SS</td>
<td>85</td>
<td>390</td>
<td>48.55</td>
<td>52.36</td>
<td>3.81</td>
<td>86</td>
<td>43</td>
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<tr>
<td>SS</td>
<td>85</td>
<td>400</td>
<td>49.268</td>
<td>51.095</td>
<td>1.827</td>
<td>88</td>
<td>44</td>
</tr>
<tr>
<td>SS</td>
<td>85</td>
<td>410</td>
<td>49.99</td>
<td>49.88</td>
<td>0.11</td>
<td>90</td>
<td>45</td>
</tr>
</tbody>
</table>
The M-Tx drives a differential low-swing signal with either Large Amplitude or Small Amplitude.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DIF, DC, LA, RT, TX}$</td>
<td>160 mV</td>
<td>240 mV</td>
</tr>
<tr>
<td>$V_{DIF, DC, SA, RT, TX}$</td>
<td>100 mV</td>
<td>130 mV</td>
</tr>
<tr>
<td>$V_{CM, LA, TX}$</td>
<td>160 mV</td>
<td>260 mV</td>
</tr>
<tr>
<td>$V_{CM, SA, TX}$</td>
<td>80 mV</td>
<td>190 mV</td>
</tr>
</tbody>
</table>

Figure 1.3.9 Single ended output waveform for SA at TT
Figure 1.3.10 Eye diagram for SA driver at TT

a) $V_{CM\_SA\_TX}$ is around 100 mV.

b) $V_{DIF\_DC\_SA\_RL\_TX}$ is around 100 mV.

Figure 1.3.11 Single ended output waveform for LA at TT
Figure 1.3.12 Eye diagram for LA driver at TT

a) $V_{CM,LA,\text{TX}}$ is around 200 mV.
b) $V_{DIF\,DC,LA,\text{RL, TX}}$ is around 200 mV.

**HS frequencies used in the S-parameters templates**

$$F_{HS} = \frac{D_{RHS}}{2} = 5\text{GHz}$$

$$F_{HS,\text{MIN}} = \frac{D_{RHS}}{10} = 1\text{GHz}$$

$$F_{HS,\text{MAX}} = \frac{3 \times D_{RHS}}{4} = 7.5 \text{GHz}$$
Figure 1.3.13 $S_{11}$ mask for SA at TT

Figure 1.3.14 $S_{11}$ mask for LA at TT
1.4 Whole Transmitter

![Block diagram of the whole transmitter](image)

Figure 1.4.1 Block diagram of the whole transmitter

![Single ended for SA TX at TT](image)

Figure 1.4.2 Single ended for SA TX at TT
Figure 1.4.3 Single ended for LA TX at TT

Figure 1.4.4 Eye diagram for SA TX at TT
Figure 1.4.5 Eye diagram for LA TX at TT

Figure 1.4.6 (a) Rise Time, (b) Fall Time for SA TX at TT
Figure 1.4.7 (a) Rise Time , (b) Fall Time for SA TX at SS

Figure 1.4.8 (a) Rise Time , (b) Fall Time for LA TX at TT
Figure 1.4.9 (a) Rise Time, (b) Fall Time for LA TX at SS

Table 1.4.1 Rise and Fall time for SA & LA at TT & SS

<table>
<thead>
<tr>
<th>Corner</th>
<th>Amplitude</th>
<th>Rise Time (ps)</th>
<th>Fall Time (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>SA</td>
<td>13.172</td>
<td>14.242</td>
</tr>
<tr>
<td>SS</td>
<td>SA</td>
<td>14.79</td>
<td>16.66</td>
</tr>
<tr>
<td>TT</td>
<td>LA</td>
<td>12.9291</td>
<td>17.218</td>
</tr>
<tr>
<td>SS</td>
<td>LA</td>
<td>16.98</td>
<td>19.957</td>
</tr>
</tbody>
</table>

Table 1.4.2 It shows the Power consumption and Efficiency

<table>
<thead>
<tr>
<th>Blocks</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>16:1 multiplexer</td>
<td>56.4 µW</td>
</tr>
<tr>
<td>Pre-driver</td>
<td>400 µW</td>
</tr>
<tr>
<td>Driver</td>
<td>800 µW</td>
</tr>
<tr>
<td>Total Power Efficiency</td>
<td>1.2564 mW/10Gb/s=0.12564mW/Gb/s</td>
</tr>
</tbody>
</table>
Figure 1.4.10 Power Consumption in TX
Chapter 2: Receiver

2.1 Receiver Termination

2.1.1 Concept Review

Termination is a matching part between the channel and the transmitter and the receiver to prevent the signal from reflection and ensure that all the transmitted data enter the channel then enter the receiver.

2.1.2 Circuit Review

We have different types of termination and different classifications.

Example: on-chip and off-chip termination, ac coupling and dc coupling, active and passive termination.

Passive termination consist of resistance while active termination consist of transistors. We use combination of both of them to achieve our required specs, such that we use the transistors as an on/off switch connected to the resistance in branches.
2.1.3 **Settled topology**

We have different ways to connect this termination

![Diagram](image)

Figure 2.1.1 (a) differential Resistance (b) Resistance to ground (c) Resistance to Vdd

First we design figure 2.1.1 (c) as a termination

![Diagram](image)

Figure 2.1.2 (Resistance to Vdd schematic)

With minimum length 60n and 55u width PMOS transistors the transistor is on and off by changing the gate volt between vdd and gnd.
But when we connect it to the transmitter it doesn’t work right and figure 2.1.2 although doesn’t work right.

So we have to make termination like in figure 2.1.1(a) (differential termination).

2.1.4 **Final design Achieved**

The required resistance to match is 50 ohm so when we make a differential termination it becomes 100 ohm, this design in figure 2.1.3 achieve the 100 Ohms.

![Figure 2.1.3 (differential resistance schematic)](image)

As we see two transistors as a switch when on the branch will be parallel to the 140 Ohms resistance, we have these two branches for the corners analysis.

**For typical-typical resistance case**, we have Q3 transistor is on so that we have 140 Ohms parallel to 350 Ohms gives total resistance 100 Ohms.
For fast-fast resistance case, the two transistors are off, so that the 140 Ohms become 98.8 Ohms.

For slow-slow resistance case the two transistors are on having 140//350//310 given 98.2 Ohms total.

This design needs a control circuit to control the transistors to be on and off, this control circuit consists of a circuit that sense the value of the resistance and then send a (0,1) code to on and off the transistors.

2.1.5 Specifications Required and Met

The specs required are between 80 to 110 Ohms. Across corners the resistance value is in this range. While the s11 required is given by

Table 2.1.1 S_{11} mask

<table>
<thead>
<tr>
<th>frequency</th>
<th>0 HZ</th>
<th>(F_{min}=1.16\ \text{GHZ})</th>
<th>(F=5.8\ \text{GHZ})</th>
<th>(F_{max} = 8.7\text{GHZ})</th>
</tr>
</thead>
<tbody>
<tr>
<td>S_{11}</td>
<td>-17dB</td>
<td>-17dB</td>
<td>-4.8dB</td>
<td>-3dB</td>
</tr>
</tbody>
</table>

For calculating \(S_{11}\) we use 2 ports and transform equations between 2 ports and 1 port \(S_{11}\).

So we calculate \(S_{dd11}\) in stand of \(S_{11}\)

\[ S_{dd11} = \frac{1}{2} (S_{11} - S_{12} - S_{21} + S_{22}) \]

For typical-typical \(S_{11} = S_{22} = 0.53, S_{21} = S_{12} = 0.469\)

\(S_{dd11} = 20 \log (0.5\times0.06) = -24\text{dB}\)
Table 2.1.2 $S_{dd1\ 1}$ results

<table>
<thead>
<tr>
<th>corners</th>
<th>TT</th>
<th>SS</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{dd1\ 1}$</td>
<td>-29dB</td>
<td>-28dB</td>
<td>-35dB</td>
</tr>
</tbody>
</table>

2.1.6 Layout

![Layout diagram](image)

Figure 2.1.4 (layout of termination)

2.1.7 Conclusion

The termination satisfy the required specs from it, it match the circuit well with the channel and transmitter.
2.2 Receiver Equalizer

Receiver side equalization offers an alternate method to mitigate ISI without any peak power constraint. The loss in channel is suppressed by boosting the high frequency signal spectrum rather than attenuating low frequency content. We now present linear receive equalization architectures:

2.2.1 Discrete time equalizer (FIR)

I- Digital FIR equalizer:

This kind can be used in transmitter as a pre-emphasis and its input is a binary signal unlike that in receiver case whose input is the channel output which is analog in nature and that requires an ADC. Depending on the number of taps and the amount of each tap delay we can control certain frequency components.

![Digital FIR equalizer](image)

Figure 2.2.1 Digital FIR equalizer
II- **Analog FIR equalizer:**

Number of taps determined by amount of power and the link pulse response. Spacing between taps (tap delay), which is usually a fraction of T since it reduces the aliasing and improves the performance.

![Diagram of Analog FIR equalizer](image)

**Figure 2.2.2 Analog FIR equalizer**

**The reasons for not using FIR filter:** Sampling clock jitter reduces the equalization performance. And the needed sampling in front end of receiver dictates that Clock recovery to be in raw with the channel which results in excessive jitter, consequently practical discrete-time FIR equalizer needs source synchronous interface containing separate clock channel moreover, Complexity of the analog delay-time circuit.

2.2.2 **Continuous Time linear equalizer**

Physical channel of high-speed serial data links is usually of a low-pass nature. A passive high-pass filter (HPF) or active HPF is able to flatten the joint frequency domain channel response and reduce ISI. The HPF can be continuous time analog filter composed of passive RLC. In addition, the HPF cells are usually connected in cascade to give more gain at high frequencies.
Receiver continuous time analog linear equalizers are not sampled Therefore, clock jitter does not affect their performance.

However, there are many challenges for this kind of equalizer.

**Some challenges are listed as follows**

a. It has limited tuning range and rarely matches channel, especially when there are both frequency dependent attenuation and frequency dependent delay.

b. Linearity is a challenge, especially when input swings vary greatly in amplitude.

c. Limited by gain bandwidth of each stage of differential pair.

d. It is sensitive to PVT variations.

e. It is sensitive to device mismatch and non-linearity.

f. Offset cancellation and calibration are difficult.

Continuous time analog Rx linear equalizers are sometimes used as pre-equalizer for decision feedback equalizer. The task is to make the impulse response causal, with most of its energy concentrated in the time origin (with some fixed delay).

I- **Inductive peaking**

The availability of monolithic inductors may suggest the use of under damped complex poles to provide the required boost at high frequencies. For example, the shunt-peaking circuit of a following transfer function

\[
T(s) = \frac{k(s + \omega_z)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}
\]
While providing enough boost to match the inverse of the FR4 frequency response, high-complex poles introduce substantial phase distortion. As an example, a cascade of two such stages is designed to equalize a 30-in trace [Fig. (b)], yielding the equalized eye shown in Fig. (d).
This issue restricts realizations to non-feedback structures containing real zeros and poles.
II- Capacitive degeneration

![Capacitive degeneration diagram](image)

Figure 2.2.7 Capacitive degeneration

\[
|\omega_Z| \approx \frac{1}{R_S C_S}
\]

\[
|\omega_{p1}| \approx \frac{1}{R_D C_P}
\]

\[
|\omega_{p2}| \approx \frac{1 + \frac{g_m R_S}{R_S C_S}}{R_S C_S}
\]

Improving the linearity of the stage, degeneration nonetheless creates a trade-off between the low-frequency gain and the boost factor, \( \omega_{p1}/ \omega_Z \). Interestingly, one can write

\[
A_0 \frac{\omega_{p1}}{\omega_{p2}} \approx \frac{g_m}{C_P}
\]
The degenerated structure trades this gain-bandwidth product for the boost factor, the low-frequency gain, and the linear range.

As the number of stages in the cascade increases to achieve a higher boost factor, the overall bandwidth tends to drop unless a greater low-frequency loss is allowed in each stage.

for a total boost factor of 24 dB at 5.8 GHz and an overall bandwidth of 7 GHz, two degenerated stages with a low-frequency loss of 9 dB per stage are required, which may affect the receiver sensitivity. **Which we used.**

2.2.3 **Schematic and Simulation results**

Here we use PMOS due to our small input common mode according to MIPI standards.

![Schematic of CTLE](image)

Figure 2.2.8 Schematic of CTLE

By varying channel length it results in different losses and hence for different boost factors which is controlled by varying the degeneration resistance and capacitance.
Figure 2.2.9 Variation of boosting across channels

1.2.2 Table

<table>
<thead>
<tr>
<th>Channel (in)</th>
<th>Rs  (fF)</th>
<th>Cs (fF)</th>
<th>Boost factor (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>430</td>
<td>125</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>645</td>
<td>104</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>950</td>
<td>94</td>
<td>5.5</td>
</tr>
<tr>
<td>10</td>
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<td>84</td>
<td>9.5</td>
</tr>
<tr>
<td>16</td>
<td>2.15K</td>
<td>94</td>
<td>11</td>
</tr>
<tr>
<td>20</td>
<td>2.8K</td>
<td>183</td>
<td>14</td>
</tr>
</tbody>
</table>
And that boost factor can be controlled either digitally by branches of switches of resistors and branches of Capacitors, but that will make controlling the capacitance values for boosting somehow difficult as the transistor which acting as switches will add its capacitances so, we can make it by analog control and here we need only one branch of one transistor whose gate voltage is controlled to get the required resistance and using mos cap also controlled by voltage to get the required boosting.

Figure 2.2.10 channel loss and CTLE boosting for 10-in
Figure 2.2.11 Before and after CTLE for 10-in

Figure 2.2.12 Before and after slicer for 10-in
Figure 2.2.13 Before and after CTLE for 20-in

Figure 2.2.14 Before and after slicer for 20-in
Figure 2.2.16 30-channel loss and CTLE boosting

Figure 2.2.15 before and after CTLE for 30-in channel
Figure 2.2.17 before and after slicer for 30-in

Figure 2.2.18 when composing receiver and transmitter circuits
Power consumed by CTLE = 2.47 mw

By increasing CTLE stages we can get higher boosting but limited BW.

It meet the spec to have the minimum differential amplitude to be in slicer range so we didn't need a gain stage.
2.3 Clock and Data Recovery (CDR)

Introduction

Clock and data recovery (CDR) is a critical function in high-speed transceivers. Such transceivers serve in many applications, including optical communications, backplane routing, and chip-to-chip interconnects. The data received in these systems are both asynchronous and noisy, requiring that a clock be extracted to allow synchronous operations. Furthermore, the data must be “retimed” such that the jitter accumulated during transmission is removed. In order to perform synchronous operations such as retiming and de-multiplexing on random data, high-speed receivers must generate a clock. As illustrated in Fig. 1a, a clock recovery circuit senses the data and produces a periodic clock. A D flip flop (DFF) driven by the clock then retimes the data (i.e., it samples the noisy data), yielding an output with less jitter. As such, the flip flop is sometimes called a decision circuit.

The clock generated in the CDR must satisfy three important conditions

1) It must have a frequency equal to the data rate; for example, a data rate of 11.648 Gb/s (each bit 85.851 ps wide) translates to a clock frequency of 11.648 GHz (with a period of 85.851 ps).

2) It must bear a certain phase relationship with respect to data, allowing optimum sampling of the bits by the clock; if the rising edges of the clock coincide with the midpoint of each bit, the sampling occurs farthest from the preceding and following data transitions, providing maximum mar-gin for jitter and other timing uncertainties.
3) It must exhibit a small jitter since it is the principal contributor to the retimed data jitter.

2.3.1 CDR Architectures

1. PLL based CDR

1.1 PLL based CDR without reference frequency:

Figure 2.4.1 shows architecture without a reference clock, where a frequency tracking loop provides a frequency comparison through the frequency detector (FD) and a phase tracking loop leads to phase locking through the phase detector (PD). The FD module provides a frequency comparison between the input data, D(in), and the voltage-controlled oscillator (VCO) output clock which eliminates the need for using an external reference frequency. During either CDR startup or loss of phase lock, the FD is activated to produce a control voltage through the charge pump (CP) and the loop filter (LF), which moves the VCO oscillation frequency toward the input data rate. Once the frequency difference falls within the phase tracking loop’s capture range, the PD takes over and allows the VCO output clock phase to lock onto the input data phase.
There are two possible issues associated with this architecture:

1) the frequency tracking loop and the phase tracking loop may potentially interfere with each other during the interval when the FD transfers control to the PD, resulting in a failure to lock onto the phase and/or ripple generation on the VCO control line.

2) The FD could become momentarily “confused” about the actual input data rate if the received input data consists of random consecutive identical digits or if the received rising and falling edges are corrupted by external or internal noise during the transmission.

### 1.2 PLL based CDR with reference frequency:

Frequency loop operates during startup or loss of phase lock. Ideally should be mostly off in normal operation.

**Advantages**

1) Input jitter rejection.

2) Input frequency tracking.

**Disadvantages**

1) Jitter peaking

2) Large loop filter Area

3) Long Acquisition time
Analog Phase Interpolator based CDR (Selected Topology)

The VCO generates multiple clock phases that the PI interpolates between them to get the phase equivalent to the input voltage. The input control voltage of the PI is coming from a bang bang phase detector followed by a charge pump and a loop filter. The bang bang PD generate up and down pulses that the charge pump convert into control current that charge and discharge a capacitor.

Advantages

1) Multichannel Share Input Clocks.

2) High resolution, so less jitter.
2.4 Phase Detector (PD)

2.4.1 Concept Review

CDR phase detectors compare between the phase of the clock and the received data, and it generate pulses that indicate the phase difference between them.

Random Data

When the incoming data has a spectral energy at the clock frequency, a synchronous clock tuned to the nominal clock frequency. In most signaling formats as NRZ data the data spectrum has no components at the clock frequency making it necessary to use clock recovery.

![Power Spectral Density of an NRZ Signal](image)

Figure 2.4.1 Random data spectrum

The phase detectors used for periodic signals can't work properly if they detect random signal.

For example, XOR gate can't work for random data, the XOR gate produces a zero average at the output if the ONEs and ZEROs in input data occur with equal probabilities.
IF we consider a D flip flop as a PD, first if we suppose that the flip flop senses the random data at its D input and the clock at its clock input, as shown in the figure the clock samples the data at each rising edge of the clock producing a delayed replica of the input data, so if the random data has equal number of ONEs and ZEROs will produce a zero average too, Second if we suppose that the data samples the clock, if the data lags the clock, the flip flop continues to sample the high level of the clock producing a positive output, and if the data leads the clock, the flip flop produces a negative output, thus the output signifies the polarity of the phase difference between the input data and the clock.

The output of the flip flop takes only two values so it's a binary PD.
There are two basic types of phase detectors used in CDR circuits, linear phase detectors and binary phase detectors. These circuits are named based on how they respond to phase errors. A linear phase detector generates correction information which is proportional to the size of the phase error. On the other hand, a binary phase detector applies correction of the same magnitude regardless of how large or small the phase error is. The ideal phase detector gain of linear and binary phase detectors is illustrated in Figure 2.3.7. The x-axis represents the phase error between the clock and data signals, where $\Delta \Phi = 0$ represents the situation where the signals are perfectly aligned. The y-axis represents the output of the phase detectors, which will be discussed next.
Linear phase detectors

A linear phase detector is also known as a proportional phase detector, as it corrects for phase errors in proportion to their magnitudes. The proportional nature of the phase detector gain leads to low activity on the VCO control voltage when the CDR circuit is in the locked condition, which in turn leads to good jitter performance. The linear response of this circuit allows for simple formulation of loop equations, which is very helpful for system analysis. Virtually all linear phase detectors operate in a similar manner.

To a Hogge phase detector, hence it will be used as the reference linear phase detector. The architecture of the Hogge phase detector is shown in Figure 2.3.8. The Hogge phase detector generates UP and DOWN pulses which control the charge pump. Figure 2.3.9 illustrates the logical operation of the Hogge phase detector in two situations: when the CDR circuit is in the ideal locked state and when there is a phase error. When the CDR circuit is perfectly locked the clock and data are synchronized and the UP and DOWN
pulses are exactly equal, as can be seen in Figure 2.3.9a. With UP and DOWN pulses of equal width an equal amount of charge is added to and subtracted from the loop filter. As such the voltage on the loop filter has no net change. Figure 2.3.9b illustrates the situation where the clock is leading the data. With this phase error, the width of the UP pulse is reduced such that there will be a net loss of charge from the loop filter. This correction will adjust the phase of the PI so as to correct the phase error.

![Figure 2.4.5 Architecture of Hogge phase detector](image)

In the Hogge phase detector the DOWN pulse is generated by performing the logical XOR over the outputs of the two DFFs, therefore it has a constant width of half a period regardless of the phase error between the clock and data signals. The UP pulse is generated by performing the logical XOR over the input data signal and the output of the first DFF. While the output of the DFF is phase aligned with the clock, the input data signal is not. Therefore it
is the UP pulse which contains the information as to whether the clock is leading or lagging the data and by what amount.

![Operation of Hogge phase detector](image)

**Figure 2.4.6 Operation of Hogge phase detector**

**Binary phase Detectors**

The name of the linear phase detector alludes to its proportional nature and similarly the name of the binary phase detector describes the nature of its correction. In a binary phase detector there are only two states, which correspond to whether the clock is leading or lagging the data. With a binary
phase detector no information is generated as to the magnitude of the phase error. There are numerous binary phase detector architectures like the D flip flop we discussed earlier, which is the simplest binary PD. The advantages of this phase detector lie primarily in its simplicity, as a single DFF comprises the entire phase detection circuitry. This simplicity means that the circuit is robust and has little sensitivity to process non-idealities, however, the DFF phase detector also has several disadvantages.

One problem with the DFF phase detector is the lack of integrated retiming, requiring the second DFF seen in Figure 2.3.5. The Hogge phase detector and the Alexander phase detector (which will be discussed next) both have integrated retiming. This is important, as it guarantees that there is no skew between the retiming clock signal and the phase aligned clock signal, as they are one and the same. A DFF phase detector based CDR circuit needs a separate retiming circuit, and care must be taken to ensure that clock skew is not a problem. A second problem with the DFF phase detector is the fact that it supplies correction information to the charge pump even when there are no data transitions. The phase detector can only determine the phase relationship between the clock and data when there is a data transition. This means that when there are long strings of ‘1’s or ‘0’s, the CDR circuit continues to implement the last known correction. This information may not be correct and this could cause the CDR circuit to lose lock. Many binary phase detectors have a third state during which no information is sent to the charge pump. These phase detectors are known as tri-state or ternary phase detectors.
Alexander phase detector

The Alexander phase detector is another binary architecture, and it is the one most commonly implemented in multi-Gb/s CDR circuits. This circuit samples the data signal at three points and uses logic to determine whether the data is leading or lagging the clock. Figure 2.3.9 illustrates the result of sampling in two cases: when the clock leads the data and when the clock lags the data. DFFs are used to acquire the sample points $S_0$, $S_1$, $S_2$, and XOR gates are used to determine the phase error.

The architecture of the Alexander phase detector is shown in Figure 2.3.11

![Figure 2.4.7 The sampling behavior of Alexander phase detector](image1)

![Figure 2.4.8 Architecture of Alexander phase detector](image2)
One important difference between the DFF phase detector and the Alexander phase detector is the tri-state nature of the Alexander phase detector. This means that the Alexander phase detector actually has three logical states, as opposed to two. The three states are: data leading clock, data lagging clock and no transition. The ‘no transition’ state is important, as it means that when there are no transitions in the data, the phase detector will not provide any correction information to the charge pump. This allows the CDR circuit to stay locked, even when there are long strings of ‘0’s or ‘1’s. As mentioned before, another benefit of the Alexander phase detector is the integrated retiming. This can be seen in Figure 2.3.11 where the output of DF F2 is taken as the retimed data signal. The primary downside of the Alexander phase detector as compared to the DFF phase detector is its complexity. The Alexander phase detector requires four DFFs and two XOR gates and the extra logic consumes power and area. The increased complexity also leads to a greater sensitivity to process non-idealities.

**Half rate phase detectors**

At very high speeds it may be difficult to design oscillators that provide an adequate tuning range with reasonable jitter. For this reason CDR circuits may sense the input random data at full rate but employ a VCO running at half the input rate. This technique also relaxes the speed requirements of the phase detector.

The obvious benefit of a multi-rate architecture is the lower frequency of operation; however there are several downsides which must be considered. First, as there architectures use both the in-phase and quadrature clock signals, the clock phases must be very precise. Any mismatch between the in-phase and quadrature clock signals will degrade overall system performance.
There are linear and binary half rate phase detector, here we worked with binary PD, a three state Alexander phase detector

**Selected topology:**

The chosen topology is half rate binary PD, this phase detector samples the data at the current and following center and the 2 edges (at 0, 90, 180, 270 phases) of the data producing D0, D90, D180, D270 similar to the full rate Alexander PD. The phase detector logic is as follows:

\[
\begin{align*}
\text{Down 1} &= D0 + D90 \\
\text{Down 2} &= D180 + D270 \\
\text{UP 1} &= D90 + D180 \\
\text{UP 1} &= D270 + D0
\end{align*}
\]

Instead of using one up and one down signals we used 2 ups and 2 downs, each control signal is valid for 270 degrees, we multiplex the 2 ups and the 2 downs to generate one up and one down control signal.

When the phase detector is in locked condition the quadrature phases will be aligned with the data edges so D0 & D180 will be the de-multiplexed retimed data. This table illustrates the performance of the phase detector.

<p>| | |</p>
<table>
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</thead>
<tbody>
<tr>
<td><strong>Down 1</strong></td>
<td><strong>90 \rightarrow 360</strong></td>
</tr>
<tr>
<td><strong>Down 2</strong></td>
<td><strong>270 \rightarrow 360+180</strong></td>
</tr>
<tr>
<td><strong>UP 1</strong></td>
<td><strong>180 \rightarrow 360+90</strong></td>
</tr>
<tr>
<td><strong>UP 2</strong></td>
<td><strong>0 \rightarrow 270</strong></td>
</tr>
</tbody>
</table>

Table 2.4.1 Phases of the control signals
The PD has symmetrical architecture so the delay in the signal path is matched so we can compensate this delay by choosing the suitable phase for the multiplexer's clock.

1st block of the PD

1) Slicer

1.1 Concept review:

The slicer is a dynamic latch followed by a simple RS latch, there are many topologies of dynamic latched like strong arm and double tail dynamic comparators.

2) Comparator:

A comparator is a circuit that provides a high Boolean output if the differential input is positive and a low Boolean output if the differential input is negative. High gain amplifiers are often used as comparators since the
outputs of most amplifiers naturally clip at high and low levels when overdriven. If over-driven amplifiers are used for comparators, the power dissipation of these types of comparators is often high.

Some comparators are clocked and only provide an output after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition.

The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Clocked comparators are often called Dynamic Comparators.

Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators.

**Static characteristics of comparators:**

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Figure 2.3.13. As shown in this figure, the output of the comparator is high (VOH) when the difference between the non-inverting and inverting inputs is positive, and low (VOL) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Figure 2.3.14. Comprises a voltage-controlled voltage source (VCVS) whose characteristics are described by the mathematical formulation given on the figure.
The second no ideal effect seen in comparator circuits is input-offset voltage, $V_{os}$. In Figure 2.3.13 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value $+V_{os}$, then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit for a given design. Figure 2.3.14 illustrates offset in the transfer curve for a comparator.
Dynamic characteristics of comparators:

The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator.

Clocked Comparator Model:

While a comparator is by definition a nonlinear circuit element that makes a hard decision on the input signal polarity, almost every clocked comparator does so by sampling the input signal and then regeneratively amplifying it, each of which operation can be treated as that of a linear system. The key difference with traditional linear circuits such as amplifiers is that the comparator may have different linear behaviors at different time points; in other words, it is a linear, but time-varying (LTV) system. While this property precludes the use of the linear time-invariant (LTI) system theory or the traditional small-signal analysis framework for estimating the
noise effects in clocked comparators, we will find that their simple extensions to time-varying systems can provide all the necessary insights to design a good comparator with low random decision error rates.

Fig. 2.3.16 illustrates our assumed model for a clocked comparator. The clocked comparator periodically samples the input voltage $V_{in}(t)$ which is then regeneratively amplified to resolve a digital bit. The sampled and amplified voltage $V_s[n]$ can be expressed as a weighted time-average of the input voltage. The weighting function $ISF(\tau)$ is the impulse sensitivity function (ISF), which describes the sensitivity of the sampled voltage $V_s[n]$ to an impulse arriving at the input at time $nT+\tau$. The final digital output $D_{out}[n]$ can then be determined by the polarity of $V_s[n]$, ignoring hysteresis.

![Figure 2.4.13 clocked comparator model](image)

While the ISF was originally defined for oscillators to analyze the phase noise, the ISF of a clocked comparator can also reveal many of its important characteristics, as illustrated in Figure 2.3.16. For example, the width of the ISF corresponds to the aperture width or the time resolution of the
comparator. The area under the ISF is the DC sampling gain. The center of the ISF is the sampling time. And the sampling bandwidth is found from the Fourier transform of the ISF.

Most comparators are triggered by periodic clocks and therefore can be treated as linear, periodically time-varying (LPTV) systems.

**Circuit Review**

**Conventional strong arm (sense Amplifier)**

Figure 2.4.14 Strong Arm comparator
This circuit was introduced by Kobayashi et al. in 1993. The current flow of the differential input transistors M8 and M9 controls the latch circuit. A small difference between currents through M8 and M9 converts to a large output voltage. Extra switching transistors M10 and M11 are added to increase its characteristics. These circuits are used in sense amplifier based flip-flop, current-sensed SRAM.

**Operation**

During reset phase when clk=0V, the output nodes of the comparator are reset to VDD through the reset transistors M10 and M11. During evaluation phase when clk=VDD, M1 turns ON and the input transistors M2 and M3 starts to discharge Ni node voltages to GND. When any of Ni node voltages falls from VDD to VDD-Vtn, NMOS transistors of the cross coupled inverters turn ON initiating positive feedback. Further when any of out node voltage drops to VDD-Vtp, PMOS transistors of the inverters turns ON and further enhances the positive feedback and converts a small input voltage difference to large full scale output.

**Drawbacks**

1) To increase the drive current of the cross-coupled latch stage, M1 has to be size up. If size of M1 is increased, then the drain currents of both M2 and M3 will be increased during the evaluation phase (clk = VDD). Because of that the Ni nodes of M2, M3 will be discharged from VDD to ground in a very short period because of which the time duration of M2 and M3 being operated in the saturation region decreases. Hence the lower amplification of the input voltage difference will be made.

2) This structure shows very strong dependency on speed with different common mode input voltages.
3) Using this SA in low-voltage deep-sub-micron CMOS technologies is difficult because stack of the four transistors requires large voltage headroom.

**Selected topology**

**Double tail sense amplifier**

![Double tail SA](image)

Figure 2.4.15 Double tail SA

the advantages of this topology is that it has less stacking and the separation of the input tail current and the latch tail current make it easier to lower the delay by widening the upper tail transistor so there'll be fast regeneration, and have less offset voltage by decreasing the input tail transistor size so there's less input tail current for the differential input pair to obtain a long integration time and a better $gm/Id$ ratio for a bigger gain.
**Operation**

The signal behavior of the double-tail SA is also shown in Figure 2.3.18. During the reset phase (Clk = 0V), transistors M7 and M8 pre-charge the Di nodes to VDD, which in turn causes M10 and M11 to discharge the output nodes to ground (so there is no need for dedicated reset transistors at the output nodes). After the reset phase, the tail transistors M9 and M12 turn on (Clk = VDD). At the Di nodes, the common-mode voltage then drops monotonically with a rate defined by \( \frac{I_{M9}}{C_{Di}} \) and on top of this, an input dependent differential voltage \( \Delta V_{Di} \) will build up. The intermediate stage formed by M10 and M11 passes \( \Delta V_{Di} \) to the cross-coupled inverters and also provides additional shielding between the input and output with less kickback noise as a result. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground. The ideal operating point \( (V_{cm}) \) and the timing of the various phases can be tuned with the transistor sizes.

**Sizing considerations:**

1. Large size for M12 for high latch current so less delay.
2. Small size for M9 so we've high \( \frac{gm}{Id} \) so more saturation time so less input offset voltage.
3. High gain of the inverters (\( gm \cdot R > 1 \)).

**2- RS latch:**

The SR latch of the SAFF, shown in Figure 2.3.19, operates as follows: input \( \bar{S} \) is a set input and \( \bar{R} \) is a reset input. The low level at both \( \bar{S} \) and \( \bar{R} \) node is not permitted and that is guaranteed by the SA.
stage. The low level at $\bar{S}$ sets the output $Q$ to high, which in turn forces $\bar{Q}$ to low. Conversely, the low level at $\bar{S}$ sets the $Q$ high, which in turn forces to low $\bar{Q}$. Therefore, one of the output signals will always be delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays. Additionally, the delay of the true output depends on the load on the complementary output, and vice versa. This limits the performance of the SAFF.

![Figure 2.4.16 SAFF](image)

In order to overcome the problem of nonsymmetry of the SR latch in SAFF, we applied modifications to the SL stage. In the following description, $Q$
represents a present, while \( Q^+ \) represents a future state of the SL, i.e., the state after the transition of the clock. The SL modification starts with logic representations for the new output values \( Q^+ \) and \( \overline{Q}^+ \) that are obtained by writing independent logic equations for the and outputs of the cross coupled NAND gate SR latch.

\[ Q^+ = S + \overline{R}.Q \]
\[ Q^+ = R + \overline{S}.\overline{Q} \]

\( Q^+ = S + \overline{R}.Q \) is implemented as an AND-OR structure, where \( S \) is an OR branch of the circuit used to implement this expression. Conversely, the same topology applies the expression for: \( Q^+ = R + \overline{S}.\overline{Q} \) In this topology signal \( R \) is a parallel branch. The reason for choosing those expressions in implementing SL stage is to reduce the number of p-type series transistors in the branch responsible for the transition to one. This will be fully understood only when we analyze the entire SL stage resulting from these modifications.
Figure 2.4.17 The improved RS – latch
2.4.2 **Final Design achieved**

**Double tail comparator**

**Schematic**

![Schematic of double tail comparator](image)

Figure 2.4.18 Schematic of double tail comparator
Results

Transient output

Figure 2.4.19 transient output of Double tail comparator

RS latch

1st topology schematic

Figure 2.4.20 NAND gate based RS latch
2nd topology schematic

Figure 2.4.21 modified RS latch
The whole slicer

Schematic

Figure 2.4.22 The slicer schematic
### Sizing

Table 2.4.2

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<td>M19</td>
<td>200/60n</td>
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<td>M18</td>
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<tr>
<td>M14</td>
<td>200/60n</td>
<td>M15</td>
<td>468/60n</td>
</tr>
</tbody>
</table>
1) Transient simulation:

\[ V_{inpp} = 50 \text{ mV} \]

Delay = 40.775 psec

Power consumption = 84.8 uw

Figure 2.4.23 Transient Simulation result of the slicer

Sweeping \( \Delta V_{in} \) for the same \( \text{vdd} = 1\text{v} \)

Figure 2.4.24 delay for different common mode voltage
Delay for different vdd

![Delay vs Vin for diff vdd & Vcm](image)

Figure 2.4.25 Delay vs Vin for diff vdd & Vcm

2- XOR gate:

CMOS logic is used and not CML logic because of its low power consumption.

At 1st I tried to use CMOS static logic, but they didn't support the speed of 5GHz, so I used dynamic XOR gate.

The only disadvantages of using dynamic XOR gate in my topology is that I had to delay the clock to be synchronized with the XOR output at multiplexing.

I delayed the clock using the same XOR gate to guarantee the synchronization between the up and down signals and the clock across PVT variations.
XOR schematic:

The 1st topology (static CMOS)

Figure 2.4.26 Static XOR gate

The 2nd topology (Transmission gate XOR)

Figure 2.4.27 TG based XOR gate
Selected topology (dynamic XOR)

Sizing

All the transistors has minimum sizing to support the high switching speed.

3- Multiplexer:

The mux I have in this PD topology is a level triggered mux that works according to table 7.2.2.1 mentioned before
Schematic of the mux in the PD:

Figure 2.4.29 Schematic of the clocked inverter MUX
Operation

When clk = 0 & clkn = 1, D1 passes through the down inverter and the upper inverter is off.

When clk = 1 & clkn = 0, the upper inverter is on and the lower one is off, and D0 passes to the output.

Sizing

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<table>
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<tbody>
<tr>
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<td>200/60n</td>
</tr>
<tr>
<td>PMOS</td>
<td>268/60n</td>
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</table>

The total PD schematic:

![Figure 2.4.30 Total PD schematic](image-url)
Simulation Results of the PD

Total power of PD = 604.159 uw.

The clock is late by 30 psec:

The clock is late so we expect that only DN signal that will be out.

1- Output of the slicer:

![Figure 2.4.31 transient output of the slicer](image)

3- Output of the MUX:

![Figure 2.4.32 Transient output of MUX](image)
2.5 **Charge Pump (CP)**

2.5.1 **Concept Review**

Charge pump converts the digital data from the PD that represents the phase difference between the clock and data into analog current through digital controlled switches. Charge pump must be carefully designed to minimize feedthrough and phase noise. In spite of numerous variations a charge pump will usually consist of two current sources and two switches.

It places charge in or take it out of the filter and moving the control signal on the phase interpolator up or down.

![Simple CP Diagram](image)

*Figure 2.5.1 Simple CP*

\[ Q_{cp} = I_{up} \times t_{up} - I_{down} \times t_{down} \]

Ideally, \( I_{up} = I_{down} \), but practically they're not equal because of the mismatches in the current sources and the rise and fall time of the up and down signals.
Difference between single ended and differential charge pump:

1- Single ended

**Operation**

M3, M4 are current sources that work in the saturation region, and M1, M2 act like switches that are controlled with the PD.

When M1 is on, the capacitor starts charging through M3 and when M2 is on, the capacitor discharges through M4.

In this topology, the control signal must be full rail to rail signal.

**Advantages**

1) Simple to implement
2) Low power and Area

**Disadvantages**

1) High phase noise.
2) Current mismatches which lower the compliance range.
2-Differential charge pump

![Figure 2.5.3 Simple differential cp](image)

**Operation**

In this circuit, it is assumed that the current sources M5, M6, and M8, M9 are matched. When UP and DN are both low, the switches M1 and M4 are closed, and the current sourced from M9 is all sunk by M5; likewise, all current sourced by M8 is sunk by M6, and no current passes into or out of the loop filter (not shown, but connected between the output nodes). Now suppose that UP becomes active. In this case, M1 is open, and M2 is closed. Now the current from both M9 and M8 passes down the right-hand side of the circuit. Since M6 can only sink half this current, the other half must pass through the loop filter and be sunk by M5. In this case, a current is passed differentially through the loop filter, and a differential voltage is developed across it. A similar, but opposite, situation occurs when a down pulse is present.

Although this circuit seems like the cml circuit, it requires rail to rail input to work properly.
Advantages

1) Mismatches between NMOS transistors and PMOS transistors does not affect the overall performance
2) Use NMOS switches only or PMOS only
3) \( UP & DN \) do not generate any offset due to its symmetrical operation.
4) Required to Match NMOS only or PMOS only
5) Doubles the range of the output voltage compliance.
6) Output is less sensitive to the leakage current since it acts as a common-mode offset.
7) Better immunity to the supply, ground and the substrate noise.

Disadvantages

1) Need of common-mode feedback circuitry
2) More power dissipation due to the constant current biasing

Selected topology

Since the open loop transfer function of the CDR loop is of first order, so there's no need for stabilizing zero, thus the loop filter can be realized by a charge pump with a single capacitor.

I used a conventional differential cp like the one I explained earlier, but I put only 2 control signals not 4 as the PD generated only the up and dawn signals, I needed to bias the output nodes using two constant pmos current sources and two adjustable nmos current sources. The currents of the nmos sources are controlled by a common mode feedback loop.

When the PD generates no pulses the charge pump capacitances are discharged by the impedance of the current sources and by the current
sources mismatches, the former cause can be minimized by the use of cascade current sources, to reduce both effects large dimensions where used to the bias current sources transistors. Then I realized that at some cases the output node become floating and damage the value of the output common mode so I used 4 control signals ($U_P, \bar{U_P}, D_N, \bar{D_N}$) and it worked.

**The charge pump circuit**

![Charge Pump Circuit](image)

Figure 2.5.4 CP Schematic

**Sizing of the CP**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>76.6/2u</td>
</tr>
<tr>
<td>M1</td>
<td>31.8/2u</td>
</tr>
<tr>
<td>M2</td>
<td>31.8/2u</td>
</tr>
<tr>
<td>M3</td>
<td>20u/60n</td>
</tr>
<tr>
<td>M4</td>
<td>20u/60n</td>
</tr>
</tbody>
</table>
### The bias circuit

![Bias Circuit Diagram](image1)

Figure 2.5.5 Current source biasing schematic

### Common mode feedback circuit

![CMFB Diagram](image2)

Figure 2.3. 3: Common mode feedback schematic
Sizing of bias circuit

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>19.4 u/60n</td>
</tr>
<tr>
<td>M1,2,3</td>
<td>2.4 u/60n</td>
</tr>
<tr>
<td>M4,5</td>
<td>800/200n</td>
</tr>
<tr>
<td>M6,7</td>
<td>3.4u/720n</td>
</tr>
<tr>
<td>M8,9</td>
<td>5.64u/720n</td>
</tr>
<tr>
<td>M10,11</td>
<td>1.2u/720n</td>
</tr>
<tr>
<td>M12,13</td>
<td>1u/720n</td>
</tr>
</tbody>
</table>

Output of the cp

![Figure 2.5.6 Transient output of CP](image)

126
Step size of the control voltage = 0.2896 mv

\[ \Delta v = \frac{\Delta t \times I}{C} = \frac{85.851 \text{psec} \times 50.6 \mu A}{15 \text{pF}} = 0.2869 \text{mv} \]

This is equivalent to 0.17 degree

So the PI resolution become 531 point per quad

Power consumption = 1.4 m

**Voltage Compliance range**

It's the range of the output common mode voltage that the output current equal zero (no mismatches). It define the efficiency of the charge pump.

\[ V_{ctrl}(\text{max}) = V_{DD} - V_{od3} - V_{s1} \]

\[ V_{ctrl}(\text{min}) = V_{od4} + V_{s2} \]

\[ V_{comp} = V_{DD} - V_{od3} - V_{od4} - V_{s1} - V_{s2} \]

To ensure a large compliance range we need to minimize the overdrive voltages of the current sources, increase the widths of the current sources and decrease the current.

At first the compliance range was small because of mismatches in the current sources so I used larger dimensions. The compliance range of the charge pump itself without the biasing were from 118.5 mv to 791.2 mv
After adding the bias current sources as they are cascaded the range decreased to from 271.1mv to 573m

As the PI works from 300 mv to 500 mv, the range was accepted.
The switching

I needed also to make some kind of switching between the up and down signals using a control signal coming from the phase interpolator.

If $B_2 = 1$, the up and down signal remain the same.

If $B_2 = 0$, the up and down signals are reversed.

I've done that using clocked inverters like the mux used in the PD.

Figure 2.5.9 Switching circuit in CP
2.6 **Analog Phase Interpolator (PI)**

2.6.1 **Introduction**

With the growing amount of data communication between signal processing chips building a conventional PLL-based CDRs is not recommended. The required VCO could couple both through substrate and by electromagnetic fields, if an LC VCO. Thus, the architecture would suffer from inter-channel crosstalk problems. Delay-Locked loop (DLL) can also be used for data and global clock dynamically alignment. Since the frequencies of the receiver and the transmitter system clock can be slightly different, the DLL has to shift the phase over an unlimited phase range. The phase limitation of voltage-controlled delay elements (VCDL) can be avoided by use of phase interpolation. The main issue here is to develop a suitable controller for the phase interpolator (PI). The limited resolution of digitally controlled PIs degrades the jitter performance of the CDR, and also suffers from speed limitations. To overcome this, trade-offs regarding the speed of the distributed clock has to be made. With decreasing clock frequency, the required number of distributed clock phases rises. This increases the complexity and power dissipation of the clock distribution network, which is affected when the number of channels is high.

2.6.2 **Purposed Architecture**

To overcome these drawbacks of the digitally controlled PIs we developed an analog PI controller. Thus, no speed limitation is set by the PI controller and the required clock phases are minimized to four, which is called quadrature phase interpolation.
2.6.2.1 Phase Interpolator Core

Quadrature phase mixing was applied to minimize the required global clock phases. Thereby, the phase interpolation can be expressed as a weighted summation of the two quadrature clock signals $V_{CLK,1}$ and $V_{CLK,Q}$:

$$V_{out} = a_1 V_{CLK,1} + a_2 V_{CLK,Q}$$ (1)

The summation is performed in the PI core, shown in Fig.2.6.1. The output currents of differential stages are summed up on the same load resistor pair. The weighting factors are realized by adjustable current sources.

To obtain a phase from 0° to 360°, the weighting factors $a_1$ and $a_2$ have to assume positive and negative values, this can be accomplished by switching the polarity of the input clock phases in the incoming signal path. However, this approach is unfavorable, because switching in the signal path is likely to introduce jitter on the output signal. To avoid switches in the high frequency path, in this design four instead of two differential stages were used for the summation. As can be seen in the schematic of Fig4.1, the output currents of the first and the second, and those of the third and the fourth stage, respectively, counteract each other. Thus, $a_1$ depends on $I_1 - I_2$ and $a_2$ on $I_3 - I_4$. While this architecture avoids switching in the signal path, it suffers from an increased capacitive load at the output node. However, this is less harmful than an increased jitter.
As stated in Phase detector needs two orthogonal clocks. These clocks can be generated by using two identical PIs with changed weighting factors. To get a signal $V_{\text{out,90}}$ with a 90° shifted output phase $a_{1,90}$ has to be equal to $a_2$ and $a_{2,90}$ to $-a_1$. We can assume the differential input is sinusoidal.

$V_{\text{clk}_1} = \sin(\omega t)$ & $V_{\text{clk}_Q} = \cos(\omega t)$

For Sinusoidal weighting factors:

$V_{\text{out}_o} = \cos(\omega t_o) \sin(\omega t) + \cos(\omega t) \sin(\omega t_o)$

$= \sin(\omega t + \omega t_o) = a_{1o} \sin(\omega t) + a_{2o} \cos(\omega t)$

$a_{1o} = \cos(\omega t_o)$ & $a_{2o} = \sin(\omega t_o)$

$V_{\text{out}_{90}} = -\cos(\omega t + \omega t_o)$

$= -\cos(\omega t_o) \cos(\omega t) + \sin(\omega t_o) \sin(\omega t)$

$= -\cos(\omega t_o) V_{\text{clk}_Q} + \sin(\omega t_o) V_{\text{clk}_I}$

$a_{1_{90}} = -\cos(\omega t_o) = -a_{1o}$
This can be easily implemented by interchanging the input clock to the PI core as shown in Fig. 2.6.2

\[ a_{290} = \sin(\omega t_0) = a_{20} \]

\[ V_{\text{out},90} = a_2 V_{\text{CLKI}} - a_1 V_{\text{CLKQ}} \] (2)

Figure 2.6.2 Simplified Schematic of PI Core for orthogonal clock generation

**2.6.2.2 Phase Interpolator Controller**

**Interpolation concept**

The Analog PI-Controller has the task to derive the four required steering currents from only one control signal which is provided by the phase detector. However, digital phase interpolators suffer from a limited phase resolution, which can only be increased at the cost of a higher complexity. Thus, quantization jitter is applied to the recovered clock. Also, the required logic gates are speed limited and thus have difficulties to handle the PD output pulses, which has a pulse width only of 86ps in the used CDR-architecture. Because of these drawbacks, an analog solution for the controller was developed.
Considering an ideal PI with constant output amplitude, the weighting factors from (1) must fulfill the equation

\[ a_1^2 + a_2^2 = \text{const.} \quad (3) \]

Leading to a circle in the diagram of Fig. 2.6.3(a), where \( a_1 \) is shown versus \( a_2 \).

Ideally, the change of the PI output phase \( \phi \) is proportional to the change of the charge pump control voltage \( V_{\text{ctl}} \). This means a constant gain

\[ K_{\phi_{\text{pi}}} = \frac{d\phi_{\text{out}}}{dV_{\text{ctrl}_{\text{CP}}}} \]

To achieve this, \( a_1 \) and \( a_2 \) must be sinusoidal functions of \( \phi \), as is displayed in Fig.2.6.3(b). To simplify the derivation of the weighting factors, the sinusoidal functions are approximated by triangular ones. Thus, both \( K_{\phi} \) and the amplitude of \( V_{\text{out}} \) vary by a factor of 2 maximum over the whole phase range for the reason shown in Fig.2.6.3 (a) and Fig.2.6.4 (b).
Figure 2.6.3 weighting factor $a_2$ and $a_1$ for an ideal PI (dashed lines) and the triangular approximation (solid lines) (a) is the phasor diagram, while (b) shows $a_1$ and $a_2$ versus phase $\varphi$.

Figure 2.6.4 the maximum variation in both $K_{\varphi}$ and the amplitude of $V_{\text{out}}$ by factor 2 over the whole phase range at phase $45^\circ$.

However the amplitude variation is not crucial, because only the zero-crossing of the clock is of importance for sampling the data. Also, some of the amplitude variation is filtered by the clock buffer between the PI and the phase detector.
Weighting factors \( (a_1 \text{ and } a_2) \) generation

The task for the PI controller is to derive these two monotonic functions \( a_1 \) and \( a_2 \) from only one control information, which is provided by the phase detector.

However, the control mechanism used four active current sources are used for \( a_1 \) and \( a_2 \) generation purpose. A robust symmetrical architecture for the controller is used by assuming the four controlling currents are the components of two differential currents. Then they fulfill the equations

\[
I_1 + I_2 = I_0 \quad (3)
\]

\[
I_3 + I_4 = I_0 \quad (4)
\]

Figure 4.1 shows mixing done at the differential pairs summing nodes between steering current \( I_1 \) and \( I_2 \) for the branch carrying positive In phase component (0°) and negative Quadrature component (270°), similarly for the branch carrying negative In phase component (180°) and positive Quadrature component (90°). Similarly for the steering currents \( I_3 \) and \( I_4 \), this mixing is equivalent to

\[
a_1 \equiv I_1 - I_2 \quad (5)
\]

\[
a_2 \equiv I_3 - I_4 \quad (6)
\]

Thus Fig.2.6.4(b) can be deduced from the relations (5) and (6).
Figure 2.6.5 Idealized controlling currents $I_1, I_2, I_3$ and $I_4$ versus phase $\varphi$

Fig.2.6.5 shows the required curves of the controlling currents to get the aimed triangular curves for the weighting factors $a_1$ and $a_2$. Since only one differential current can be derived directly from the charge pump, $I_3$ and $I_4$ have to be deduced from $I_1$ and $I_2$. From Fig.4.5 it can be seen that the sum of the smaller two currents always $0.5 I_0$. It depends on the value of $\varphi$ which currents are the lowest ones.

Comparing $I_1$ with $I_2$, and $I_3$ with $I_4$, respectively, the instant quadrant can be detected. The result of this comparison are the binary signals $B_1$ and $B_2$. With these signals the found relationship can be expressed as

$$ (B_{1\text{bar}} \cdot I_1 + B_1 \cdot I_2) + (B_{2\text{bar}} \cdot I_3 + B_2 \cdot I_4) = 0.5I_0 \quad (7) $$

Table 2.6.1 Binary control signals $B_1$ and $B_2$ values across the whole phase range

<table>
<thead>
<tr>
<th>Quadrant</th>
<th>$B_1 \ B_2$</th>
<th>Smallest currents</th>
<th>Relation</th>
</tr>
</thead>
</table>
| 1<sup>st</sup> | 1 1 | $I_2$  $I_4$ | $B_1 \cdot I_2 + B_2 \cdot I_4$  
\[= 0.5 \cdot I_0 \] |
If the controller would be implemented with the ideal relationships for the steering currents derived above, it would be sensitive to mismatches of the three constant current sources, which are required for the right side of the equations. A kind of latch-up problem can occur at quadrant boundary crossing of multiples of 180°. For example, let us assume that the momentary phase is below 180° in the second quadrant, \( I_1 \) must be decreased, \( I_4 \) is simultaneously increased, because \( B_1 \) is on a low and \( B_2 \) is on a high level and (7) can be simplified to \( I_1 + I_4 = 0.5 - I_0 \) for this quadrant. The boundary at \( \varphi = 180° \) is determined by the equality of \( I_3 \) and \( I_4 \), \( I_3 = I_4 = 0.5I_0 \), according to (7) \( I_1 \) must be 0 to reach this state. If now the current on the right side of (7) is a little bit decreased by mismatches in the transistor level implementation, \( I_1 \) has to be negative value. This is not possible in the transistor level implementation. Therefore, \( I_1 \) would stop to decrease at a value of 0, and equality of \( I_3 \) and \( I_4 \) could not be obtained. This would finally lead to an inability of crossing the quadrant boundary.

To alleviate the mismatch requirements for the currents sources (7) is changed to

<table>
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<tbody>
<tr>
<td>01</td>
<td>( I_1 )</td>
<td>( I_4 )</td>
<td>( B_{1bar}.I_1 + B_{2}.I_4 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>= 0.5( .I_0 )</td>
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</tbody>
</table>

<table>
<thead>
<tr>
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<th>3(^{rd})</th>
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</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>( I_1 )</td>
<td>( I_3 )</td>
<td>( B_{1bar}.I_1 + B_{2bar}.I_3 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>= 0.5( .I_0 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th>4(^{th})</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>( I_2 )</td>
<td>( I_3 )</td>
<td>( B_1.I_2 + B_{2bar}.I_3 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>= 0.5( .I_0 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
\( (B_{1\text{bar}}.I_1 + B_{1}.I_2) + (B_{2\text{bar}}.I_3 + B_{2}.I_4) = 0.6I_o \) (8)

Fig.2.6.6 shows the effect of this modification on the diagram of the controlling currents. The curves shrunk around the average value of 0.5I_o, which causes a decline of the amplitude of the weighting factors (see Fig.2.6.7). However, the ratio of the maximum of \(a_1\) and \(a_2\) is not changed by this modification and remains 1. This, the aspect ratio of the rhombic in the phasor diagram of Fig.2.6.7 (a) is not changed by this modification and the nonlinearity of the Pi is not further increased. However, although the increased current has no effect on the PI nonlinearity, it decreases the amplitude of the PI output. Therefore a value of 0.6 I_o was chosen to have enough margin for mismatches on the one hand and not to reduce the PI output amplitude unnecessarily on the other hand.

Figure 2.6.6 Shrunken controlling currents I_1, I_2, I_3 & I_4 versus phase \(\phi\) for higher robustness against mismatch.
The implementation of the PI controller on the transistor level is shown in Fig. 2.6.8. The controller is fed by the currents $I_{1,in}$ and $I_{2,in}$. These currents are provided by a differential amplifier which converts the charge pump voltage into a differential current shown in Fig. 4.8. The input currents steer two current mirror banks. A resistor pair uses two mirror currents of $I_1$ and $I_2$ to generate differential voltage $V_{B1}$. A comparator, which is not shown in the schematic, evaluates the present value of $B_1$ from the sign of $V_{B1}$. Depending on the state of $B_1$, either $I_1$ or $I_2$ is fed to the upper encircled circuit node. At this node (8) is realized. To ease the understanding of the controller, let us assume that $B_1$ and $B_2$ are both on a high level. Then, the current mirror bank of $I_2$ acts as a current source to the upper encircled node. The current mirror bank of $I_4$ on the other hand is diode-connected to that node. Thus, the current $I_4$ is forced to be the difference between the constant current $0.5I_0$ from the current source and the control current $I_2$. Finally, $I_3$ is derived from $I_4$ at the lower encircled node. Again, one current mirror acts as a current source, while the other one is diode-connected.

Figure 2.6.7 Effect of modified controlling currents on the weighting factors. The dashed line shows the weighting factors before shrinking.
In Fig.2.6.6 it can be observed that $\frac{dI_1}{d\varphi}$ and $\frac{dI_2}{d\varphi}$ have to change their sign, when $\varphi$ reaches a multiple of 180°. To this end, a switch was applied between the PD and the charge pump as shown in Fig.4.10. Thus, the control signal $B_2$ can interchange the impacts of the up and down pulses on the charge pump voltage and in that way alternate the signs of $\frac{dI_1}{d\varphi}$ and $\frac{dI_2}{d\varphi}$.

The comparators which detect the signs of $V_{B_1}$ and $V_{B_2}$ are realized with Schmitt trigger circuits. The Schmitt trigger prevents the control signals $B_1$ and $B_2$ from acquiring an undefined state between high and low. Another beneficial property of the Schmitt trigger is its inherent hysteresis. Without the hysteresis the controller would permanently switch between two adjacent quadrants in the presence of some high frequency jitter, if the phase vector $\varphi$ is close to a quadrant-boundary. Fig.2.6.9 shows the single ended simple...
Schmitt trigger circuit used to generate the Quadrant controlling signals \( B_1 \) and \( B_2 \).

![Schmitt trigger circuit](image)

**Figure 2.6.9 Simple Schmitt trigger comparator**

### 2.6.2.3 PI in the System Architecture

Fig.2.6.10 shows Voltage-to-current converter, that converts the voltage resulted from the charge pump as a phase difference indication to two main steering currents \( I_1 \) and \( I_2 \). Figure also shows two PI cores one for differential 0° clock generation and the other one for differential 90° clock generation. Both cores are feed by the steering currents generated by the VI Converter. The PI controller also is fed by \( I_1 \) and \( I_2 \) to generate the rest of the steering currents \( I_3 \) and \( I_4 \) (by the technique discussed in section 4.2.2.2) and feed them to both cores. Certain Currents value will indicate certain phase difference and interpolating them will result the required phase shifted clocks \( 0^+, 0^-, 90^+, \) and \( 90^- \). A CML to CMOS stage is used in the Feedback path, to convert the small swing clock signals generated by the Phase Interpolator into rail to rail clocks for the phase detector.
2.6.3 Circuit Design

Analog Phase Interpolator Circuits discussed above are implemented with parameter \( I_0 = 110 \mu m \) to provide minimum power consumption and suitable currents ranges against mismatches.

2.6.3.1 PI Core

Fig. 2.6.11 and Fig. 2.6.12 shows the 2 PI cores Schematics used for 0°, 180° and 90°, 270° differential clocks respectively. Steering currents mixing is done in both structures to generate the required phase as discussed before. Transistors Q9 & Q21 are the variable current source \( I_1 \), Transistors Q10 & Q22 are the variable current source \( I_2 \), both derived by the Voltage-to-current converter circuit as will be discussed in next section.
Figure 2.6.11 0° & 180° differential clocks PI Core Schematic

Figure 2.6.12 90° & 270° differential clocks PI Core Schematic
Transistors Q11& Q23 are the variable current source $I_3$, Transistors Q12 & Q24 are the variable current source $I_4$, both derived by the PI-Controller as previously discussed.

**Design Challenges**

Each Diff pair in the core shown in Fig.2.6.11 and Fig.2.6.12 are biased using variable current sources, with a fixed gate voltage transistors and fixed sizing, their source node suffers from Voltage variations across the current Range from 11 $\mu$A to 99 $\mu$A. Thus these transistors sizing must guarantee that $V_{ds}$ of the current source greater than $V_{od}$ to keep them in Saturation region of operation.

From Table 2.6.2, notices that Current sources transistors have larger length to provide immunity against secondary effects due to short channels.

Table 2.6.2 PI Core Transistors Sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
<th>No. of Fingers</th>
<th>Total Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q1-8 and Q13-20</td>
<td>60 nm</td>
<td>440 nm</td>
<td>2</td>
<td>880 nm</td>
</tr>
<tr>
<td>Q9-10 and Q21-22</td>
<td>120 nm</td>
<td>660 nm</td>
<td>1</td>
<td>660 nm</td>
</tr>
<tr>
<td>Q11-12 and Q23-24</td>
<td>240 nm</td>
<td>570 nm</td>
<td>2</td>
<td>1.14 $\mu$m</td>
</tr>
</tbody>
</table>
Table 2.6.3 PI Core Passives values

<table>
<thead>
<tr>
<th>Passives</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1-2 and R3-4</td>
<td>Resistors</td>
<td>1.35984 kΩ</td>
</tr>
</tbody>
</table>

Table 2.6.4 PI Core Input Specs

<table>
<thead>
<tr>
<th>Input Ports</th>
<th>Common Mode</th>
<th>Voltage Swing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clk0, Clk180, Clk90 and Clk270</td>
<td>800 mV</td>
<td>400 mVpp</td>
</tr>
</tbody>
</table>

Table 2.6.5 PI Core output Specs

<table>
<thead>
<tr>
<th>Output Ports</th>
<th>Common Mode</th>
<th>Max-Voltage Swing</th>
<th>Min-Voltage Swing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vclk0+, Vclk0-, Vclk90+, and Vclk90-</td>
<td>850 mV</td>
<td>300 mVpp</td>
<td>140 mVpp</td>
</tr>
</tbody>
</table>

2.6.3.1 Voltage-to-Current Converter

Fig.2.6.13 shows Voltage to current converter schematic that is used to convert the variable common mode voltage (from the charge pump) on its input PMOS transistors Q26 and Q27 into different steering currents ratios in both branches, that are mirrored through V1 and V2 nodes to the PI Core I₁ and I₂ current sources.
Design Challenges

Transistor Q25 is assumed with $V_{ds} = 200\text{mV}$, then its drain = 800mV, this value with the variable input common mode on both transistor Q26 and Q27 from 300mV to 500mV must be greater than $V_{th}$ which suffers large variations in 65nm technology. At the same time Nodes V1 and V2 are the gate voltages of the $I_1$ and $I_2$ current sources in the PI Core, thus they must be also larger than $V_{th}$ to maintain the operating Region and also be sufficient for providing the current range from 11uA to 99uA required.

Notice that current sources transistors and diode connected are larger in length to maintain more stable current source and fewer mismatches during current mirroring.
2.6.3.2 PI Controller

Fig. 2.6.14 shows the simplified PI Controller Schematic without the comparators. Circuit operation was previously discussed. Input Nodes V1 and V2 are output voltages from the V-to-I converter whose values are indication from currents $I_1$ and $I_2$. Output ports $I_3$ and $I_4$ are fed to the current sources gate voltage to steer both currents in the PI Core, after being
generated in the controller based on $I_1$ and $I_2$ values and the Quadrants indicators $B_1$, $B_1\bar{\text{bar}}$, $B_2$ and $B_2\bar{\text{bar}}$.

Figure 2.6.14 Simplified PI Controller Schematic

**Design Challenges**

Transistors Q45, Q49, Q50, Q51, Q52, Q53, Q54, Q55 and Q56 are switching transistors with large sizing as shown in Table 2.6.9, so that they have the less possible on resistance, allowing all the current to pass through it.

The main design challenge was to provide a suitable current ratios in the branches against mismatches, thus a closer $I_3$ and $I_4$ range to $I_1$ and $I_2$. 
### Table 2.6.9 PI Controller Transistors sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
<th>No. of fingers</th>
<th>Total Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q30, Q32, Q35, Q36, Q40, Q41, Q42 and Q43</td>
<td>60 nm</td>
<td>2.66 μm</td>
<td>20</td>
<td>53.2 μm</td>
</tr>
<tr>
<td>Q31 and Q33</td>
<td>120 nm</td>
<td>530 nm</td>
<td>1</td>
<td>530 nm</td>
</tr>
<tr>
<td>Q34</td>
<td>240 nm</td>
<td>430 nm</td>
<td>8</td>
<td>3.44 μm</td>
</tr>
<tr>
<td>Q39</td>
<td>240 nm</td>
<td>720 nm</td>
<td>8</td>
<td>5.76 μm</td>
</tr>
<tr>
<td>Q37 and Q38</td>
<td>120 nm</td>
<td>690 nm</td>
<td>1</td>
<td>690 nm</td>
</tr>
<tr>
<td>Q44 and Q45</td>
<td>120 nm</td>
<td>610 nm</td>
<td>1</td>
<td>610 nm</td>
</tr>
</tbody>
</table>

#### 2.6.3.3 Schmitt trigger Comparator

2 Schmitt trigger circuits are used in the generation of both $B_1$ and $B_2$. Both the same structure shown in Fig.2.6.17 but with different sizing depending on the Reference level in each case. Since a simple Schmitt trigger circuit is used which is a single ended one. Also $B_2$ can’t be generated with a simple Schmitt trigger if it is the result of comparing $I_3$ and $I_4$, since $I_3$ and $I_4$ are generated based on $B_2$ value to open the suitable branch as shown in Fig.4.14.

Thus only $I_1$ value is compared with a reference value, instead of comparing based on the difference between the currents to generate both $B_1$ and $B_2$. 
A Common Source stage is used to step up the variations on the Q47 gate to the range that guarantees proper hysteresis operation. Schmitt trigger is followed by 2 stages of inverters to generate \( B_{1\, \text{bar}} \) and \( B_{2\, \text{bar}} \), and let \( B_1 \) and \( B_2 \) have sharper values than the waveform generated directly from Schmitt trigger suffering \( \Delta V \) variation during switching.

**B1 and B1-bar Generation (B1-bar \( (P_1) \) and B1 \( (P_2) \))**

In the first Quadrant shown in Fig.2.6.15, as \( I_1 \) decreases gradually from 99 \( \mu A \) to 11\( \mu A \), Schmitt trigger input voltage will gradually rise until exceeding \( VR_1 \) leading to output switching from High to Low.

This Schmitt trigger circuit is implemented with zero hysteresis length since switching from high to low and from low to high will occur at the same voltage level, thus \( VR_1 = VR_2 \).

![Figure 2.6.15 B1 Generation](image)

**B2 and B2-bar Generation (B2-bar \( (P_1) \) and B2 \( (P_2) \))**

Similarly \( I_1 \) decreases gradually during the first 2 Quadrants as shown in Fig.2.6.16 leading to gradual rise in the voltage after the CS stage at the
Schmitt trigger’s input, until exceeding a certain reference $VR_3$ when $B_2$ drops from high to low. Then it gradually fall due to $I_1$ rise in both the 3rd and the 4th Quadrants, until being below the second reference $VR_4$, when $B_2$ rises from low to high.

![Figure 2.6.16 B2 Generation](image1)

![Figure 2.6.17 Controlling Signals (B1, B2, B1 bar & B2 bar) generation Schematic](image2)
Table 2.6.10 B1 Generation Schmitt Trigger transistors Sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
<th>No. of fingers</th>
<th>Total Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q46</td>
<td>60 nm</td>
<td>600 nm</td>
<td>1</td>
<td>600 nm</td>
</tr>
<tr>
<td>Q47</td>
<td>60 nm</td>
<td>200 nm</td>
<td>1</td>
<td>200 nm</td>
</tr>
<tr>
<td>Q50</td>
<td>60 nm</td>
<td>3 µm</td>
<td>2</td>
<td>6 µm</td>
</tr>
<tr>
<td>Q46,Q49,Q50,Q51,Q52</td>
<td>60 nm</td>
<td>200 nm</td>
<td>1</td>
<td>200 nm</td>
</tr>
<tr>
<td>,Q53,Q54,Q55 and</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q56</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.6.11 B1 Generation Schmitt Trigger Reference levels values

<table>
<thead>
<tr>
<th>Reference Level</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VR₁ and VR₂</td>
<td>464.15 mV</td>
</tr>
</tbody>
</table>

Table 2.6.12 B2 Generation Schmitt Trigger transistors Sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
<th>No. of fingers</th>
<th>Total Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q46</td>
<td>60 nm</td>
<td>790 nm</td>
<td>2</td>
<td>1.58 µm</td>
</tr>
<tr>
<td>Q47</td>
<td>60 nm</td>
<td>200 nm</td>
<td>1</td>
<td>200 nm</td>
</tr>
<tr>
<td>Q48</td>
<td>60 nm</td>
<td>3.68 µm</td>
<td>2</td>
<td>7.36 µm</td>
</tr>
<tr>
<td>Q45, Q49, Q51, Q52, Q53, Q54, Q55, and Q56</td>
<td>60 nm</td>
<td>200 nm</td>
<td>1</td>
<td>200 nm</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>-------</td>
<td>--------</td>
<td>-----</td>
<td>--------</td>
</tr>
<tr>
<td>Q48</td>
<td>60 nm</td>
<td>3 μm</td>
<td>2</td>
<td>6 μm</td>
</tr>
</tbody>
</table>

Table 2.6.13 B2 Generation Schmitt Trigger Reference Levels values

<table>
<thead>
<tr>
<th>Reference Level</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$VR_3$</td>
<td>626.24 mV</td>
</tr>
<tr>
<td>$VR_4$</td>
<td>507.79 mV</td>
</tr>
</tbody>
</table>

2.6.4 Measurements and Results

Fig.2.6.18 and Fig.2.6.19 shows respectively the variations on the input common mode voltage coming from the $C_p$ between 300mV and 500mV, then the variations on the VI converter output voltage node ($V_1$, $V_2$) and the steered currents $I_1$ and $I_2$ as a result of the mirroring.
Figure 2.6.18 $I_1$ generation

Figure 2.6.19 $I_2$ generation

Figure 2.6.20 $I_1$ and $I_2$
Figure 2.6.21 shows the variations of $B_1$ and $B_2$ across Quadrants as a result of using Schmitt trigger comparator circuit, to control Quadrants transitions based on a certain reference level comparison.

Figure 2.6.21 B1 and B2

Fig.2.6.22 shows the generated main steering currents by the V-to-I converter and the PI controller.

Notice that the switching behavior on the currents in the PI controller will let both $I_3$ and $I_4$ suffer from spikes at each boundary crossing as shown in figure.
During the Quadrant-boundary crossing, several MOSFETs of the PI Controller are switched by either $B_1$ or $B_2$. This switching activity produces spikes on the gate voltages of the current mirror banks and thus on the controlling currents. However, the current mirror bank transistors have large channel lengths because of mismatch concerns. Thus, the gate capacitance of the current mirrors is large compared to the parasitic coupling capacitance.

A special problem occurs at the transistors Q31 and Q33 in Fig.2.4.67 For example, if $B_1$ is high, then Q33 operated partly in the triode region during switching. Thus, its gate-drain capacitance $C_{GD}$ is 0.5 times the gate oxide capacitance. Because of large transistors dimensions the discharging of thus capacitance would cause spikes. To alleviate this problem the drain voltage
of Q33 is clamped when $B_1$ is high, using a diode connected transistor with the same dimensions. Of Course, the same principle was used for Q31.

![Figure 2.6.23 Clamping Circuits](image)

Table 2.6.14 Clamping circuits transistors sizing

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
<th>No. of Fingers</th>
<th>Total Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q58 and Q61</td>
<td>120 nm</td>
<td>690 nm</td>
<td>1</td>
<td>690 nm</td>
</tr>
<tr>
<td>Q57 and Q60</td>
<td>240 nm</td>
<td>430 nm</td>
<td>8</td>
<td>3.44 μm</td>
</tr>
<tr>
<td>Q59 and Q62</td>
<td>60 nm</td>
<td>1 μm</td>
<td>20</td>
<td>20 μm</td>
</tr>
</tbody>
</table>
Figure 2.6.24 All steering currents after spikes removal

Figure 2.6.25 Output phases across input voltage variation

$$K_{PI} = 0.5851^\circ / \text{mV}$$
2.7 CDR Loop Simulation

2.7.1 Loop schematics

We notice that the control voltage began varying then it settled into a constant value when the loop reached the locked state.

Figure 2.7.1 CDR Schematic

\[ V_{\text{control}} (V_1, V_2) \]

Figure 2.7.1 Control voltage
Phase Interpolator currents

Notice that Phase Interpolator Steering currents starts to vary at the beginning to achieve the required phase then it settle on a certain value indicating a fixed phase shift.

![Figure 2.7 2 PI currents](image)

2.7.2 CDR Loop Power Consumption

<table>
<thead>
<tr>
<th>Component</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase detector</td>
<td>604.2 uw</td>
</tr>
<tr>
<td>Charge pump</td>
<td>1.42 mw</td>
</tr>
<tr>
<td>Phase Interpolator</td>
<td>1.299 mw</td>
</tr>
<tr>
<td>CML to CMOS buffer</td>
<td>7.757 mw</td>
</tr>
<tr>
<td>Total power consumption</td>
<td>11.08 mw</td>
</tr>
</tbody>
</table>
Figure 2.7 3 Pie chart of the power consumption in the CDR loop

- Phase Detector: 604.2uW
- Charge Pump: 1.42mW
- Phase Interpolator: 1.29mW
- CML to CMOS: 7.75mW

- 69.94% of the power consumption
- 11.64% of the power consumption
- 12.81% of the power consumption
- 5.45% of the power consumption
2.8 De-Serializer (De-Multiplexer):

2.8.1 Concept Review:

The Demux circuit is the far end of our system. The Demux circuit in general is used to convert serial input data to parallel output data. With the development of CMOS technology, the minimum gate length continues to decrease and the frequency continues to increase. We use minimum sizing of 60 nm that makes the CMOS technology able to achieve such high speeds.

![Diagram of Demux circuit]

Figure 2-2-1: the Rx circuit showing the Demux.
CMOS vs. CML

Table 2.8.1 A comparison between CMOS and CML (current Mode logic) in case of an inverter.

<table>
<thead>
<tr>
<th>Point of Comparison</th>
<th>CMOS</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Inverter</strong></td>
<td><img src="image1" alt="CMOS Inverter Diagram" /></td>
<td><img src="image2" alt="CML Inverter Diagram" /></td>
</tr>
</tbody>
</table>
| **Power Consumption** | 1- No static power consumption  
2- Depend directly on the operation frequency | 1- Static power consumption due to continuous tail current M5  
2- Nearly depend on operation frequency |
| **Disadvantage**    | Poor immunity against ISI | Large power consumption |

**Notes on the comparison above**

Power in CMOS depends on frequency. While in CML it consumes more power due to current sources (constant).

CMOS is also referred as VML (voltage mode logic).
Storage elements (Latches & Flip-Flops)

Latches:

Latch is a circuit that has two stable states and can be used to store state information so it is simply a data storage element. There is 2- types of latches shown in figure (2.8.1).

![Positive Latch](image1)

![Negative Latch](image2)

Figure 2.8.1 the Rx circuit showing the Demux

Latch is the most basic circuit in the de-multiplexer. It plays a vital role in determining the timing and function of the whole circuit in achieving high speed with low power consumption. The most common structures are static latch, the Quasi static –CMOS latch, dynamic CMOS latch, Single-ended dynamic load latch and so on.

Table 2.8.2 static and dynamic latch

<table>
<thead>
<tr>
<th>Static Latch</th>
<th>Dynamic Latch</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3" alt="Static Latch using transmission gate" /></td>
<td><img src="image4" alt="Dynamic latch" /></td>
</tr>
<tr>
<td>Depends on static feedback loop to store Q</td>
<td>Depends on charge retention to store Q</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>----------------------------------------</td>
</tr>
<tr>
<td>CLK high → D affects Q</td>
<td>CLK high → D affects Q</td>
</tr>
<tr>
<td>CLK low → feedback loop stores Q</td>
<td>CLK low → Q is floating</td>
</tr>
</tbody>
</table>

In the design we intend to use CMOS logic circuits because the static power consumption of such circuits is almost zero and there is only the dynamic power and this will decrease the circuit power consumption.

**Master Slave Flip-Flops**

Two latches can be connected as Master & Slave to operate as a flip flop

![Master Slave Flip-Flops Diagram](image)

Figure 2.8.2 example on +ve edge triggered FF

**Clocked Inverters**

It is an inverter that controls its output by a clock.

From the opposite figure... If clk = 1, Inverter pass the input to output & If clk = 0, it holds the data as a latch (high impedance).
2.8.2  **Circuit Review:**

**Structure**

The de-multiplexer has mainly 3 types of structures: serial, parallel, and tree. Serial multiplexers are simple in design, however, multiple triggers work at very high data rate that lead to large power consumption. In parallel structures, there is only one trigger working on the highest data rate, so power consumption is minimal. However, it requires multiple clocks with different phases which complicate the circuit design. The tree structure Demux uses a hierarchical cascade structure and this makes the whole circuit run with low power and high speed.

**In our circuit and as the system required we will use a 2:16 tree structure de-multiplexer.**

**1st iteration:**

We tried to use the same topology as the multiplexer (the clock inverters topology) simply by reversing the inputs and the outputs as shown in figure (2-5).

![Clocked Inverter Topology](image)

Figure 2.8.3 clocked inverter topology used
The circuit developed a lot of problems and the De-multiplexing of the input data was not correct so we went for the conventional demux unit cell that consists of 5 latches and the problem was how to choose the right latch circuit.

Latches

During the study (papers and reference) different types of latches were suitable for example the single ended dynamic load latch shown in figure (2.8.4)

![Single ended CMOS dynamic latch](image)

Figure 2.8.4 single ended CMOS dynamic latch

Xie Feng, Xu Yanyi, “Design of low voltage ultra high speed 1:16 demux in 0.18 um Cmos”

This topology is excellent for high speed application but its only problem was the power consumption however we didn’t have any spec on the power but the aim of any good design is to minimize power consumption as possible so this topology was rejected.
CML circuits were an option of course but also the large power consumption was a trade-off.

2.8.3 Settled topology:

As mentioned before in the concept review we stated different topologies of latches one proven to be more suitable than the others is the CMOS dynamic latch shown in figure (2.8.5). The operation of such a simple circuit (transmission gate and an inverter) as explained above.

![CMOS dynamic latch](image)

Figure 2.8.5 CMOS dynamic latch

So for a unit cell Demux consisting of 5 latches the cell view is as shown in figure (2.8.6).

![1:2 demux structure block diagram](image)

Figure 2.8.6 1:2 demux structure block diagram
We can see from this structure that we used 5 latches:

DFF1, DFF2 makes a falling edge master-slave trigger

DFF4, DFF5 makes a raising edge master-slave trigger

In order to synchronize both outputs (1&2) DFF3 is used (half a duty cycle delay)

By using falling and raising edge FF we managed to sample data at both edges and hence achieved 1:2 demux functionality.

A simple timing diagram to elaborate this functionality is shown in figure (2.8.7) below.

![Timing Diagram](image)

Figure 2.8.7 1:2 demux timing diagram

The final tree structure of the 2:16 demux circuit is shown in figure (2.8.8) due to the symmetry of the circuit we draw only one half (1:8 demux).
Figure 2.8.8 2:16 demux tree structure
We note that both of the inputs are driven from the block before PI and that outputs are the end for the whole system the clock used is driven from the VCO and the divider all the rates, clocks and outputs are shown in the figure above.

2.8.4 Final design achieved

The final design achieved is illustrated in figure (2.8.8) while every 1:2 demux cell consist of 5 latches connected as in figure (2.8.6) and every latch is a CMOS latch shown in figure (2.8.5). The schematics was then put using cadence and are shown as following in figure (2.8.9).

![Figure 2.8.9 CMOS dynamic latch](image-url)
Notes on figure (2.8.10)

a) the sizing of the transistors is as minimum as possible

For all the NMOS: L=60nm, W=200nm, No. of fingers =1 finger

For all the PMOS: L=60nm, W=200nm, No. of fingers=2 finger

b) for the 1:8 demux and the other one (symmetry) we noticed that the output placed on top is always inverted than expected due to the presence of odd no. of inverter in the upper path so we added an extra inverter in order to even their no. and hence correct the output.

Results

The graph (2.8.11) shows inputs in orange, outputs of stage one in red, outputs of stage 2 in green, outputs of stage 3 in blue.
Figure 2.8.11 input and different stage outputs

The figure (2.8.12) shows the 1\textsuperscript{st} stage eye, (2.8.13) the 2\textsuperscript{nd} stage eye and 3\textsuperscript{rd} stage eye (2.8.14)

After running 100nsec simulation with periods 0.69ns, 1.38ns, 2.76ns respectively.
Figure 2.8.12 1st stage eye diagram

Figure 2.8.13 2nd stage eye diagram
The corner simulation was run in different types FF SS FS SF and the results were as same as figure (2.8.14) above. This shows that the circuit is functional under different conditions.

2.8.5 Specifications required and met:
The Deserializer circuit is working with minimum static power consumption equals 449 uW with high speed handling reaching 5.8 Gb/sec. The circuit works under different variations and conditions.

2.8.6 Conclusion:
A simple yet efficient topology is introduced to achieve the highest data rate handling and the maximum eye opening and minimum power consumption.
Chapter 3: Phase Locked Loop (PLL)

3.1 Introduction

The introduced PLL consists of: PFD/CP/LF, Dividers and VCO. There are two division values: 112 & 96, and the VCO can produce two frequencies: 4.992 GHz or 5.824 GHz. The reference frequency=52 MHz.

3.2 Phase/Frequency Detector, Charge Pump & Loop Filter

3.2.1 Concept Review

PFD, charge pump and loop filter are of the main blocks in the PLL. The simple PLL consisted of VCO, PD and one capacitor that acts as a loop filter, but because of the inefficiency of such a simple design, a frequency detection property was added to the phase detector, and also a charge pump is introduced.

The basic idea of such blocks is that the PFD detects the difference in frequency and phase between two input signals; reference frequency (52 MHz) and feedback-divider frequency. The output pulses that represent these differences are introduced to the charge pump that generates an equivalent current, which in return passes through a loop filter that converts this current to voltage to control the output of the VCO, so that the VCO can increase or decrease its output frequency, until it matches the reference frequency (after being divided).

The PFD's main problem is the Dead Zone problem. Simply, when the input signals of the PFD have a very small phase difference, sometimes the PFD
can't detect that difference, that's what's called a "Dead Zone". The Dead Zone causes the PLL not to lock properly, resulting in jitter "phase noise".

The Charge Pump has his own problems as well. Clock feed-through is one of the most known problems of the CP. It can be avoided by placing the switches away from the output node.

The loop filter main compromise is the choice between second and third order, since the filter consumes much area while a higher order introduces more stability.

3.2.2 Circuit Review

3.2.2.1 PFD

Many topologies were proposed:

GDI Cell

The first proposed circuit works similar to conventional PFD but it has many advantages. This PFD is basically constructed with two GDI (Gate Diffusion Input) cells.

![GDI Cell Diagram](image)

Figure 3.2.1 GDI Cell

This technique allows reducing power consumption and area. A variety of GDI implementations are compared with typical CMOS asynchronous circuits. Dynamic GDI state holding elements are 2× smaller than CMOS C-
elements. It's also faster, and consumes less power. GDI performs better under reduced supply voltage.

Figure 3.2.2 GDI Cell-based PFD

The only drawback of the above circuit is that its range is between (–pi,pi). Instead, a topology with range (-2pi,2pi) will be used.

TSPC

TSPC (True Single Phase Clock) D-flip flop is widely used as it has less number of transistors than that of CMOS, and also CMOS needs both Clk and inverted Clk. It also consumes low power.

The drawback of this topology is the charge leakage problem, especially under considerably low frequencies.
The third proposed topology is the CMOS topology.

CML

CML was out of question since it consumes higher power than CMOS in low
3.2.2.2 Charge Pump

There's a compromise between single-ended and differential control path to achieve better noise immunity. Since the differential charge pump requires two loop filters, which means larger chip area and more complex CP circuitry, then a single-ended topology will be chosen. Besides, noise isn't of much effect in the proposed PLL.

The first proposed circuit for the CP is an o/p cascade circuit, to increase the output impedance, but since cascade consumes more headroom and the supply voltage is low, it was hard to use that circuit with such a low supply.
The second proposed circuit is the conventional charge pump, where the switches are placed at the supply rails to avoid clock feed-through effect.

![Conventional Charge Pump](image)

**Figure 3.2.6 Conventional Charge Pump**

### 3.2.2.3 Loop Filter

The first order loop filter is out of our scope because it doesn’t suppress the ripples efficiently. The choice is between the second and third order loop filter, where there is a trade off; the third order introduces an additional pole which results in a more stable loop, but on the other side, the third order is an active filter, which consumes power, unlike the second order loop filter which is a passive filter.
Since the third order filter contains a series resistance, it means that the equivalent voltage coming from the charge pump won't be the same as the control voltage that reaches the VCO (voltage drop on R3), that's why an amplifier is used in that case.
3.2.3 Settled Topology

PFD

CMOS technology is used for the design of the PFD.

Charge Pump

Conventional charge pump is used. It performs the required task efficiently and its switching speed isn't slow.

Loop Filter

A second order LF is used.

3.2.4 Final Design

PFD

Average power consumption of the PFD=6 µm.

Figure 3.2.10 CMOS Based PFD
The UP/DOWN signals and UP-B/DOWN-B signals will arrive at different times to the CP inputs, since UP and DOWN signals are delayed by one inverter delay. To solve that problem, two inverters will be added in the path of the DOWN signal, from the PFD to the charge pump input. These two inverters should have the same delay as that of the inverter from UP to UP-bar.

![Figure 3.2.11 PFD Output](image)

Figure 3.2.11 PFD Output
UP and DOWN pulses that appear at locking cause the CP current sources to turn on temporarily, which causes reference spurs at the output spectrum when the loop is locked.

**Charge Pump**
The conventional charge pump will be used.

Average power consumption of the CP = 0.52 mW
As shown in the above figure, there's no mismatch between the UP and DOWN currents. For current matching, long devices are preferable. So, the length of the transistors that are connected to the output node has been increased up to 1µm.

Figure 3.2.14 Compliance Range
As shown in the above figure, the compliance voltage ranges between 0.2 → 0.8 volt.

Figure 3.2.15 PFD/CP Output Current Noise

As shown above, the flicker noise is quite high, because the channel length is very low (65nm). Flicker noise is inversely proportional to channel length.

Figure 3.2.16 PFD/CP Phase Noise
**Loop Filter**

The values of the loop filter components are calculated using the Matlab code.

![Loop Filter Diagram](image)

Figure 3.2.17 Loop Filter

<table>
<thead>
<tr>
<th>Passives</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td>Capacitor</td>
<td>0.391 pF</td>
</tr>
<tr>
<td>C2</td>
<td>Capacitor</td>
<td>7.58 pF</td>
</tr>
<tr>
<td>R2</td>
<td>Resistance</td>
<td>18 KΩ</td>
</tr>
</tbody>
</table>

Table 3.2.1 Loop Filter Components

3.2.5 **Specifications**

The compliance range is as expected.

The PFD is robust across corners (Speed, temperature and supply voltage)

The CP is robust across all corners except “SF-temp125-supply1.1” & “SF-temp125-supply0.9”, where the output is slightly changed.
3.3 **Dividers**

3.3.1 **Concept Review**

Dividers are a very important block in phase locked loop, the loop can have more than one divider.

1) Feedback Divider which can be integer or fractional depends on the type of PLL. – Division Ratio N-

2) Divider for input frequency.

Division Ratio- M –

$$\text{In this case } f_{out} = \frac{N \times f_{in}}{M}$$

There are 2 main Divider types:

1- **Synchronous Divider:**

All flip flops work at high frequency so it consumes high power.

Large loading on the input frequency signal.

![Figure 3.3.1 Synchronous Divider (Michael Perrot Slides)]
2- Asynchronous Divider:

**Advantages**

a) Each block runs at lower frequency and this result in reducing power.
b) Simple in Design.

**Disadvantages**

a) Accumulative Jitter due to cascading Blocks.

As the problem of asynchronous divider is accumulated jitter, we introduce the input frequency to a flip flop at the end to reduce the jitter.
3.3.2 **Circuit Review**


So our chosen topology

4 divide by 2 cascaded blocks & Divide by 6 or 7 block.

"*Divide by 2*" block:

The first 2 blocks works at high frequency, so the choices were between CML or TSPC.

**CML latches**

**Advantages**

a) Very fast – allows for very high frequency.
b) Signal propagates through 2 CML gates per cycle.
c) Accepts CML input levels.

**Disadvantages**

a) Static power consumption.
b) Biasing source required.
c) Large number of transistors.

**TSPC circuit**

**Advantages**

a) Fast – allow high frequency .
b) Compact size.
c) No static power –except for sub-threshold current .

**Disadvantages:**

a) Signal goes through 3 stages per cycle.
b) Requires rail to rail input signal.

c) Dynamic flip flop is not efficient at very low frequency due to charge leakage.

In the third and fourth stage the advantages of CML & TSPC aren't not required, so we can use either static Flip flop or a Dynamic one.

Differences between them

a) Delay.
b) Power consumption.
c) Robustness across corners

Dynamic circuit has less delay and less power consumption, but static circuit is Robust across corners.

3.3.3 Settled Topology

As our main concern is power consumption, so for first and second stages we can use TSPC circuit as it consume less power than CML.

Third and fourth block, options were static D-flip flop Dynamic one after running corners simulation static flip flop is robust across corners and only higher by 6u in power, so the choice is static CMOS circuit.
3.3.4 Final Design

TSPC
Figure 3.3.4 Flip-Flop

Static Flip flop

Figure 3.3.5 Static Flip-Flop
Divide by 6 & 7 circuit
For divide by 7 circuit

Figure 3.3.6 Divide By 7 Logic Diagram

Figure 3.3.7 (Figure from Deepak Floria slides)
Divide by 6 circuit

![Diagram of Divide by 6 circuit](image)

Figure 3.3.8 Divide By 6

Consists of "divide by 2" stage then divide by 3

"Divide by 6" and "divide by 7" are combined together using the same circuit

To choose whether divide by 6 or divide by 7 we have a control voltage

a) If control voltage =1, circuit will divide by 7.

b) If control voltage =0, circuit will divide by 6.

If we’re dividing by 7 the same clock will enter the 4 flip flops, but if we’re dividing by 6 we divide by 2 using the first flip flop then divide by 3 using the remaining flip flops, so the output of divide by 2 stage will be the clock for the 3 remained flip flops.

To select between them we use multiplexer, where its selection is the control voltage.
If control volt = 0 → output of the multiplexer = S0, S0 is the output from divide by 2 stage.

If control volt = 1 → output of the multiplexer = S1, S1 is the input clock for the whole stage.

### 3.3.5 Specifications

Total power consumption = 44.7uw

Total delay of the divider = 0.2578 ns

After running ocean code for corners circuit is robust across PVT.

**Noise analysis**

Pss analysis then Pnoise analysis

![Figure 3.3.9 Phase Noise](image-url)
Flicker noise = -107.9 dBc/Hz

White noise = -157.9 dBc/Hz

**Divider output**

![Divider Input and Output](image)

Figure 3.3.10 Divider Input and Output
3.1 **Voltage Controlled Oscillator (VCO)**

3.1.1 **Concept Review**

Voltage-Controlled Oscillator (VCO) is the pulsating heart of any Phase-Locked Loop (PLL) or Delay-Locked Loop (DLL). It provides the raw periodic signal of the local clock generator. Usually, Oscillators are classified into two main categories according to their output waveform: a) Harmonic oscillators, and b) Relaxation oscillators (commonly known as ring oscillators).

The harmonic oscillators usually contains a LC resonator (so it is commonly known as LC oscillators) generating sinusoidal (or nearly so with definite frequency) output waveform, i.e. it has small harmonic contents. But, according to ring oscillators, most ones switch back and forth between equilibrium states so the output waveform will be a square wave i.e. a non sinusoidal waveform. Among the most important design parameters of VCOs is the phase noise, tunability and power consumption. At this point, LC oscillator is the best choice for lower phase noise and lower power than most ring oscillators. But, when small area and large tuning range are more important specifications, then ring is the preferable. Also, another important advantage of ring oscillator vs LC is the multi-phase outputs which are generated inherently using ring oscillator which is required for clock and data-recovery in the receiver. And, for our application, small area, moderate phase noise and quadrature outputs are the main requirement for the VCO, so, ring oscillator is the one to be implemented.

Ring oscillator is just a negative feedback system of cascaded inverters that is to be designed to operate at a certain frequency \(\omega_o\) where it turns to a positive feedback system, satisfying the Barkhausen criteria to start the
oscillations but when it comes to deciding what is the suitable number of stages required, there are two methodologies:

1- Either choose suitable number of stages to get a value of gain per stage to be enough to start and sustain oscillations and could be achieved by the used topology.

2- According to required speed, choose suitable number of stages with certain delay. For example, consider a generic 3 stage ring oscillator as in figure(3.4.1). When oscillations are sustained, the output waveforms at nodes x, y, and z will be as shown in figure(3.4.2). As shown, the phase difference between these waveforms represent the delay (Td) caused by each inverter so the inverters should be designed such that period of oscillation (T) is double the total delay across the loop, i.e. \( T = 2(Td + Td + Td) \). Or, generally, \( T = 2N Td \) such that \( N \) is the number of inverters. This methodology is usually the easier and more suitable to full switching inverting stages. But this number should be odd so as to keep the necessary 180° dc phase shift across the loop and to avoid latch up but how can be this condition overcome?. Thanks, to differential amplifier (inverting stages) as we can use even number of stages simply by non inverting connections at the last stage as shown in figure(3.4.3) for a four stage differential ring oscillator. Also, another advantage appears when using differential inverting stages is quadrature outputs as each output is shifted by \( 360° / 4 = 90° \).
Figure 3.4.1 Generic three stage ring oscillator

Figure 3.14.2 Waveforms at output nodes
3.1.2 Circuit review

Now let's tune the simple ring oscillator to be a VCO. This will be done side by side with showing the common inverting topologies which are strongly related to the mechanism of controlling the frequency of operation of the oscillator.

A note at the start of the next discussion: a one stage will always be shown just to view the operation of each topology.

First, we shall consider the circuit shown in figure 3.4. M3 and M4 are in deep triode acting as a VCR (Voltage Controlled Resistor) so by controlling its value we shall vary the time constant of charging and discharging the load capacitance, accordingly, the delay caused by the stage and so the frequency of oscillation based on the following equations

$$\tau_1 = R_{on34} \cdot C_L = \frac{C_L}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{3,4} (V_{DD} - V_{cont.} - |V_{THP}|)}$$

$$f_{osc.} \propto \frac{1}{T_D} \Rightarrow f_{osc.} \propto \frac{\mu_n C_{ox} (V_{DD} - V_{cont.} - |V_{THP}|)}{C_L}$$

An advantage of this topology is the direct proportionality between the oscillation frequency ($f_{osc}$) and the control voltage ($V_{cont}$) but a drawback arises due to variable output swing as the output resistance is variable across
the frequency. Then topology used in figure (3.4.5) overcomes this problem. The idea is servo the on-resistance of $M_3$ and $M_4$ to that of $M_5$ and vary the frequency by adjusting $I_{ss}$ and $I_1$ simultaneously. If $M_3$ and $M_4$ are identical to $M_5$ and $I_{ss}$ to $I_1$, then $V_x$ and $V_y$ vary from $V_{DD}$ to $V_{DD} - V_{ref}$ as $M_1$ and $M_2$ steer the tail current to one side or the other. Thus if the process and temperature variations, say, decrease $I_1$ and $I_{ss}$, then $A$ increases the on-resistance of $M_3$-$M_5$, forcing $V_P$ and hence $V_x$ and $V_Y$ (where $M_1$ and $M_2$ are fully on) equal to $V_{ref}$.

Figure 3.14.4 Differential pair with variable output time constant
A third way can be used to control the resistance by employing negative variable resistance as shown in figure(3.4.6). By changing $I_1$, the negative resistance can be changed (cross coupled transistors have an equivalent resistance of $-2/g_m$) so the total resistance at the load changes, changing frequency of oscillation but still the usual problem due to variable resistance, namely, variable output swing. This time, it'll be solved by employing a differential pair that drives the required current for the differential amplifier and the negative resistance using a total current $I_T$ as shown in figure(3.4.7). If $M_1$-$M_4$ experience complete switching per cycle, then $I_T$ is steered through $R_1$ ($R_2$) through $M_1$ and $M_3$ ($M_2$ and $M_4$). Differential control voltage improves higher immunity against noise but as it's clear, for low supply, this configuration is hard to design so a folded cascode can be employed as in figure(3.4.8).
Figure 3.14.6 Differential stage with variable negative resistance load

Figure 3.14.7 Use of a differential pair to steer current between M1, M2, M3, and M4

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The fourth technique to control the frequency of oscillation is by using delay interpolation. This concept is viewed in figure (3.4.9). Cascading many stages and enabling and disabling fast and slow paths all through the stages, variable delay is attained.
3.1.3 **Settled topology**

As the CDR loop requires quadrature output, number of stages was restricted to four stages.

As mentioned before, the only topology that has less problems was the differential pair with variable negative resistance load so it was my choice for starting the design of the required ring VCO. The design started without the negative resistance, oscillations were obtained at the required frequency of operation (which is high) using a low value resistance but when it came to choose the range of $g_m$ for the required range of operation, a trade-off arose. For moderate values of negative resistance across the tuning range, $g_m$ was somehow high which required large transistors, which simultaneously led to large intrinsic capacitance degrading the frequency of oscillation. But after many iterations, the required frequency could not be achieved.
Then, I headed for the Maneatis delay cell shown in figure(3.4.10). It was famous for good supply noise rejection through the replica biasing as discussed in the paper inspected by Maneatis himself. The symmetric load is required to attain tuning linearity. When the design started, the short channel effects (output resistance of the transistors was comparable to the $1/g_m$ of diode connected load) appeared significantly leading to less total output resistance making gain per stage not sufficient to start oscillations and even when finally the gain condition was satisfied, it came to the frequency of oscillation ($f_{osc} \propto g_m$ which can be derived easily starting from Barkhausen criteria) that could not be achieved as it 'll degrade the gain too and further increase in current requires large transistors leading to higher intrinsic capacitance degrading the speed.

![Maneatis Delay cell](image)

Figure 3.14.10 Maneatis Delay cell
Searching more and more, a PhD thesis of Mozhgan Mansuri about “low-power low-jitter on chip clock generation” appeared, where he used a CCO (Current Controlled Oscillator) in the form of a pseudo-differential inverters which is most commonly known as DCVSL (Differential Cascade Voltage Switch Logic) showing in figure(3.4.11), a certain type of inverters that was discussed thoroughly by Prof. A. Mason as a single ended CVSL. And at last, Prof. Edgar Sanchez used the DCVSL can be used as a ring VCO not CCO. The design in this case is much simpler than that of the previous topologies in that, for DCVSL, rail to rail switching occurs i.e. large signal analysis using the equation \( T = 2N T_d \) where \( T_d \) is the average of \( t_{PLH} \) and \( t_{PHL} \) which are the low to high propagation delay and high to low propagation delay respectively. These can be calculated easily in cadence. But an undesired affect appeared is the assymetry between high and low transitions in the essence that \( t_{PLH} \) is usually greater than \( t_{PHL} \) as the pMOSs do not switch due to the input signal (as in the case of nMOSs) but due to the output signal of the opposite branch leading to this increase in the \( t_{PLH} \). This problem will be eliminated in the next section.

![Figure 3.14.11DCVSL](image-url)
3.1.4 **Final design achieved**

After required $t_{PHL}$ (which is half oscillation period) was adjusted, we would like to decrease the $t_{PHL}$ to obtain symmetric transitions. This can be achieved by introducing more voltage drop across the gate of pMOSs leading to less faster change in gate voltage leading to less $t_{PHL}$. Adjusting the suitable value of the resistance so as to get symmetric transitions, we get the DCVSL-R as shown in figure(3.4.12).

![Figure 3.4.12 DCVSL-R](image)

3.1.5 **Specifications required and met**

The specifications for the PLL were a power budget of 20 mW and a total jitter of 2 ps at its output. The output frequency is either 4.992GHz or 5.842 GHz according to the divider ratio. For, the VCO, I managed to achieve a 0.5
ps jitter that is equivalent to nearly -95 dBc / Hz at 10 MHz offset from the oscillation frequency. The upper limit of the power consumption of the VCO was about 12 mW at TT and as worst case across corners, it reached 15 mW. Also, $K_{VCO} = 5.93\text{GHz/V}$. Start-up time is about 307p in average for TT. The results will be shown in the next series of figures.

Figure 3.14.13 Tuning Sensitivity of VCO

Figure 3.14.14 Phase noise of VCO at 10 MHz offset from frequency of oscillation
Figure 3.14.15 Output Waveforms (Vo1- and Vo3- are in quadrature)

Figure 3.14.16 Output power across corners (Worst case shows 15mW)
3.1.6 Conclusions

Ring vco proves being easily designed fast and rail-to-rail switching can be obtained with sharp transitions which is effective for clock generation but on the expense of high power and moderate phase noise which is not a major issue in our application. Also, for newer technologies including short channel effects and low supply, makes a trade-off between using current steering topologies and speed. So, I think that rail-to-rail switching topologies are the most convenient for newer technologies used for high frequency applications.
3.2 PLL Loop Behavior

As shown above, the PLL locked before 0.5µsec and the V-ctrl is constant, and both UP and DOWN signals have a very small width.

Figure 3.5.1 UP, DOWN and V-ctrl
Figure 3.5.2 VCO and Divider frequencies

An open-loop analysis was performed using Matlab code and these are the outputs.

Figure 3.5.3 Open-loop Analysis
As seen above, at 0 dB, the phase margin equals 65.

The power budget for the proposed PLL was 20mW. According to the following chart, the total power consumed by the PLL is 15.57mW.

![Power Contribution in PLL](image)

**Figure 3.5.4 Power Contribution in PLL**

As seen above, the VCO has the highest contribution of power consumption, followed by the charge pump, then the dividers and the PFD comes at the end with the smallest power consumption.
Chapter 4: Power Management

4.1 Bias Cell and Voltage reference

4.1.1 Concept Review

i. **Introduction:**

The bias cell is an important block in any system, as it distribute currents and voltages needed by the system blocks. It is not realistic to make pins for each block to provide each block certain current or voltage, consequently we instead take from 1 pin the voltage coming from the device’s battery.

**Why we do need BGR Circuit:**

Analog circuits incorporate voltage and current references extensively. Such references are dc quantities that exhibit little dependence on the supply and process parameters and a well-defined dependence on the temperature. For example, the bias current of a differential pair circuit and many other systems like A/D and D/A converters a reference is required to define the input or output full scale range. So we need to provide those blocks supply independent biasing, that is why we reach the solution of using the BGR circuit.

In order to establish a dc voltage or current that is independent of the supply and process and has a well-defined behavior with temperature.
ii. **BGR Main Concept:**

The main concept of the BGR is to have 2 quantities with opposite TC and with their summation we get zero TC.

\[
V_{\text{REF}} = \alpha_1 V_1 + \alpha_2 V_2
\]

\[
\alpha_1 \frac{dV_1}{dT} + \alpha_2 \frac{dV_2}{dT} = 0
\]

The characteristics of PN Junction (BJTs and diodes) have proven the most well defined quantities providing positive and negative TC. Although nowadays most of the larger analog and mixed-signal circuits are fabricated in CMOS processes and use only MOS transistors. The band gap reference is usually an exception where either a parasitic BJT or a pn junction is used for the temperature-sensitive part of the band gap reference. There has been some research on CMOS only references that do not use a pn junction, but the BJT (or pn junction) is still overwhelming the device of choice in band gap design because of what most believe is better performance and lower design complexity. A study of the BJT’s temperature characterization is fundamental to BJT-based band gap reference design.

Where \( KT/q \) has a positive temperature coefficient (PTAT), and the \( V_{BE} \) of a BJT or \( V_D \) of a diode decrease with temperature (CTAT).
### iii. BJT Vs. MOSFET:

BJT doesn’t change with the process variation that is why it is more preferable than the MOSFET since it is very sensitive to the process variations.

In the coming section the temperature behavior of the BJT will be discussed.

### iv. Source of CTAT:

\[ V_{BE} = V_T \ln \left( \frac{I_C}{I_S} \right) \]

\[ \frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4 + m)V_T - \left( \frac{E_g}{q} \right)}{T} \]

This gives \( \frac{\partial V_{BE}}{\partial T} \approx -2 \text{ mV/}^\circ \text{K ant } 300^\circ \text{K} \)
v. **Source of PTAT:-**

This Circuits provide PTAT voltage due to different sizing of BJT’s and same applied current where the

\[
\Delta V_{BE} = V_{BE1} - V_{BE2}
\]

\[
\Delta V_{BE} = V_T \ln \left( \frac{I_{c1}}{I_{c2}} \right) - \frac{KT}{q} \left( \frac{I_{c1}}{I_{c2}} \right)
\]

vi. **Startup Circuit:-**

The band gap circuit has 2 stable point. One that we are operating at and the other is a trivial one where I=0. To solve this problem we go for constructing a startup circuit that force a current in our band gap circuit to flow then the startup is to be switched off after that so as not to consume more power.

Where

Point B shown in the previous Figure is a parasitic operating point: self-
biasing represents positive feedback. Whereas the noise in the circuits tends to drive the circuit operating point from B to A.

4.1.2 Circuit Review

There are various topologies for the design of the BGR circuit. Each has its advantages and disadvantages. Through this part of this thesis I will be discussing 3 of these topologies and their tradeoffs.

i. Topology (1) PTAT Current BG without OTA:

We design this circuit to obtain that the 2 point \( V_A \) and \( V_B \) to be equal, this by adjusting the value of “R”.

Where

\[
I = \frac{V_{BE1} - V_{BE2}}{R1} = \frac{\Delta V_{BE}}{R1} = \frac{V_T}{R1} \ln \left( \frac{I_1}{I_2} \cdot \frac{I_{s2}}{I_{s1}} \right)
\]

\[
I = \frac{V_T}{R} \ln(n) \quad \text{Supply independent}
\]

This current depend on \( \Delta V_{BE} \) which represent the PTAT part, thus the Current generated is a PTAT current.

\[
V_{REF} = V_{BE3} + I \cdot R_2
\]

\[
V_{REF} = V_{BE3} + \frac{\Delta V_{BE}}{R_1} \cdot R_2
\]

The TC of the PTAT (dependent on \( \Delta V_{BE} \)) and CTAT (dependent on \( V_{BE3} \)) in this circuit will lead us during designing to get \( V_{ref} = 1.205 \text{ V} \), in order to get a constant volt across the temperature, thus it is not applicable to get a desired value given this circuit.
Also it consumes less power than other topologies since it doesn’t require an OTA that consume a good portion of power.

This Topology has a high impedance node where it is not easily designed to choose the value of “R” to get \( V_A = V_B \).

That is why we will discuss a solution of designing an OTA to adjust both \( V_A \) and \( V_B \) to be equal.

**ii. Topology (2) PTAT Current BG with OTA:**

This topology is very similar to the previous topology, and we added the OTA for enhancing the previous circuit. The OTA is used in the Circuit as a feedback to adjust the 2 points \( V_A \) and \( V_B \), where its output will bias PMOS.

This Circuit has both positive and negative feedback.

\[
I = \frac{V_{BE1} - V_{BE2}}{R1} = \frac{\Delta V_{BE}}{R1} = \frac{V_T}{R1} \ln \left( \frac{I_1}{I_2} \cdot \frac{I_{s2}}{I_{s1}} \right)
\]

\[
I = \frac{V_T}{R} \ln(n) \quad \text{Supply independent}
\]

\[
V_{REF} = V_{BE1} + I \cdot R_2
\]

\[
V_{REF} = V_{BE1} + \frac{\Delta V_{BE}}{R_1} \cdot R_2
\]

Where \( R_2 = R_3 \).

Now we solved the problem of adjusting \( V_A = V_B \) by burning more power in the OTA.
The OTA must be designed that the current source of it has a value double the value of the current passing through the branches of the BG circuit “I”.

But yet we can’t control the value of the desired Vref and we can only achieve a voltage 1.205V as the previous topology.

iii. **Topology (3) CMOS BGR with Sub-I-V operation.**

In this topology we overcome many of the previous circuit’s defects as we can provide both constant voltage and current using this circuit, also we can have any desired value for Vref by adjusting the Value of R3.

This circuit provide Current constant by having 2 kinds of Currents, CTAT Current “I₂” and PTAT Current “I₁” to be added to each other to get a Constant current across the Temperature. Then we can provide constant voltage by multiplying this current in a resistance as shown in Figure.

Where

\[ I = I₁ + I₂ = \frac{V_{BE1} - V_{BE2}}{R₁} + \frac{V_{BE2}}{R₂} \]  
Supply, Temperature independent

\[ V_{REF} = I \times R₃ \]

\[ V_{REF} = \left( \frac{V_{BE1} - V_{BE2}}{R₁} + \frac{V_{BE2}}{R₂} \right) \times R₃ \]
BUT, if our resistors are on chip then they have a temperature coefficient that might stop me from having both current and voltage constant since the current is dependent on the resistance which is dependent on the temperature.

iv. **Startup Circuit:**

We only need a start-up circuit to avoid the stable state at I=0 when the voltage supply first startup.

This self-biased circuit is usually used for starting up the circuit and biasing the bias cell of the used OTA. It is good to use it in order to avoid the I=0 saturation point.

Where when V_{dd} is still off I=0 initially then V_X =0 \rightarrow V_Y =V_{dd} , then T_9 will start to pull up V_z to make current flow in T_5 then V_X starts to rise and V_Y starts to fall till T_9 gets off, when the current reaches its steady state. So the startup is off after we reach the required operating point to as not to consume power.

4.1.3 **Settled topology**

I settled on the 3rd Topology (CMOS BGR with Sub-1-V operation), since it provides less variation in the current yet not a constant current due to the temperature coefficient of the resistors. Getting 1V reference voltage unlike the other where I was forced to produce 1.205V. On the other hand I consumed more power due to the existence of the OTA and the extra Branch.
A well designed OTA must be used for reaching out Requirements to adjust the 2 points, get the suitable value for biasing the PMOS and get low voltage difference across the temperature. All by keeping in mind the stability of the circuit.

4.1.4 Final design Achieved

i. Circuit Schematic:

![Circuit Schematic](image)

Table 4.1.1 sizing of the BGR circuit

<table>
<thead>
<tr>
<th>Component</th>
<th>Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>L= 6u W=4.1u number of fingers= 4</td>
</tr>
<tr>
<td>R1</td>
<td>L=2u W=7u number of fingers=9</td>
</tr>
<tr>
<td>R2</td>
<td>L=2u W=7u number of fingers=85</td>
</tr>
<tr>
<td>R2</td>
<td>L=2u W=7u number of fingers=74</td>
</tr>
</tbody>
</table>
ii. OTA and its biasing cell :-

I used Folded PMOS input cascaded to get an output of 1.6 V to bias the PMOS in the BGR and PMOS input due to having small input to provide me reasonable gain and stability.
Table 4.1.2 Folded OTA Sizing

<table>
<thead>
<tr>
<th>Component</th>
<th>Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mp1</td>
<td>L= 6u W= 1.6u number of fingers=6</td>
</tr>
<tr>
<td>Mp2</td>
<td>L= 6u W=4.1u number of fingers=4</td>
</tr>
<tr>
<td>Mpin</td>
<td>L=5u W=1.8u number of fingers=2</td>
</tr>
<tr>
<td>Mpss</td>
<td>L=2u W=6.8u number of fingers=10</td>
</tr>
<tr>
<td>Mn1</td>
<td>L=6u W=6.7u number of fingers=6</td>
</tr>
<tr>
<td>Mn2</td>
<td>L=6u W=2u number of fingers=6</td>
</tr>
</tbody>
</table>

This OTA needs to be biased so it is preferable to construct a bias cell independent on your BGR to bias the OTA.

We used this resistance to generate the required current in my bias cell
Table 4.1.3 Biasing of the OTA sizings

<table>
<thead>
<tr>
<th>Component</th>
<th>Sizing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mp1</td>
<td>L= 6u W= 1.6u number of fingers=6</td>
</tr>
<tr>
<td>Mp1/3</td>
<td>L= 6u W= 1.6u number of fingers=2</td>
</tr>
<tr>
<td>Mpss</td>
<td>L= 2u W=6.8u number of fingers=10</td>
</tr>
<tr>
<td>Mn1</td>
<td>L=6u W=6.7u number of fingers=6</td>
</tr>
<tr>
<td>Mn2</td>
<td>L=6u W=2u number of fingers=6</td>
</tr>
<tr>
<td>Mn2/3</td>
<td>L=6u W=2u number of fingers=2</td>
</tr>
</tbody>
</table>

### iii. Startup Circuit

I used a very simple startup circuit to initiate current in the BGR when it first start up

This Circuit Will be on always if we increased the voltage supply since the input of the inverter will be considered a zero.
Transient Response for the Startup Circuit

Outputs and Conclusions

This is the output desired from the BGR to have constant Voltage and PTAT Current.
The stability of the BGR Circuit

Figure 4.1.1 Stability analysis
Across Corners

Running the circuit across all possible corners using an ocean code

To see if the circuit function well across corners.
4.1.5 Layout

i. The rule of BJT

In CMOS technologies, where the independent bipolar transistors are not available, parasitic bipolar transistors are used.

Realization of PTAT voltage from the difference of the source-gate voltages of two MOS transistors biased in weak inversion is also reported in the literature.

![Parasitic bipolar in a CMOS technology](image)

Figure 4.1.2 Parasitic bipolar in a CMOS technology

m is often equal to 8 for ease of layout matching.

A parasitic bipolar is used in standard CMOS technologies.

![Layout diagrams](image)
4.1.6 Conclusion:-

It is important to have a well-designed BGR and bias cell in order to provide constant volt and proper current needed by the blocks of the system.

In (CMOS BGR with Sub-1-V operation) we can’t ideally get constant volt and current when the resistance are on chip since they have a TC so we can have either constant Current or Constant voltage.

Under some analysis I deduced that also the MOSFets have TC which can be compensated by putting the opposite type MOSFET

In the used Topology I substituted the resistance R3 in the Vref branch with an NMOS diode connected having the same resistors value , and this gave me both constant voltage and current , BUT it isn’t maintained through corners since the current is still inversely proportional to the resistance that changes through corners.

Using a well-designed OTA is very Important for our BGR circuit, to maintain good stability for the BGR circuit with high gain to decrease the variation of the $V_{ref}$ with temperature.
4.2 LDO

4.2.1 Concept Review
LDO stands for Low Drop Voltage Regulators, LDO provide stable DC voltage with the required driving capabilities.

The operation of the LDO based on pass element that have the voltage difference between the input and the output voltages, and feedback to control the output voltage.

LDO main parameters
1. Line and Load regulation
2. PSRR
3. Transient response and over shot
4. Stability
5. Noise
**Line Regulation**

Is to maintain the required DC output voltage with changing input voltage, so if the input voltage increased so $V_{ds}$ is increased, so to maintain constant Load current $V_{gs}$ should be decreased as shown in figure 4.2.1-2 “going from Po to P1” and vice versa, Line regulation can be calculated and defined using figure 4.2.1-3

![Diagram of Line Regulation](image)

Line Regulation = \[ \frac{\Delta V_{out}}{\Delta V_{in}} \]

\[ \Delta V_1 = A_{ea} \beta \Delta V_{out} \]

\[ \Delta V_{out} = A_{pt} (\Delta V_{in} - \Delta V_1) \]

\[ = A_{pt} (\Delta V_{in} - A_{ea}\beta \Delta V_{out}) \]

\[ \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{pt}}{1 + A_{pt} A_{ea} \beta} \approx \frac{1}{A_{ea} \beta} \]
Let APT Area are the pass element gain and the Error amplifier gain respectively, $\Delta V_{out}$, $\Delta V_{in}$, $\Delta V_{I}$ are defined in figure 4.2.1-3.

Clearly, Line regulation depends on the Error amplifier gain.

**Load Regulation**

Is to maintain the required DC output voltage with changing load current, figure 4.2.1-4 shows that if the load current increases and to maintain constant $V_{ds}$, $V_{gs}$ should be increased and vise versa.

**PSRR**

PSRR stands for Power Supply rejection ratio and it is a measure for how well the LDO reject replies coming from the supply.
PSRR \quad = \quad 20 \log \frac{\text{Input Ripples}}{\text{Output Ripples}}

This equation gives result depends on different architecture

**Transient Response**

Due to load sudden variation the output voltage would fluctuate experience over and under shot

\[
\Delta V_{tr} = \frac{I_{max} \Delta t}{C_{out}} \quad \Delta t = \frac{1}{BW}
\]

Were \( \Delta t \) is the time for the LDO to respond, and BW is the open loop Bandwidth

**Stability**

Stability analysis for LDO is different for each architecture, however LDO have two main poles, one at the Error amplifier output and the other at the LDO output, to maintain stability one should be capable of spreading of those two poles.

**Noise**

Noise Sources:

1. Band gab Reference can be solved by RC filter.
2. Resistors, we could use smaller resistors but this decrease LDO efficiency.
3. Error amplifier, we could use larger input devices.
4.2.2 Circuit Review

External Cap LDO

One of the easiest topologies is to put large nonintegrated cap at the output of the LDO to push the output pole of the LDO to maintain stability this large cap also decrease over shot

We can define the open loop gain

$$A_v = \frac{g_{ma} \cdot R_{oa} \cdot g_{mp} \cdot Z}{1 + s \cdot R_{oa} \cdot C_{par}} \cdot \frac{R_1}{R_1 + R_2}$$

$$Z = R_x \left| \frac{1 + s \cdot R_{esr} \cdot C_o}{s \cdot C_o} \right| \frac{1}{s \cdot C_b} \approx \frac{R_x (1 + s \cdot R_{esr} \cdot C_o)}{(1 + s \cdot (R_x + R_{esr}) \cdot C_o) (1 + s \cdot R_x \cdot |R_{esr}| \cdot C_b)}$$

$$R_x = R_{opass} || (R_1 + R_2)$$

Figure 4.2.2-1 illustrates the typical frequency response of the system
This topology is easy to stabilize and gives good overshoot and PSRR could be enhanced by feed forward Ripple cancelation however external non integrated cap is expensive for mass production.

**Capacitor less LDO**

This topology stabilize the circuit with small integrated cap at the output of the Error amplifier, however it is difficult to stabilize the LDO at no load because at no load the LDO output pole shifts to lower frequency, it also have bad overshoot because of small output caps, so it is used for stable loads, it gives a fair PSRR.
Millken LDO

Millken LDO is also fully Integrated LDO used to solve the transient problem, and give stable circuit at no load, and also give fair PSRR.

Its idea depends on introducing another loop to respond fast for the Load sudden change, this loop introduce large miller cap for the stability.
we can say at transient  \[ \Delta I_{load} = \Delta V g gmp = \frac{C_f G_m f R_z \Delta V_{out}}{C_g} gmp \]

so \[ \Delta V_{out} = \frac{\Delta I_{load} C_g}{gmp C_f G_m f R_z} \]

Topologies implemented

a) External Cap LDO
b) Capacitor less LDO

4.2.3 Final design Achieved

External Cap LDO

External Cap model is C= 4uF, ESR=32m, ESI=1.5nH

Figure 4.2.1 Schematic for External Cap topology
Figure 4.2.2 PSRR for External Cap LDO
Capacitor less LDO
4.2.3 Stability for full load for Capacitor less LDO

4.2.4 Stability for no load for Capacitor less LDO
Figure 4.2.5 PSRR for Capacitor less LDO

Figure 4.2.6 Transient simulation form I load=200u to I load_max=2m with 1u raise and fall time
4.2.4 **Specifications Required and Met**

The design of the two topologies achieve a good PSRR with stable circuit under no load condition with programmable Output.

<table>
<thead>
<tr>
<th>Corner</th>
<th>External Cap LDO</th>
<th>Cap Less LDO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gnd Current</td>
<td>67uA</td>
<td>85uA</td>
</tr>
<tr>
<td>worst PSRR</td>
<td>-13.8dB</td>
<td>-8.864dB</td>
</tr>
<tr>
<td>Total Integrated Cap</td>
<td>5pF</td>
<td>8pF</td>
</tr>
<tr>
<td>over Shot</td>
<td>1.3mV</td>
<td>300mV</td>
</tr>
</tbody>
</table>

Table 4.2.1 comparison between External Cap and Cap less LDO

4.2.5 **Conclusion**

External Cap gives better results in all the parameters, however it is more expensive due to the nonintegrated cap, Cap less LDO would be sufficient for Constant loads which is the case for the driver.
Chapter 5: Intermediate Blocks

5.1 CML to CMOS converter

5.1.1 Concept Review

CML to CMOS converter is an intermediate stage used in the CDR loop between the phase interpolator and the PD. It is needed because the phase interpolator which uses CML circuits gives out a small swing that is shifted by DC (common mode output of the CML stage), if this output is used directly to drive the CMOS standard circuits used in the PD, it won't be sufficient to turn off the PDN and the PUN networks present at the CMOS circuits, leading to large leakage and thus static power consumption and degrade noise margins i.e CML to CMOS converter achieves the required swing that fully drives the CMOS stages.

5.1.2 Circuit Review

Final design block diagram:

![Figure 5.1.1 CML to CMOS Converter Block Diagram](image-url)
CML to CMOS stage

It is a differential input, differential output stage that takes two terminals from the phase interpolator and delivers the output two terminals to the stage afterwards which is the amplifier stage, each of the two output terminals will be fed to a series of an amplifier stage and then inverter and buffer stages.

Figure 5.1.2 CML to CMOS Stage

Table 5.1.1 Sizing of CML to CMOS stage

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Length</th>
<th>width</th>
<th>Number of fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M8</td>
<td>60n</td>
<td>2.1u</td>
<td>1</td>
</tr>
<tr>
<td>M2-M3</td>
<td>60n</td>
<td>200n</td>
<td>1</td>
</tr>
<tr>
<td>M14</td>
<td>60n</td>
<td>600n</td>
<td>1</td>
</tr>
</tbody>
</table>
Amplifier stage

IT is two stages of common source amplifiers, it adjusts the DC level of the output signal of the CML to CMOS converter that will be input to the inverters between the amplifier and the buffer stages so as to operate properly through adjusting the gain of the common source amplifier by designing the values of both resistances and the trans-conductance of the transistor.
Figure 5.1.4 Amplifier Stage

Table 5.1.2 Sizing of amplifier stage

<table>
<thead>
<tr>
<th>Transistors</th>
<th>length</th>
<th>width</th>
<th>Number of fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>M16-M26</td>
<td>60n</td>
<td>1.5u</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5.1.3 Passives values

<table>
<thead>
<tr>
<th>Passives</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>resistor</td>
<td>2.2kΩ</td>
</tr>
<tr>
<td>R1</td>
<td>resistor</td>
<td>4.1kΩ</td>
</tr>
</tbody>
</table>
Figure 5.1.5 Amplifier Output

Inverters and Buffer Stages

Figure 5.1.6 Inverter and Buffers Stages
Table 5.1.4 sizing of inverters stage (Upper Branch)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>length</th>
<th>width</th>
<th>Number of fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pmos</td>
<td>60n</td>
<td>470n</td>
<td>1</td>
</tr>
<tr>
<td>Nmos</td>
<td>60n</td>
<td>200n</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5.1.5 Sizing of buffering stage (Lowe Branch)

<table>
<thead>
<tr>
<th>Number of inverter</th>
<th>Length</th>
<th>Width(Wp-Wn)</th>
<th>Number of fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>60n</td>
<td>470n-200n</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>60n</td>
<td>1.88u-800n</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>60n</td>
<td>7.52u-3.2u</td>
<td>1</td>
</tr>
</tbody>
</table>

Inverters stage

The output signal from the amplifier stage will have a large swing and will drive the inverters into saturation region such that the sine wave signal will be clipped up and down and converted into a rail to rail wave to be input to the PD which is required as follows:
Buffer stages

They are used to deliver the square wave generated from the inverters stage to the PD without being distorted by the large capacitance that will load the signal.

Similar outputs will be generated after each stage at the other output terminal.
Table 5.1.6 Readings from the CML to CMOS converter

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1 V</td>
</tr>
<tr>
<td>Supply Current</td>
<td>7.75 mA</td>
</tr>
<tr>
<td>Power</td>
<td>7.75 mW</td>
</tr>
</tbody>
</table>

Figure 5.1.8 Whole Circuit Output
Chapter 6: Additional Blocks

6.1 Variable gain amplifier (VGA)

6.1.1 Concept Review
The variable gain amplifier gives different values of gain and it also can make attenuation, it’s mostly used when we have range of inputs and wants to get one output value for the next block.

6.1.2 Circuit Review
We need a circuit that has high linearity since we work on high frequency and can be easily controlled; we use a source degeneration common source amplifier as in figure 6.1.1.

![source degeneration common source](image-url)

Figure 6.1.1(source degeneration common source)
Bay changing the value of the variable resistance the gain will change so if we control this variable resistance to get the required gain values we can reach our VGA.

6.1.3 **Settled topology**

Figure 6.1.2 shows the design used

![Figure 6.1.2 (VGA design)](image-url)
The transistors are used as on/off switches which are controlled by voltage giving the required gain to the next stage.

6.1.4 Final design Achieved

![Diagram of the VGA](image)

Figure 6.1.3 (schematic of the VGA)

6.1.5 Specifications Required and Met

The required a range from -4dB to 4dB gain
In figure 2.4.2.2 when Q5 is on the gain is 5.75dB, when Q3 is on the gain is 3dB, when Q7 is one the gain is -2dB, when Q8 is on the gain is -4dB, when both Q7 and Q8 are one the gain is 0.5dB.

This figure shows the good linearity of that VGA. Since the input range from 40mV to 250mV, we use these gains to reach the required o/p for the next stage.

6.1.6 Conclusion

The variable gain amplifier could satisfy our required specs
References


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