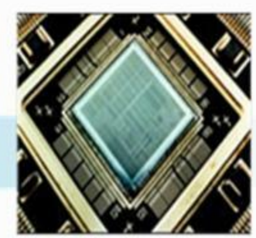
بسم الله الرحمن الرحيم

Design of CMOS Integrated High Performance DC-DC Converter for Low-Power Processor Applications

A presentation for the thesis submitted in partial satisfaction of the requirements for the degree of
Master of Science
By

Eng. Mohamed Saad





Aswan Power Electronics Applications Research Center

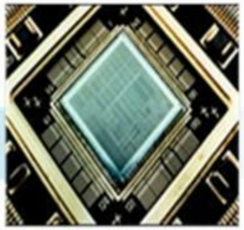
Aswan Faculty of Engineering - South Valley University

تصميم الدوائر المتكاملة لمحولات الجهد المستمر عالية الأداء لتطبيقات معالج منخفض القدرة

رسالة من إحدى متطلبات الحصول على درجة الماجستير فى الهندسة الكهربية
مقدمة من

المهندس. محمد أحمد سعد عبدالحميد





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Introduction

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Evolution in Power Management ICs

❑ Modern consumer electronics:

- Include chips fabricated with most advanced semiconductor technologies.

- These chips are expected to be:
    - **Smaller.**
    - **Faster.**
    - **High functionality.**
    - **Cheaper.**

Evolution in Power Management ICs (Cont..)

- Most consumer electronics are battery-powered.

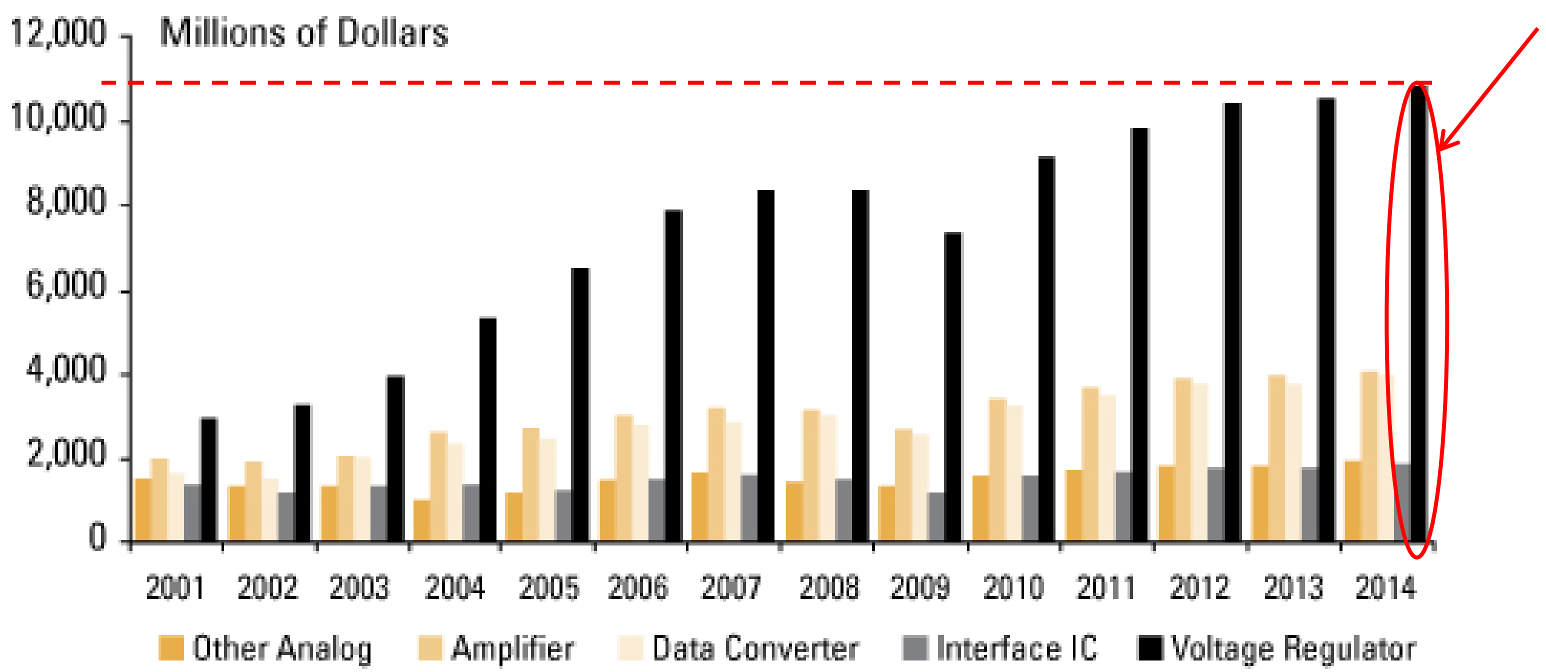
  - Chips with the lowest power consumption to maximize the battery run-time.
    - **Run these chips at the lowest possible supply voltage.**

  - Power Management IC (PMIC) is required to manage voltage and current from a single battery source.

  - PMICs may contain battery management, voltage regulation, battery charging and DC-DC converters.

Evolution in Power Management ICs (Cont..)

- Growing demand of portable applications is a large component of the growth of PMICs revenue.



DC-DC Converters

- Change DC electrical power from one voltage level to another.
  - DC cannot simply be stepped up or down using a transformer.
  - DC-DC converter is the DC equivalent of a transformer.
  - Classified based on conversion method:
    - **Linear voltage converters.**
    - **Switch-mode converters.**

Linear Voltage Converters

- Conversion depends on:
  - Depend on active devices.
    - **Bipolar Junction Transistors.**
    - **Field Effect Transistors.**

- Active device acts like a variable resistor.
- Unneeded power is dissipated in device’s resistance.
- Resistance is adjusted to maintain a constant output voltage.
- Always have Output at lower voltages than the input.

Linear Voltage Converters (Cont..)

❑ Advantages:

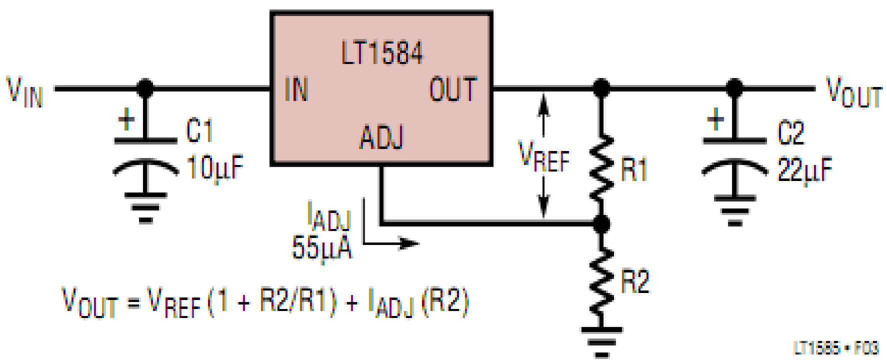
- Inexpensive.
- Simple.
- Small size.
- Low-noise output voltage.

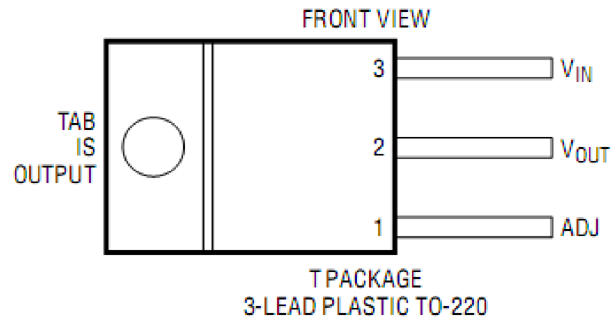
❑ Disadvantages:

- Inefficient.
- Only steps down.
- Suitable just for low-power applications.
- Excessive heat → If load and/or input to output voltage difference are high.

Linear Voltage Converters (Cont..)

Example for linear voltage converter





LT1584 - 7A fast response positive adjustable regulators (Linear Technology)

Switch-Mode Converters

- Conversion depends on:
  - Storing input energy temporarily and then releasing it to the output.
  - Energy storage may be:
    - **In magnetic field element (inductor or transformer)**
    - **In electric field element (capacitor)**
  - Pass element operate as a switch.
  - Pass element switches at a predetermined switching frequency.

Switch-Mode Converters (Cont..)

Advantages:

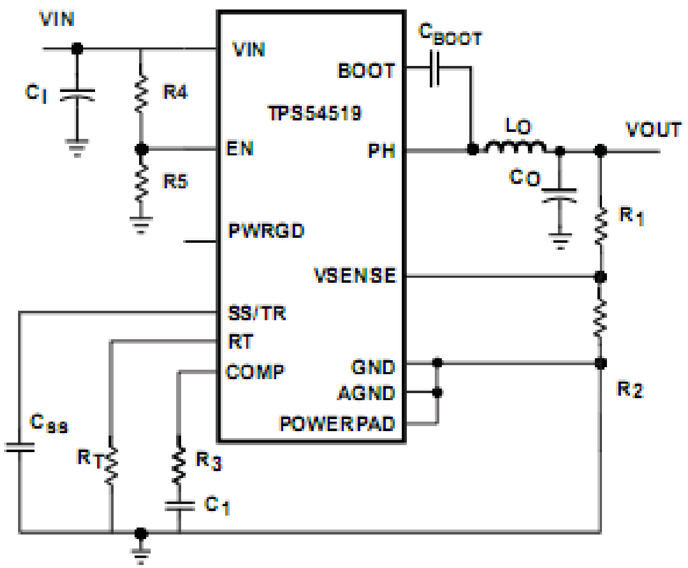
- More power efficient.
- No excessive heat.
- Suitable for low-power / high-power applications.
- Steps up, steps down, and inverts.

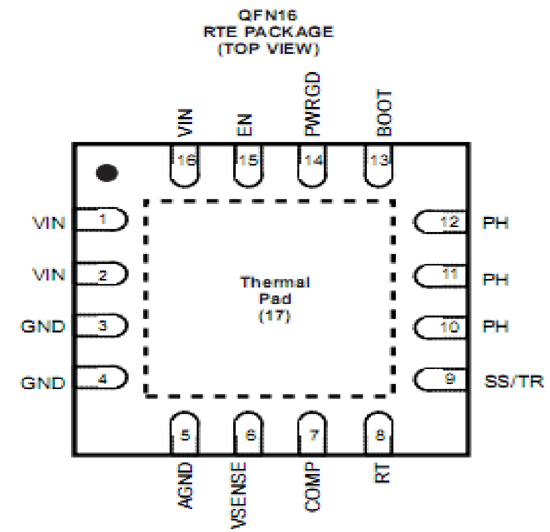
Disadvantages:

- More complicated.
- Larger size.
- Higher cost.
- Higher noise.

Switch-Mode Converters (Cont..)

Example for magnetic type switch-mode converter

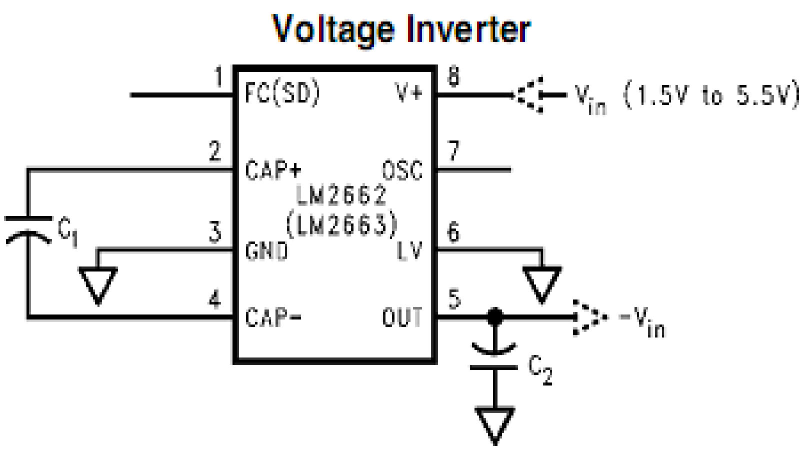


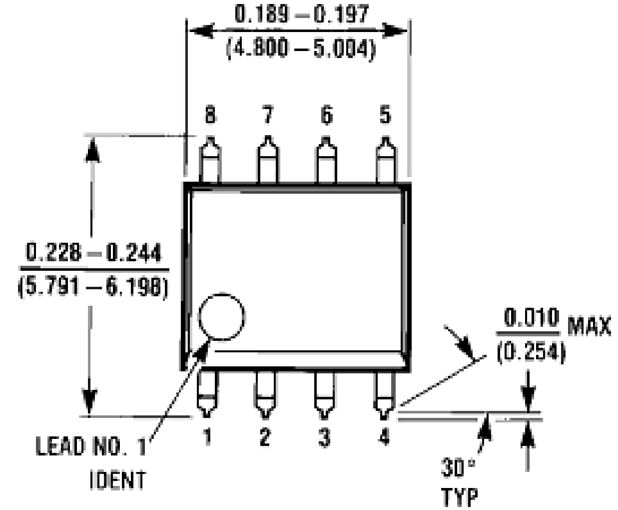


TPS54519 – 5A synchronous step-down converter (Texas Instruments)

Switch-Mode Converters (Cont..)

Example for capacitive type switch-mode converter





LM2662 – Switched capacitor voltage converter
(National Semiconductor)

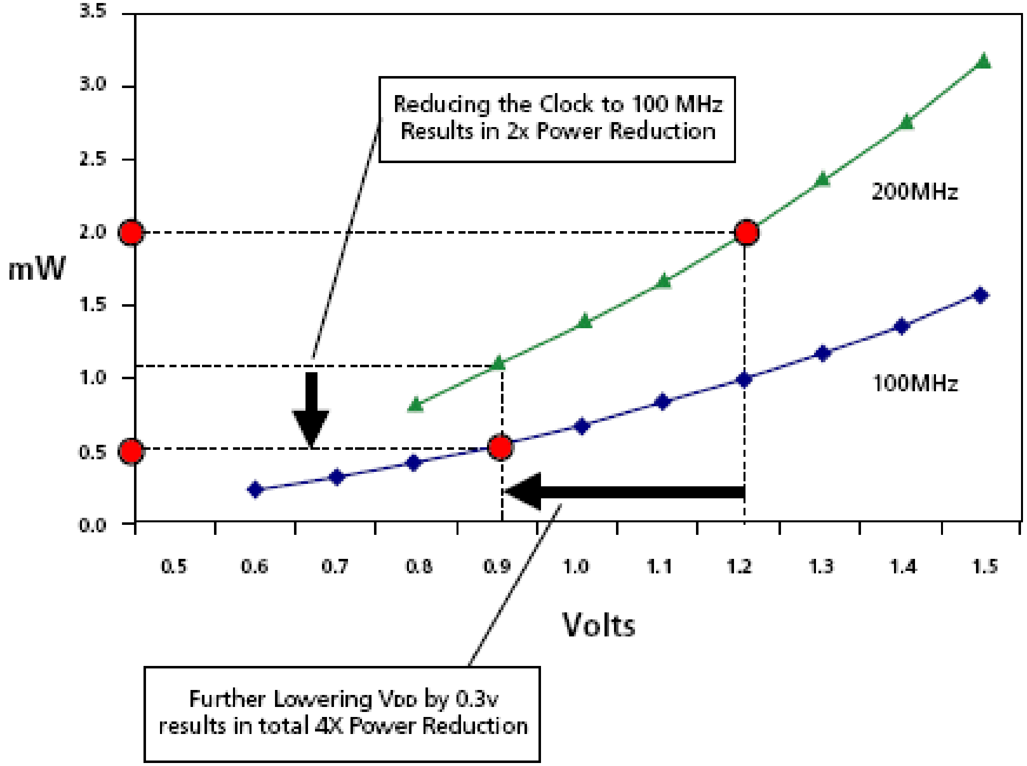
Moore’s Law and Power Supply Challenges

- Increasing demand for computing and communication devices.
  - Smaller processors needed at any portable device.
  - *Process scaling* revolution.
    - **Feature size of a transistor can be reduced.**
    - **Physical area of a chip can be significantly reduced.**
    - **Supply voltage can be scaled too.**

- Moore’s Law
  - Number of transistors on a chip roughly doubles every two years.

Moore's Law and Power Supply Challenges

- For lower power consumption and less heat
  - Processor voltage needs to be scaled.



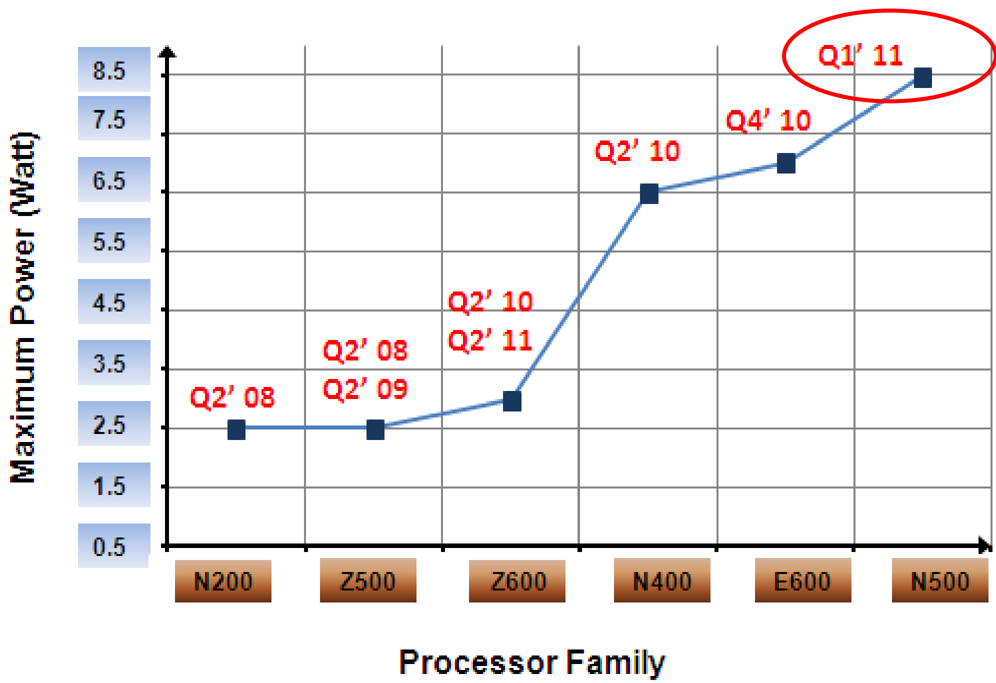
Moore’s Law and Power Supply Challenges (Cont..)

- ❑ Processor supply voltage decreased from 3.3 V to 1.1 V and smaller.
- ❑ More transistors are packed on a single processor chip.
- ❑ Processors’ current draw will increase from 13 A to 50 A.

Big challenge for processors’ power supply

Moore's Law and Power Supply Challenges (Cont..)

Example for low-power processors → Intel Atom ™



- Supply voltage ranges from 0.75 V – 1.2 V
- Relatively high current can (7 A and higher)

Motivation

- ❑ Current consumer electronics demand diverse functionality.

- ❑ Smartphone; as an example; is expected to:
  - Communicate faster.
  - Capture very high resolution photos.
  - Display HD videos and movies.
  - Read PDF files.
  - Sending files via wireless or Bluetooth connection.

It needs very fast and advanced processor

Motivation (Cont..)

- For a processor to do all of these functions:
  - Fabricated using the most advanced technologies.
    - **Supply voltage of modern technologies ranges between 0.75 V and 1.2 V.**
  - Require relatively high currents to operate billions of transistors.

Our goal:

- Design of efficient power supply for those processors.
- Low cost.
- Smaller size compared to solutions available in market.
- Fast transient response.

Thesis Organization

- Chapter 1 : Introduction
- Chapter 2 : Integrated Switched-Capacitor Converter Design
- Chapter 3 : 2 MHz Integrated Buck Converter Design
- Chapter 4 : Integrated Two-Stage Power Supply Design
- Chapter 5 : Design of Linear-Nonlinear Control Technique for Buck Converter
- Chapter 6 : Conclusion and Future Work

Integrated Switched-Capacitor Converter Design

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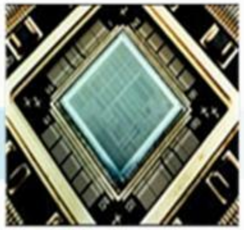


Characterization Parameters for SCC

- It is often confused when selecting between the inductor-based converters and capacitor-based converters.

- It is very important to determine the most effective parameters that characterize SCCs.

- Characterization parameters for SCCs:
  - Output voltage accuracy.
  - Size & Cost.
  - Converter Efficiency.
  - Ripple & Noise.

Characterization Parameters for SCC (Cont..)

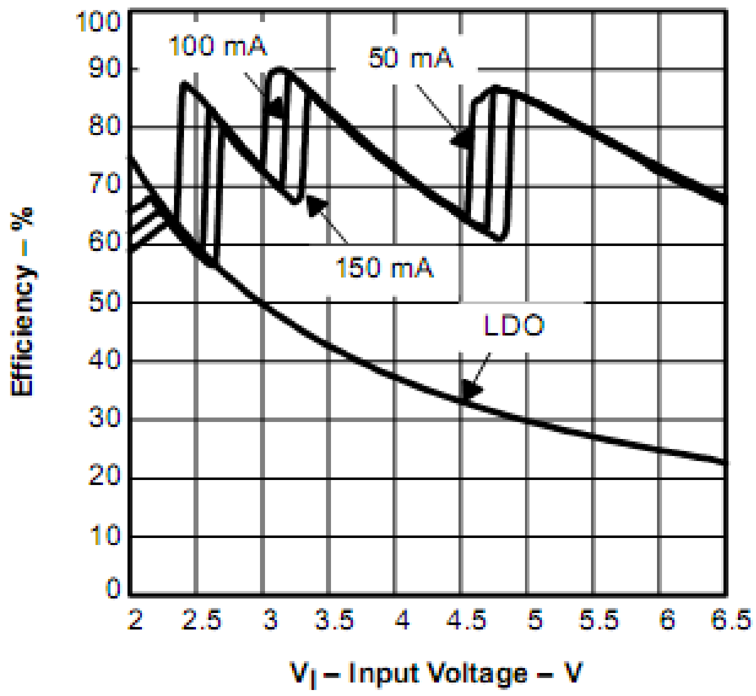
Output Voltage Accuracy

- The tolerance of setting the output voltage at a desired value.
- Output voltage regulation
  - **Closed loop system that monitors the output voltage and continuously modulates the converter power-stage.**
  - **Regulation depends on:**
    - ✓ Reference voltage accuracy.
    - ✓ Feedback voltage accuracy.
    - ✓ Closed loop DC gain.
- Unregulated Output voltage
  - **Output voltage value will change in corresponding to input line and load line.**

Characterization Parameters for SCC (Cont..)

❑ Converter Efficiency

- Long battery life.
- Lower heat dissipation.
- Inductive switching converter is more efficient than SCC.
- Efficiency of SCC depends on their structures and input voltages.
- Multi-mode SCCs can adaptively adjust the conversion ratio to achieve the best efficiency.

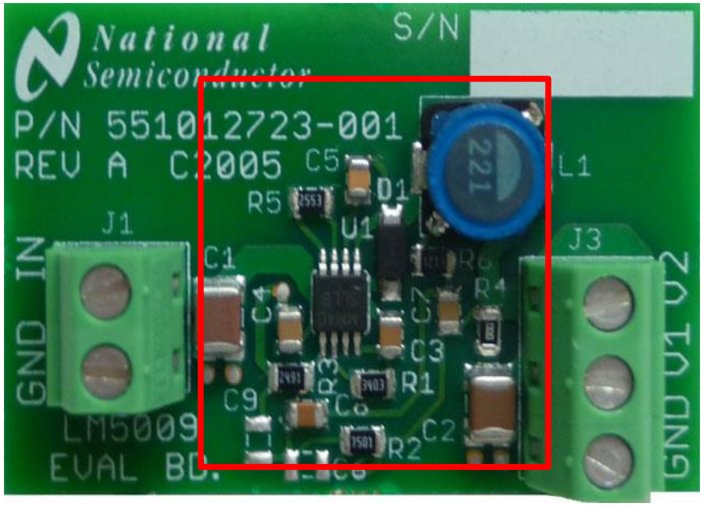


Characterization Parameters for SCC (Cont..)

❑ Size & Cost

- ➢ PCB area requirement of a SCC will be between 30% and 50% smaller than that of inductive switching converter.

90mA switched-capacitor converter

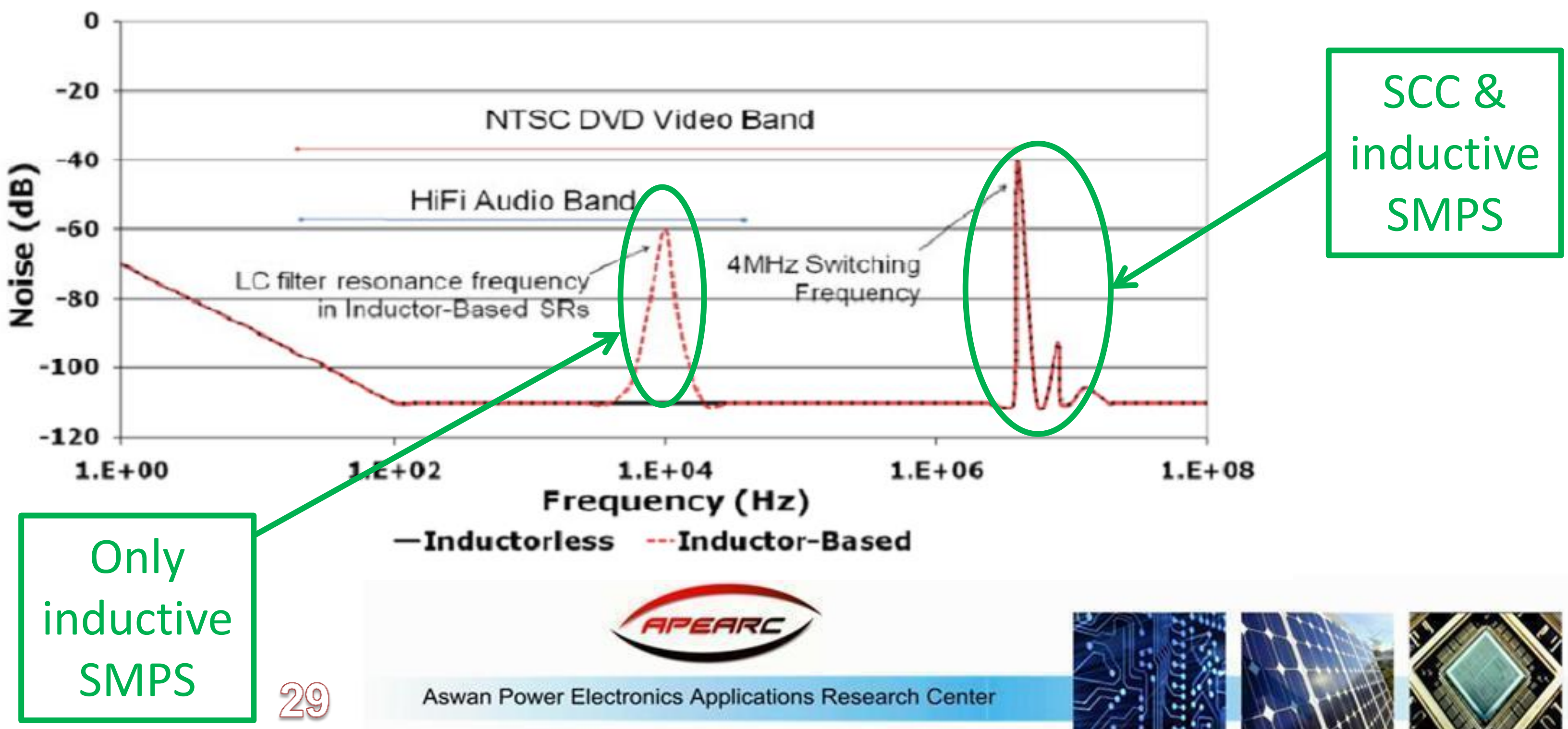


100mA synchronous buck converter

Characterization Parameters for SCC (Cont..)

❑ Ripple & Noise

- SCC is similar to inductive SMPS in ripple generation.
- Noise generation is of SCC is lower than inductive SMPS.



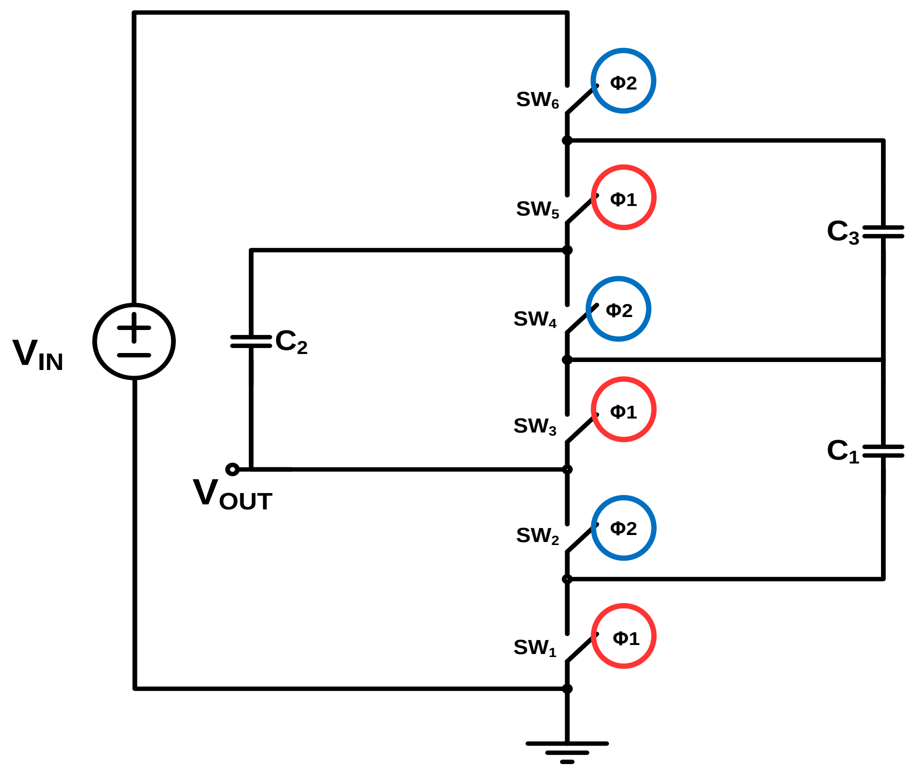
Structure of SCC

- SCC is comprised of array of switches and array of capacitors.
  - Capacitors are called “flying capacitors”.
  - Switching network enables parallel or series arrangement of the flying capacitors.
  - Each switch is turned-on during one or more phases and turned-off in the other phases.
  - Each switching period is divided into two or more non-overlapping phases.
  - The phases are denoted Φ_1, Φ_2, and so on.

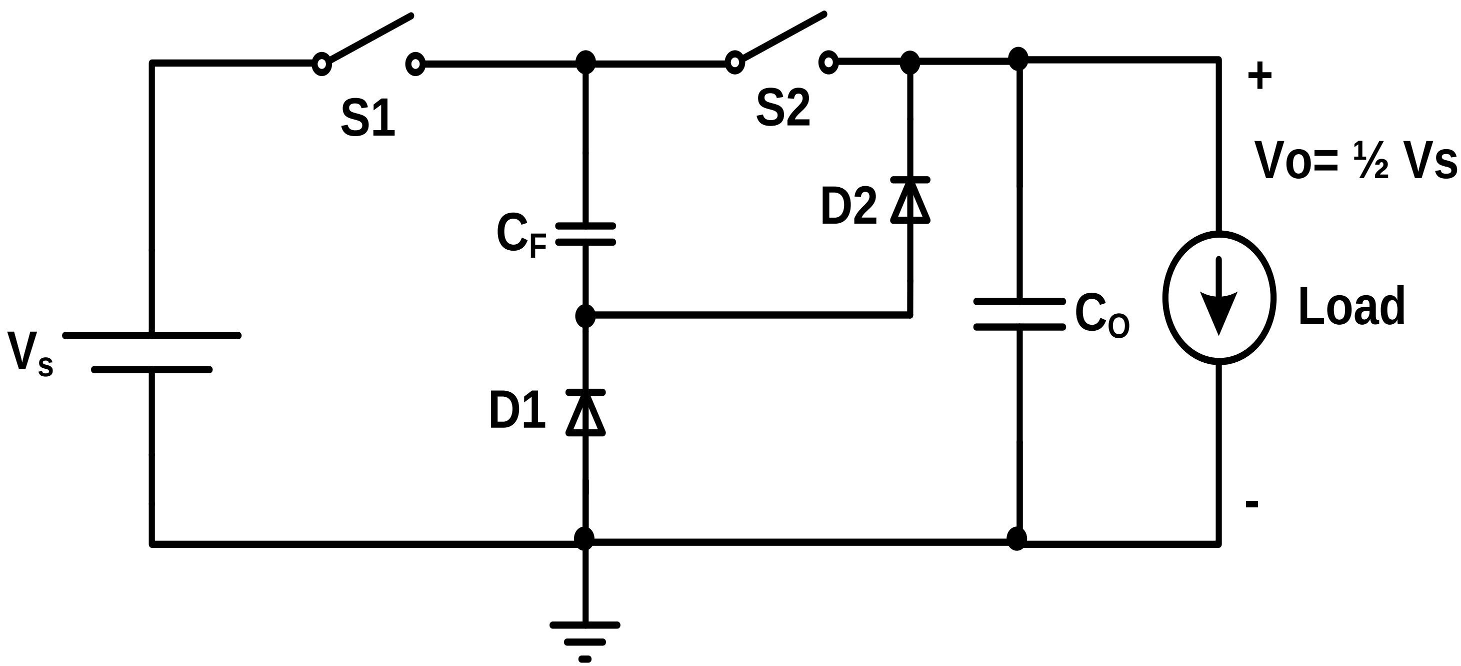
Structure of SCC (Cont..)

❑ Basic switched-capacitor converter

- Turn-on phase of each switch indicated.
- Switching network has two phases.



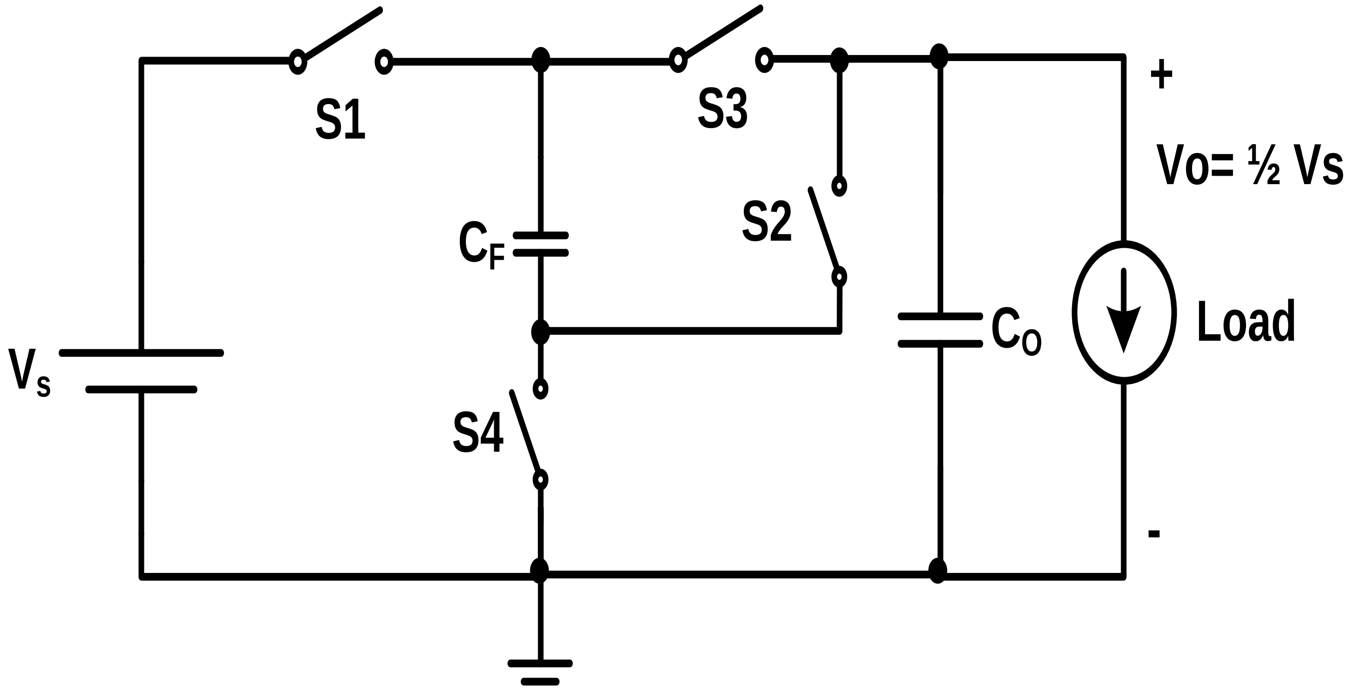
Topology Selection



- **H-bridge Topology**
  - conversion ratio equal to ½ .

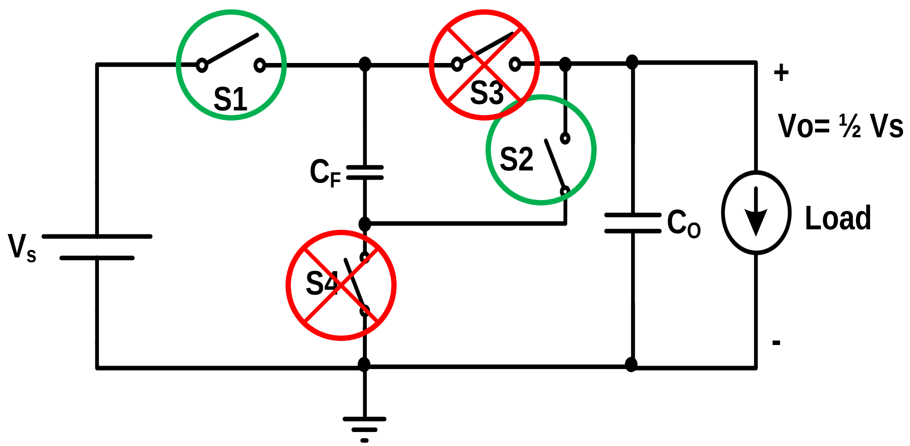
Topology Selection (Cont..)

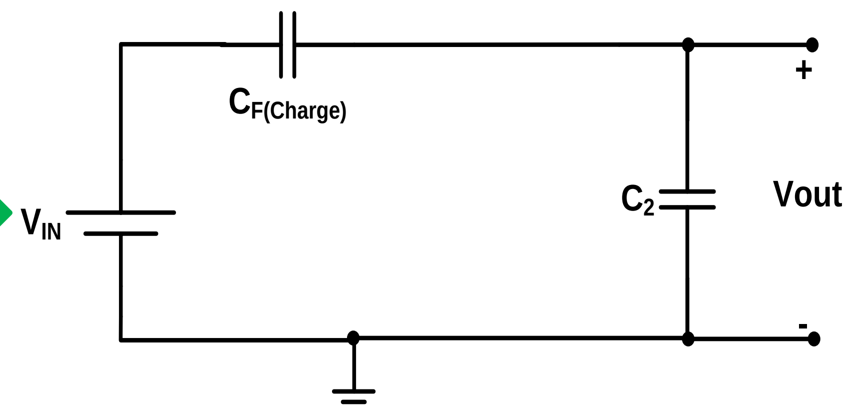
- For integration, the diodes in are replaced by ideal switches.



Topology Selection (Cont..)

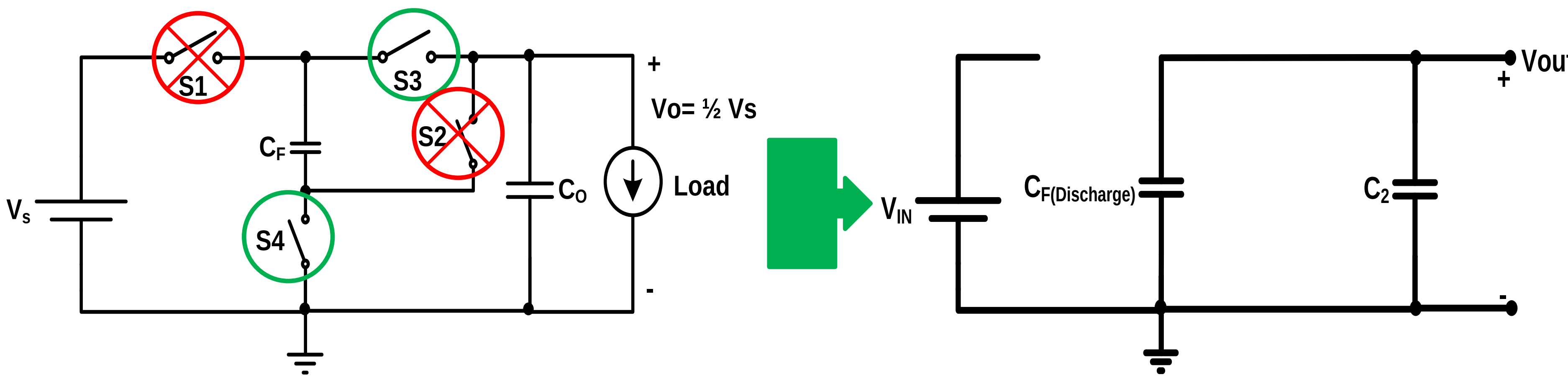
- The topology has two capacitors C_F and C_o.
- Operation can be divided into two phases:
  - First phase ➡ flying capacitor C_F is connected in series with the input source and the capacitor C_o ➡ **(Charging Phase)**





Topology Selection (Cont..)

- <u>Second phase</u> ➡ flying capacitor C_F is connected in parallel with the output capacitor C_o ➡ **(Discharging Phase)**



❑ Output Voltage is unregulated.

- SCC cannot be regulated by modulating duty cycle.

Modeling of SCC

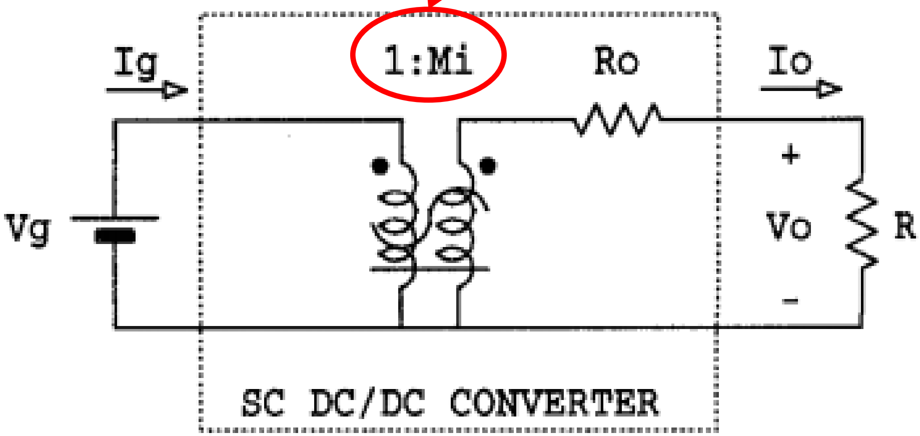
- Series output resistance of SCC:

$$R_O = \frac{1}{fC_F}$$

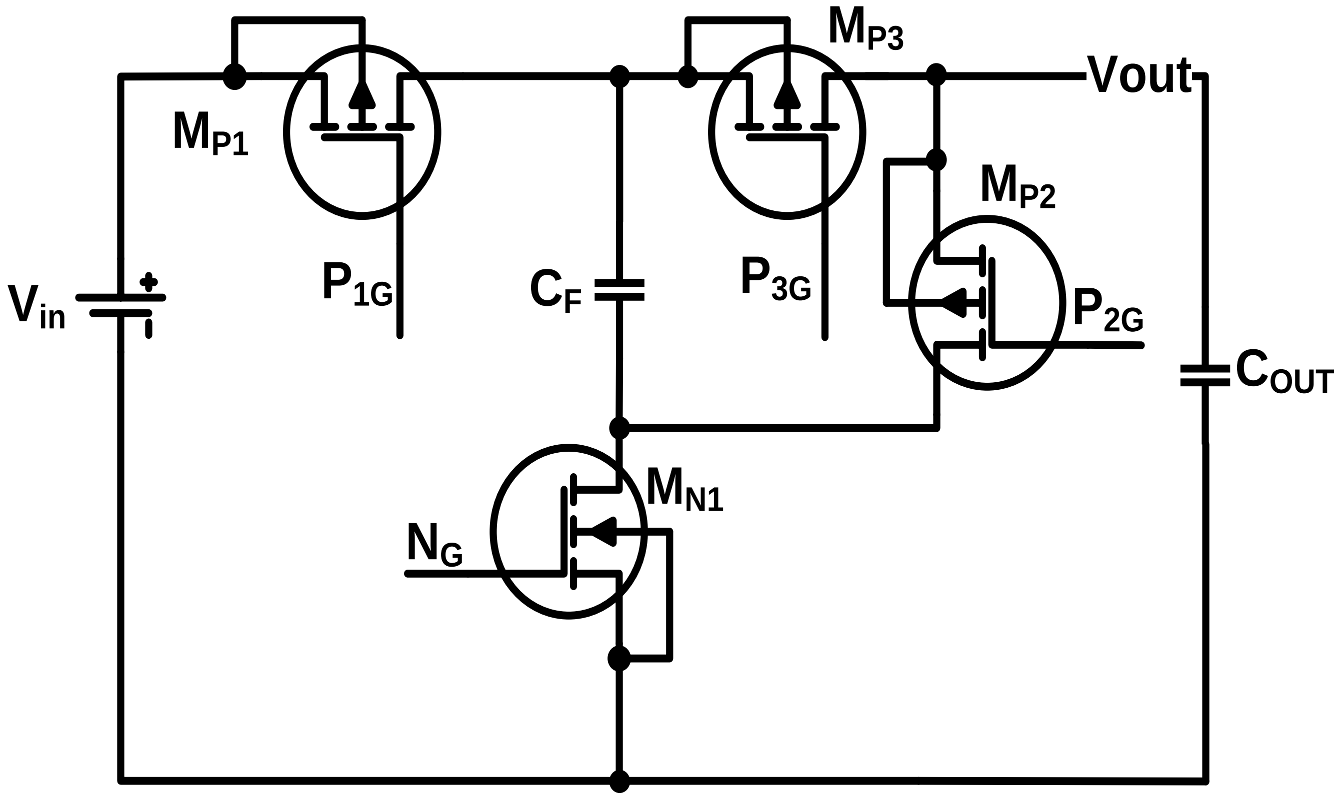
- Equation doesn't include non-ideality effects.

- Non-ideality effects include:
  - Switches' on-resistance.
  - Capacitors' ESR.

Turns ratio = ideal conversion ratio

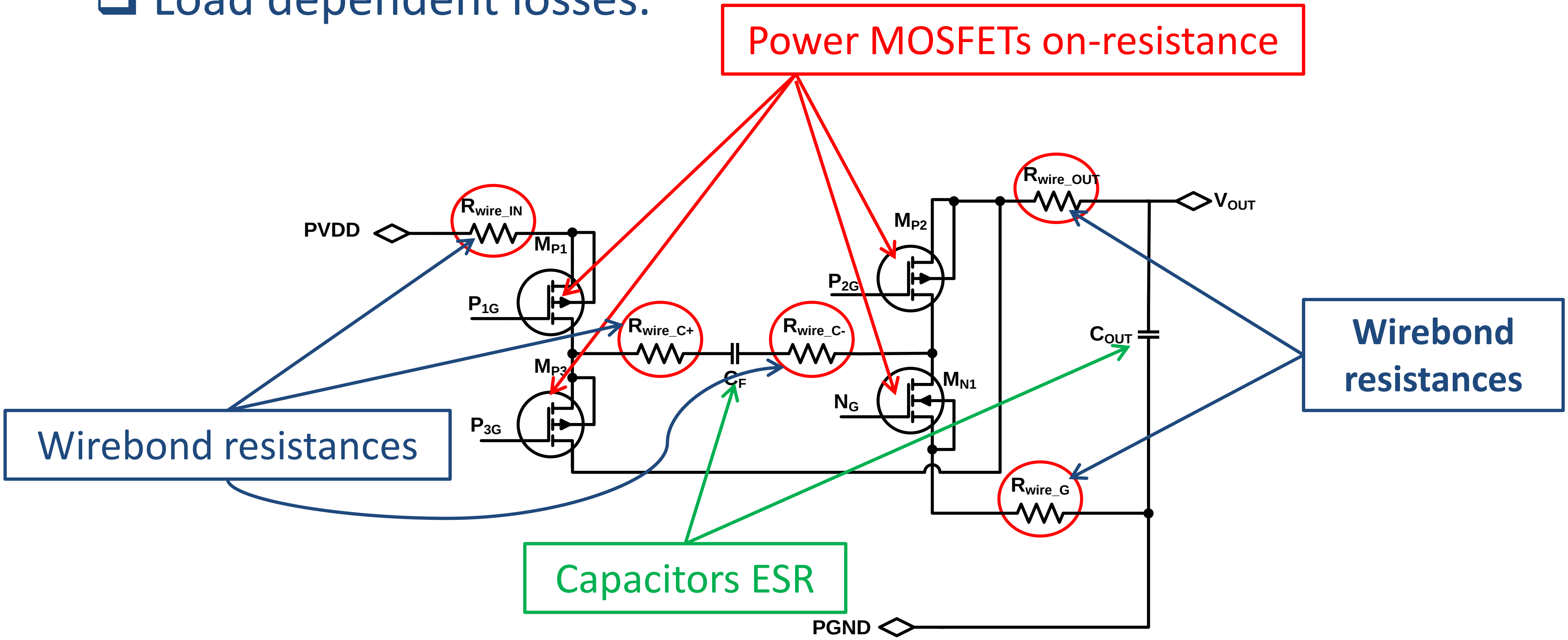


CMOS Realization of Selected SCC



Power Losses in SCC

- Load dependent losses.



Power Losses in SCC (Cont..)

- Switching frequency dependent losses.
  - MOSFET Switching Losses.
    - Power loss during turn-on and turn-off of Power MOSFETs.
  - Gate Drive Losses.
    - Power consumed to charge the gates' capacitances of power MOSFETs.
    - Gate-drive loss is independent of load current.

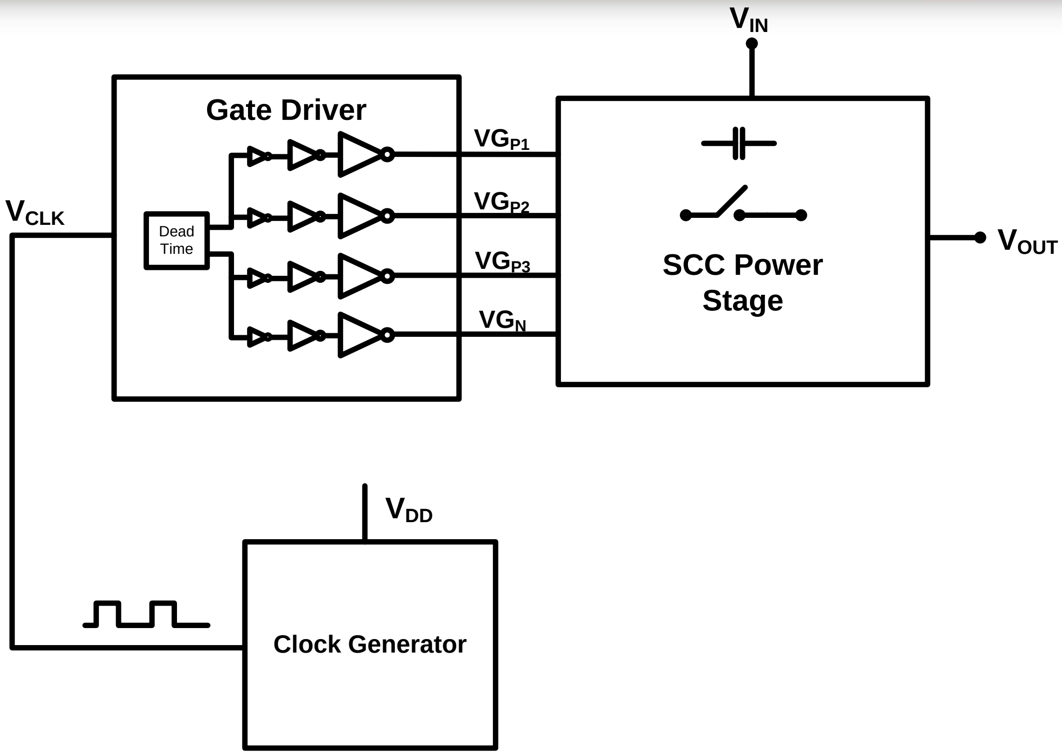
$$P_{GD} = Q_g . V_{Driver} . F_{SW}$$

Power Losses in SCC (Cont..)

❑ Static Power Loss.

- Also called "Quiescent Power Loss".
- Independent on neither frequency nor load.
  - **Always has a fixed value.**
- Comes from the quiescent current required to operate the controller circuits.
- Quiescent power loss is low compared to the other losses in the converter.
- Significant effect at light loads.

Design of High Efficiency SCC



- ❑ Optimized to convert a 6 V into 3 V with 2 A nominal output current.
- ❑ Converter is designed using 0.25 µm CMOS technology using LV devices.

Power Stage Design

❑ Capacitors selection

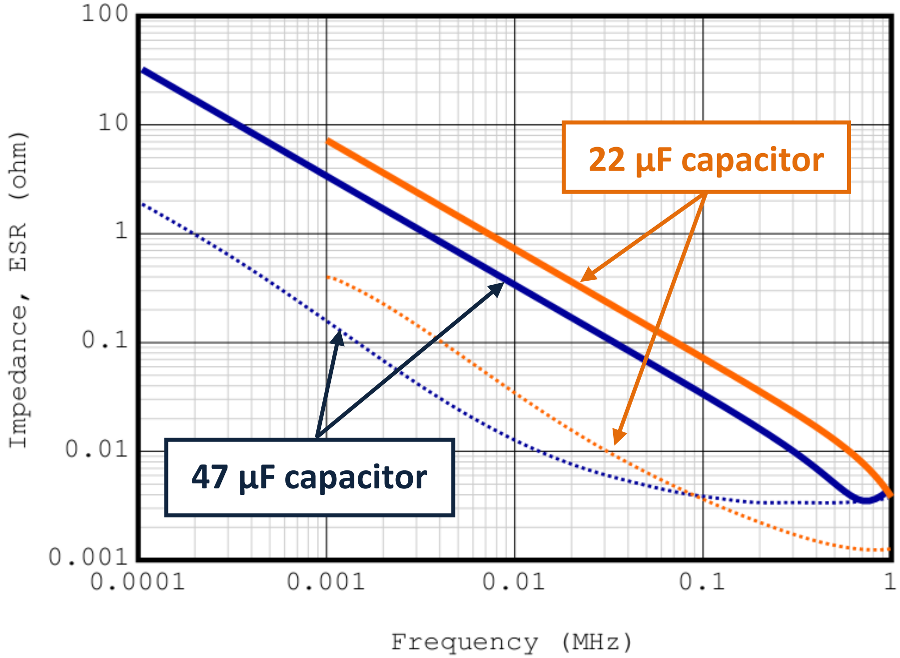
➢ For the flying capacitor C_F:

- Configuration of two parallel capacitors consists of a 47 µF 1206 capacitor in parallel with a 22 µF 0805 capacitor.
- Paralleling more than one capacitor, minimizes the ESR value of the configuration.
- Help in minimizing the output series resistance of the SCC.

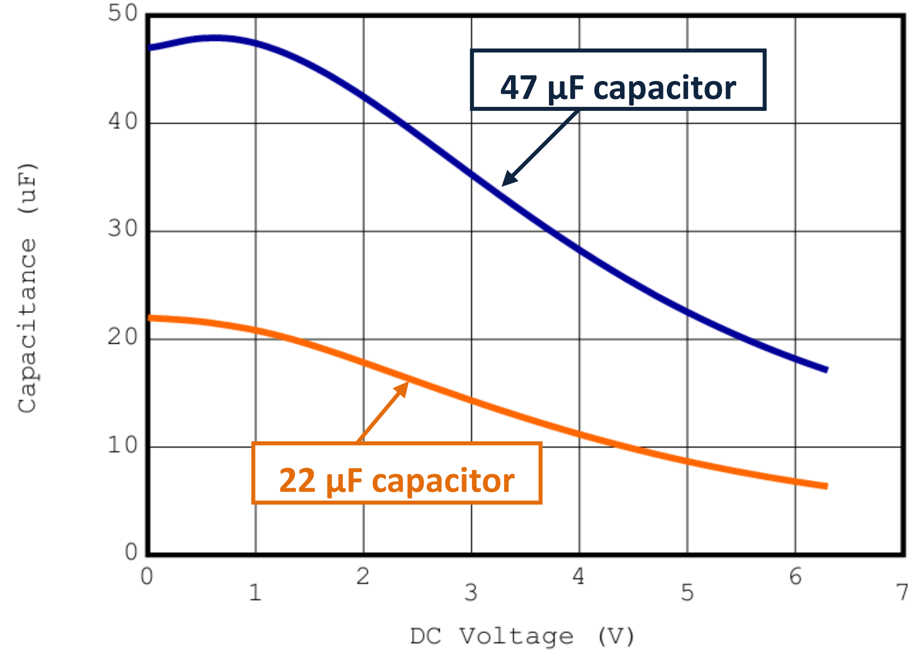
Power Stage Design (Cont..)

❑ Capacitors selection

Impedance and ESR



Capacitance vs. DC biasing



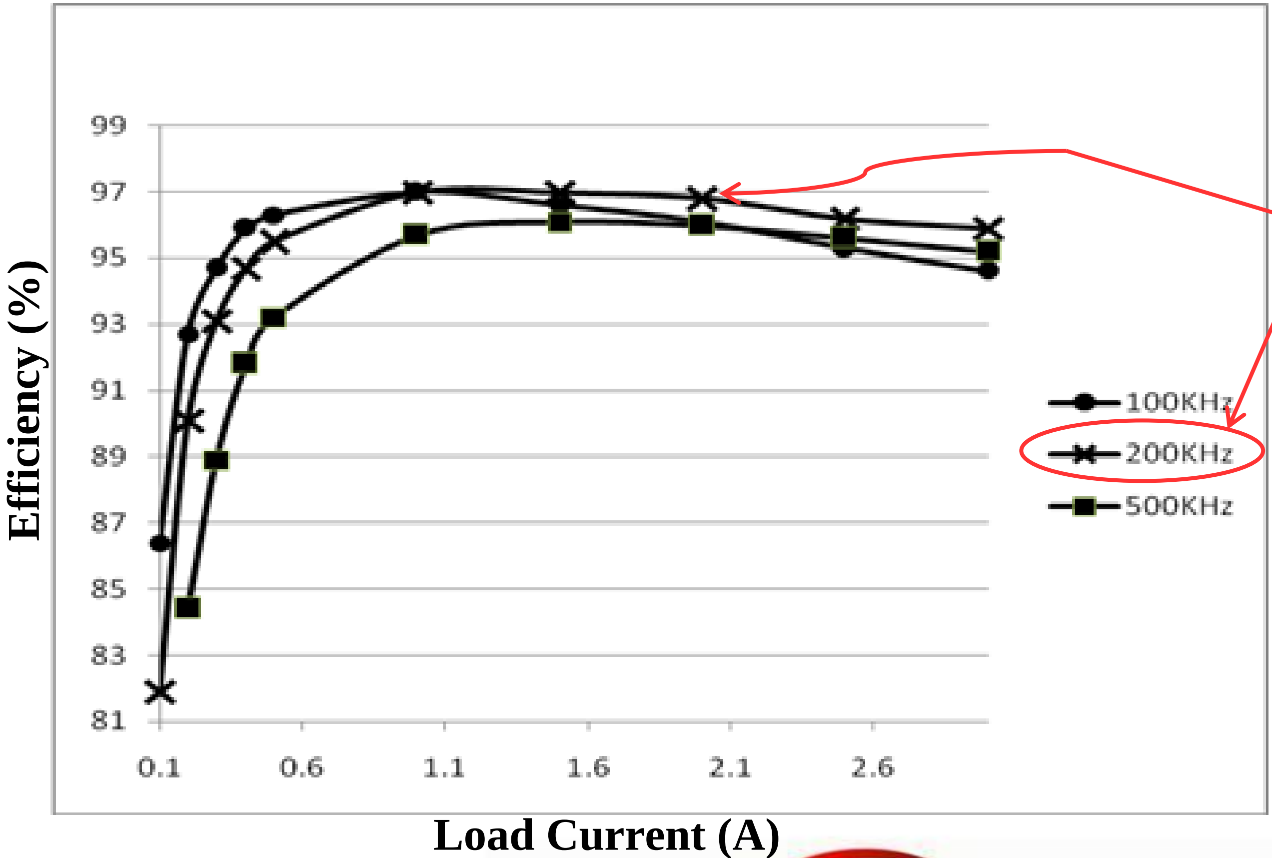
Power Stage Design (Cont..)

❑ Switching Frequency Selection

- Higher switching frequency leads to lower R_O.
  - R_o is inversely proportional to f_s.
  - Lower conduction losses.
- However, high switching frequency increase switching losses.
  - Switching losses is proportional to f_s.
- Optimum switching frequency should be selected.
  - at which the conduction and switching losses are equal.
- <u>To select the optimum switching frequency:</u>
  - A scan for the resulted efficiency is applied at different frequencies.

Power Stage Design (Cont..)

@ V_{IN}= 6V, V_{out} ≈ 3V, and MOSFET widths =160 mm



Highest efficiency at f_s = 200KHz

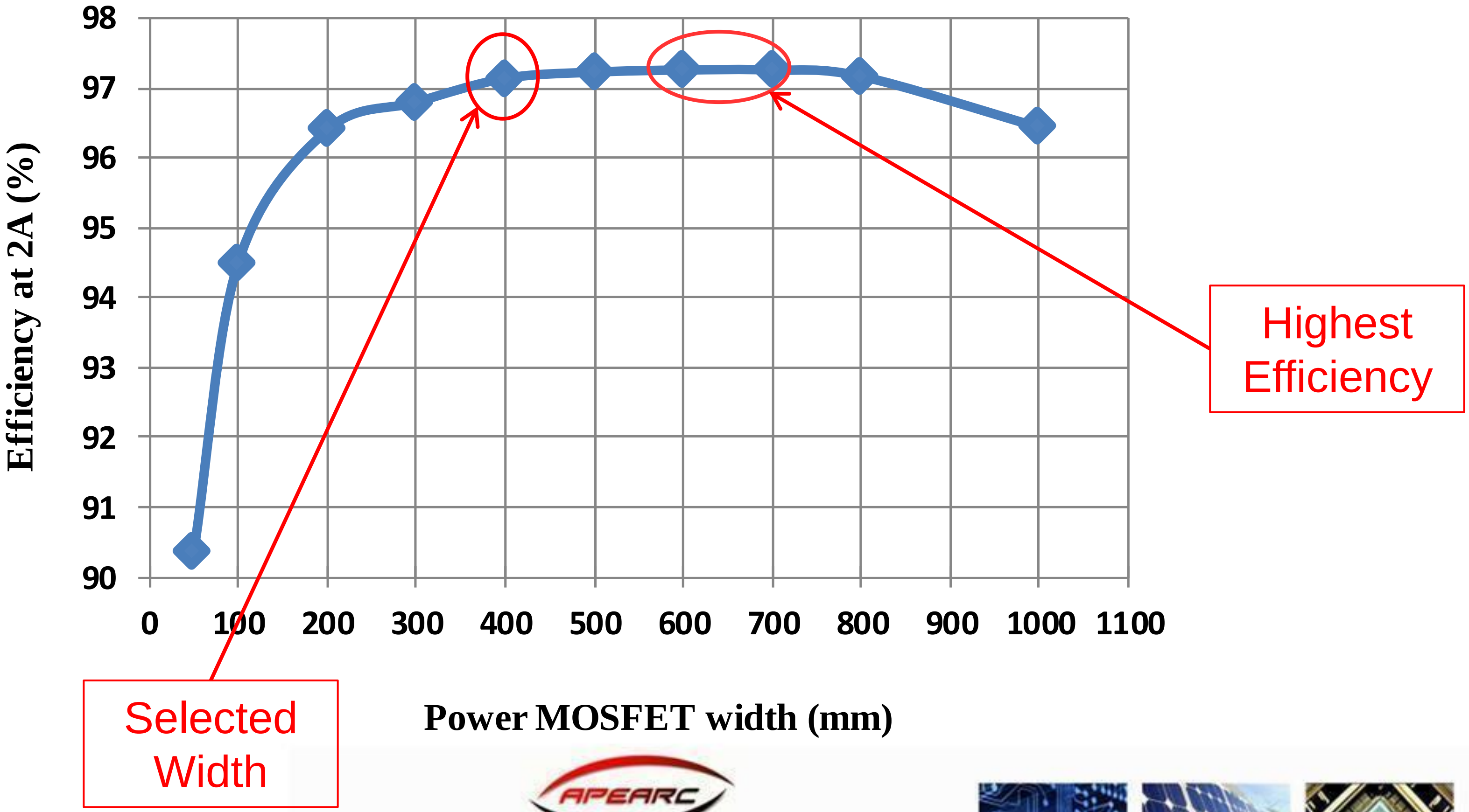
Power Stage Design (Cont..)

❑ Power MOSFETs Design

- Designing the width of each Power switch.
- Switch on-resistance is inversely proportional to the MOSFET width.
  - Minimum conduction losses require minimum on-resistance.
- Parasitic capacitances is directly proportional to the MOSFET width.
  - Minimum switching losses require minimum parasitic capacitances.
- To get maximum efficiency from a converter, an optimum width should be selected.
  - At which the conduction losses and switching losses can reach a minimum value

Power Stage Design (Cont..)

- Width of PMOS MOSFETs should be 2.5 higher than NMOS MOSFET



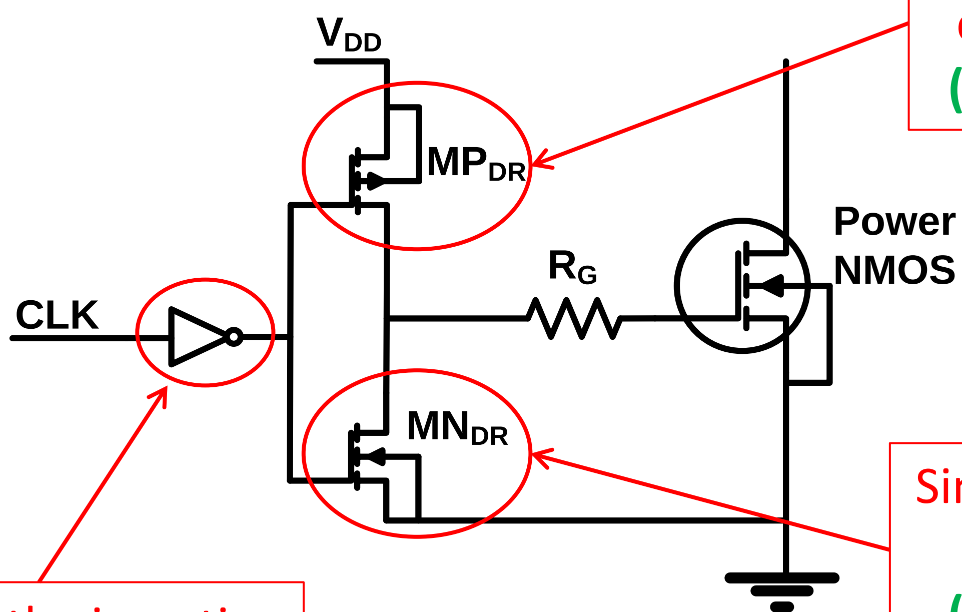
Gate Drive Design

- ❑ Parasitic capacitances value is high for a power MOSFET.
  - ➢ Act as capacitive load for the circuit that produces the gate signal for the MOSFET.
- ❑ Gate-drive circuit is used to drive the gate capacitance of the associated MOSFET.
  - ➢ Fast turning-on and turning-off power MOSFETs.
- ❑ Gate-drive effectiveness is determined by:
  - ➢ How fast the gate capacitances are charged and discharged.

Gate Drive Design (Cont..)

- The most popular drive circuits for driving MOSFETs is CMOS totem-pole driver.

Supply the current to charge gate capacitances **(Turn-on Power MOSFET)**

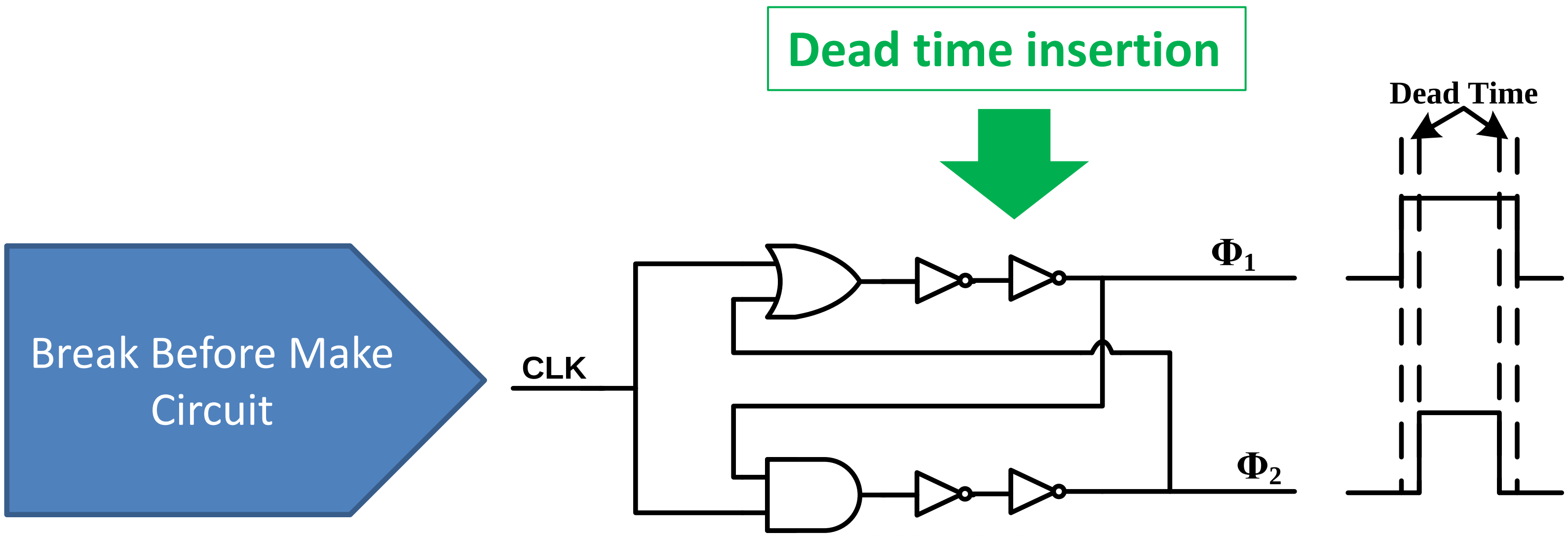


Sink the current to discharge gate capacitances **(Turn-on Power MOSFET)**

To cancel the inverting property of driver

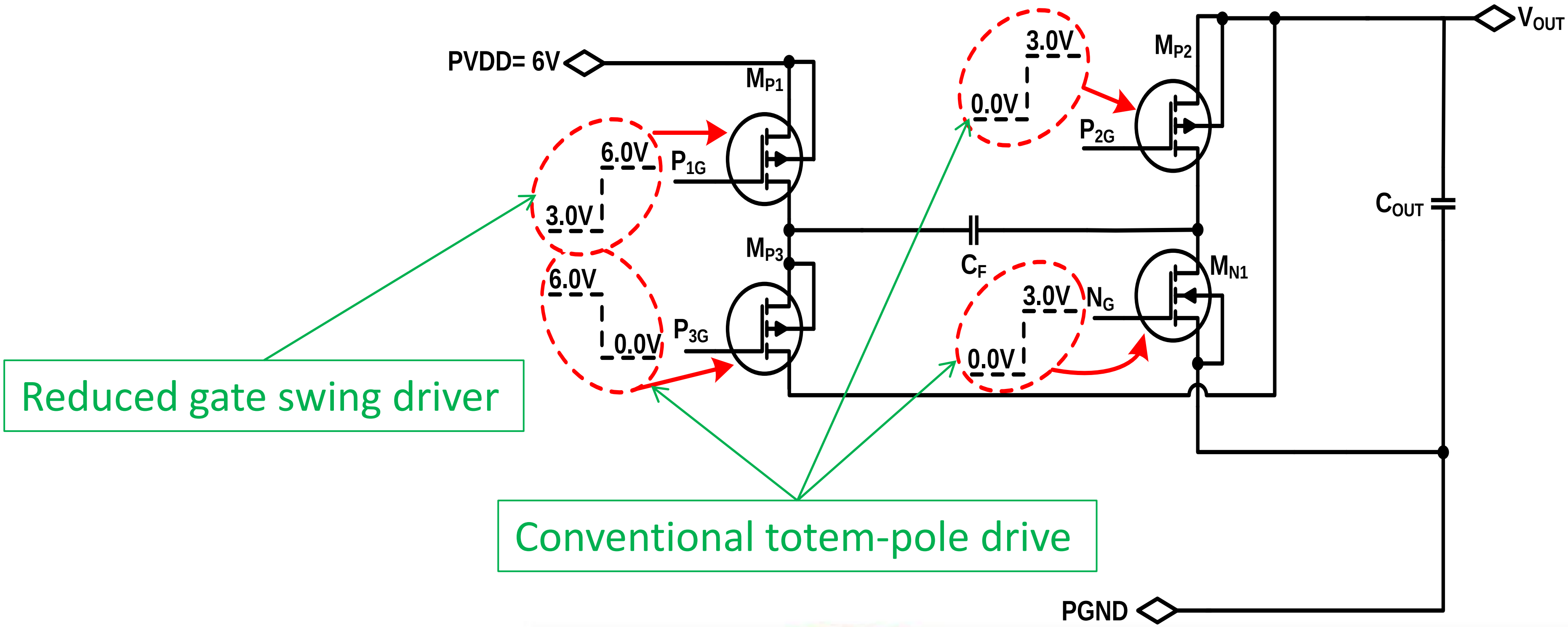
Gate Drive Design (Cont..)

- Turning-on two power MOSFETs from different phases creates
  - Shoot-through problem.
  - Large spikes on output voltage.



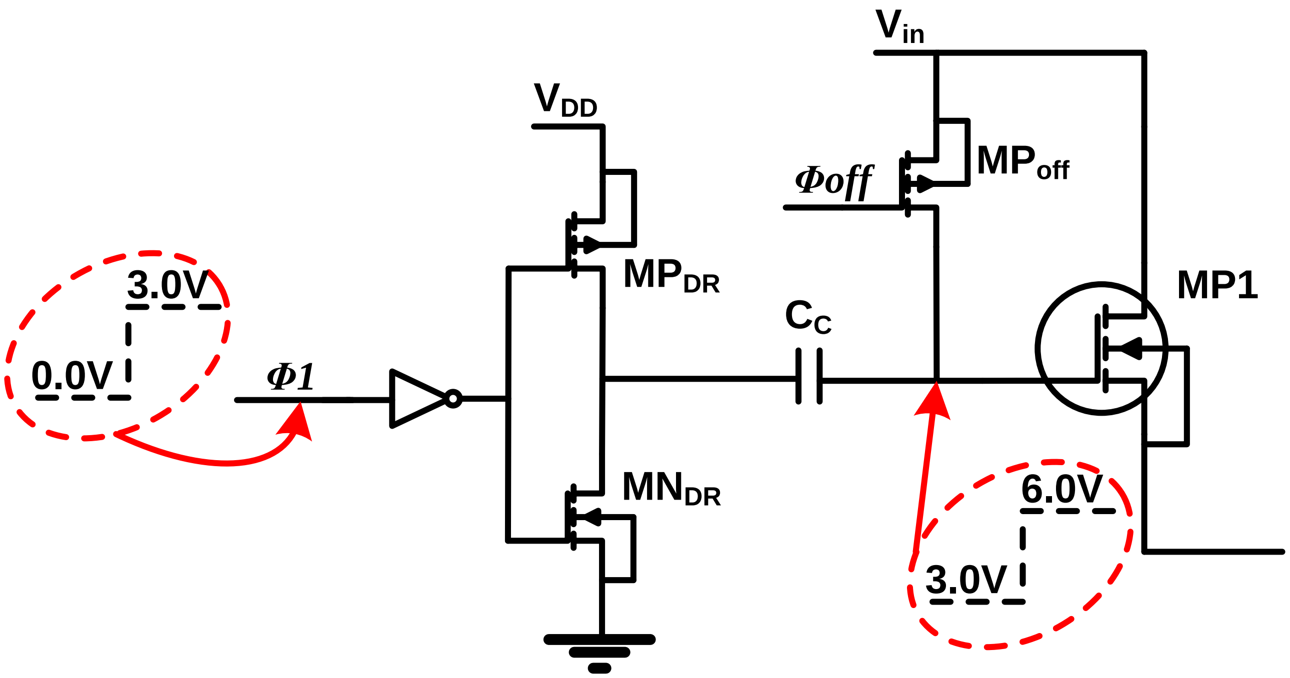
Gate Drive Design (Cont..)

- Driving voltages for each MOSFET



Gate Drive Design (Cont..)

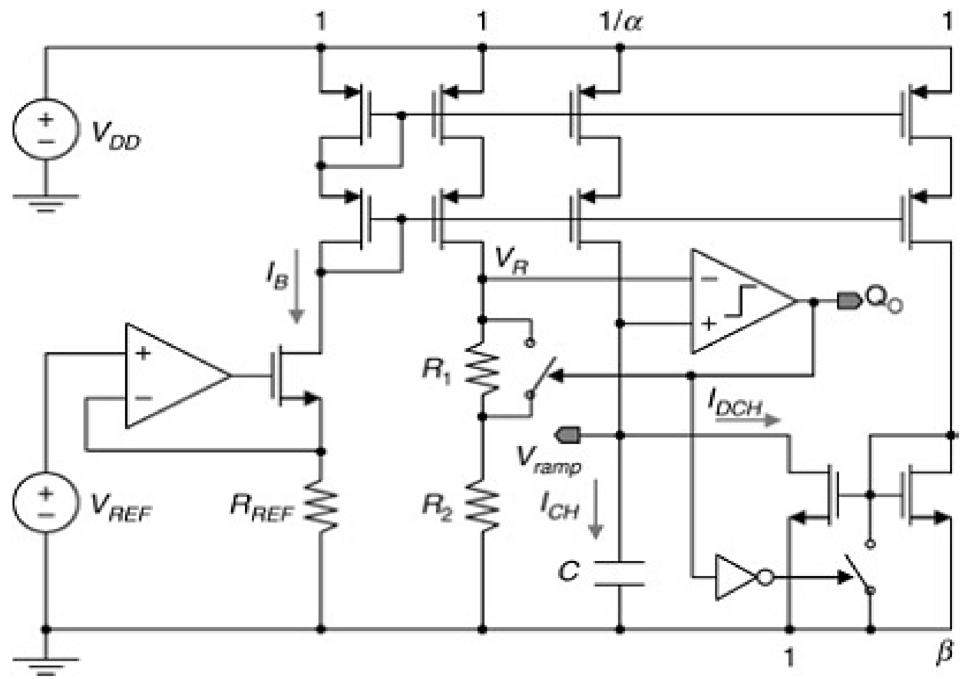
- Reduced Gate swing driver



Clock Generator Design

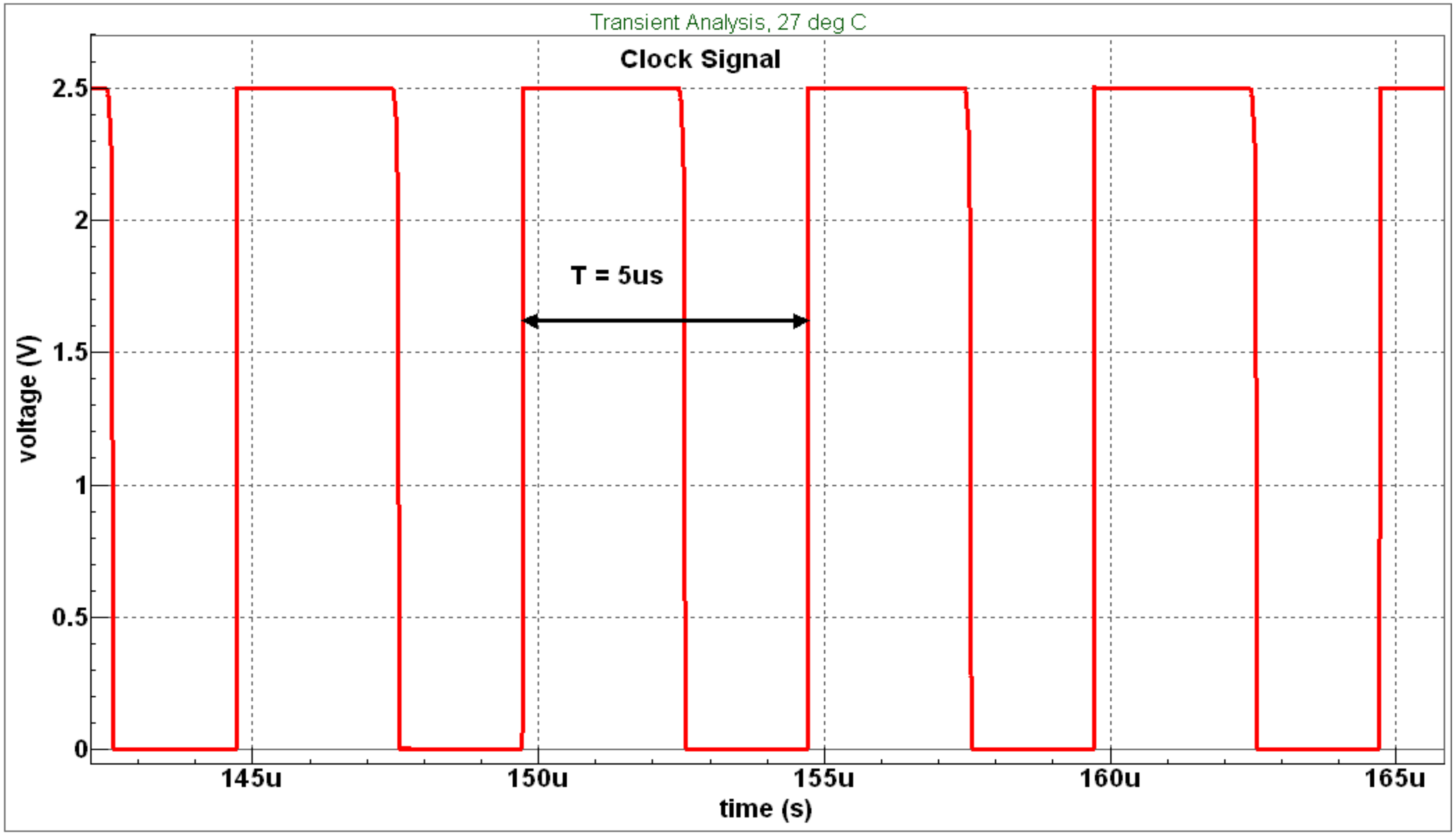
❑ Main idea of the clock generator:

- Charge a capacitor with a constant current.
- Capacitor voltage is compared to constant high and low reference voltages.
- Clock frequency adjusted by:
  - Capacitor Value.
  - Charging current value.
  - High and low reference voltages.



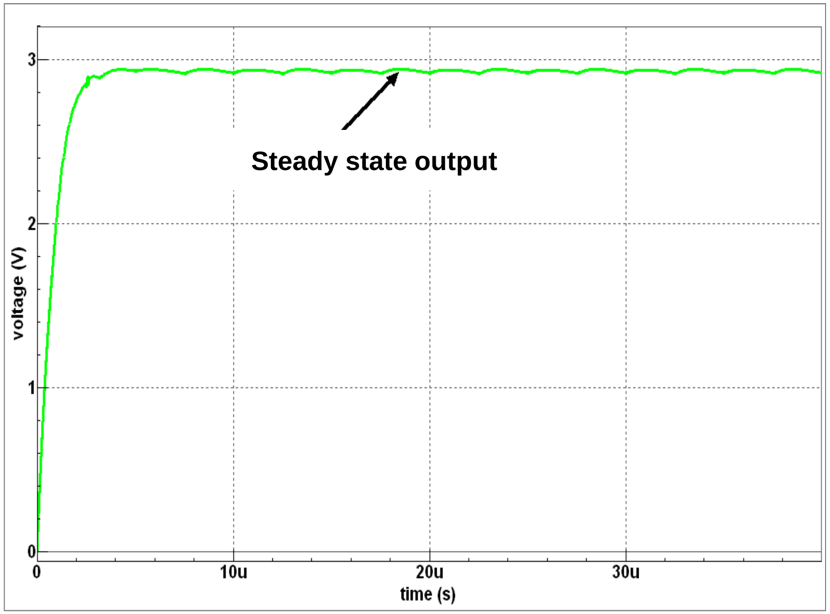
Clock Generator Design (Cont..)

Clock Signal

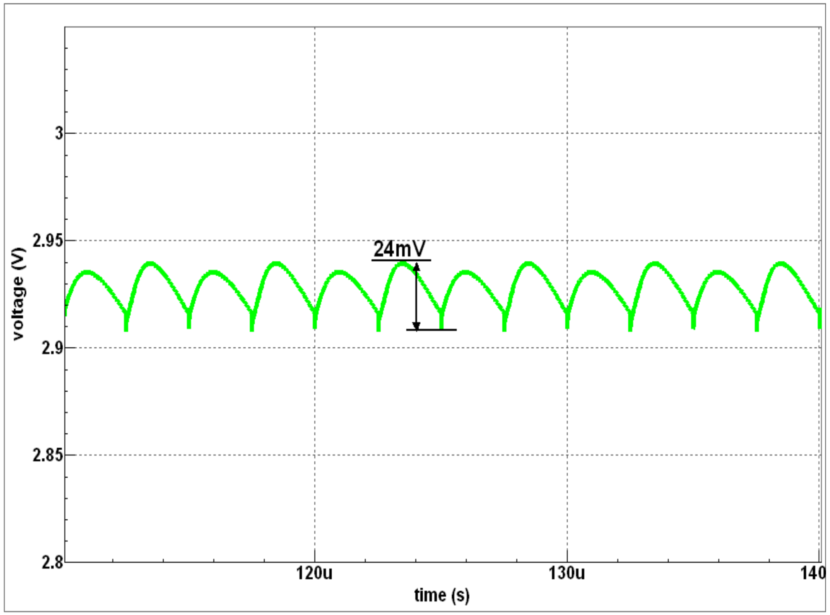


SCC Integration and Simulation Result

Output average value ≈ 2.94 V

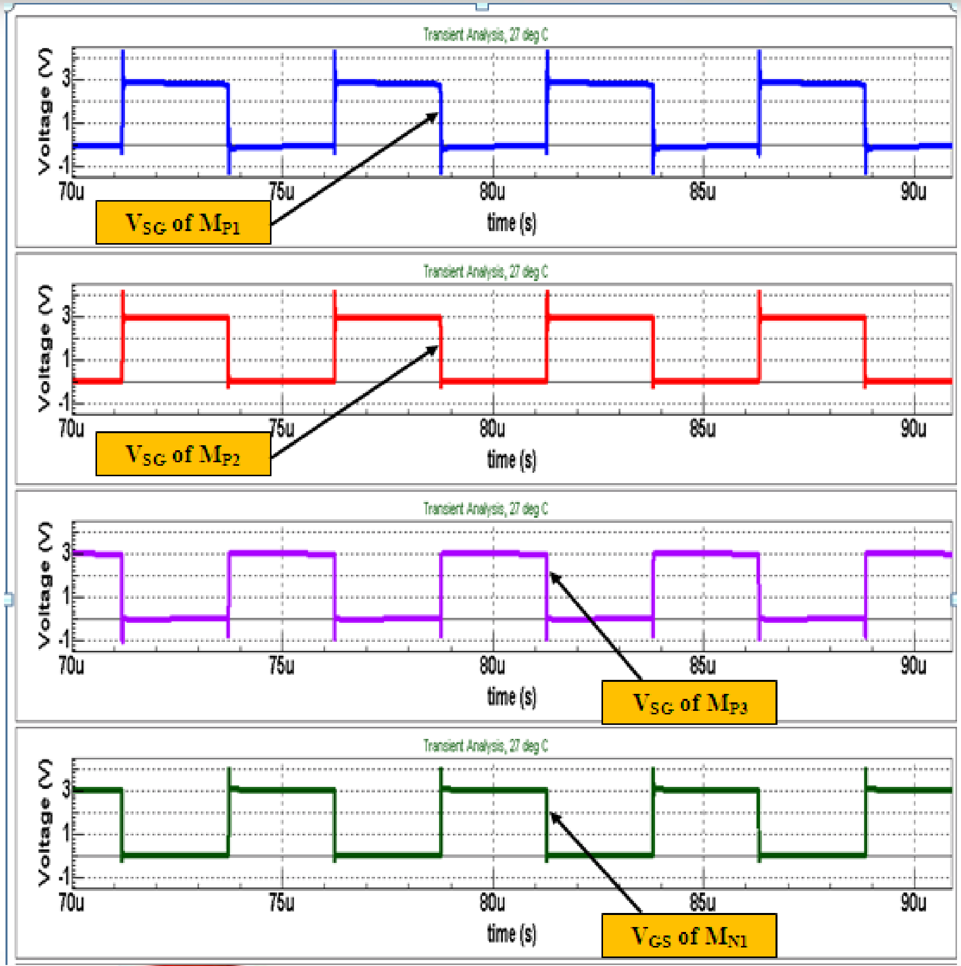


Output Ripple = 24 mV (< 1%)



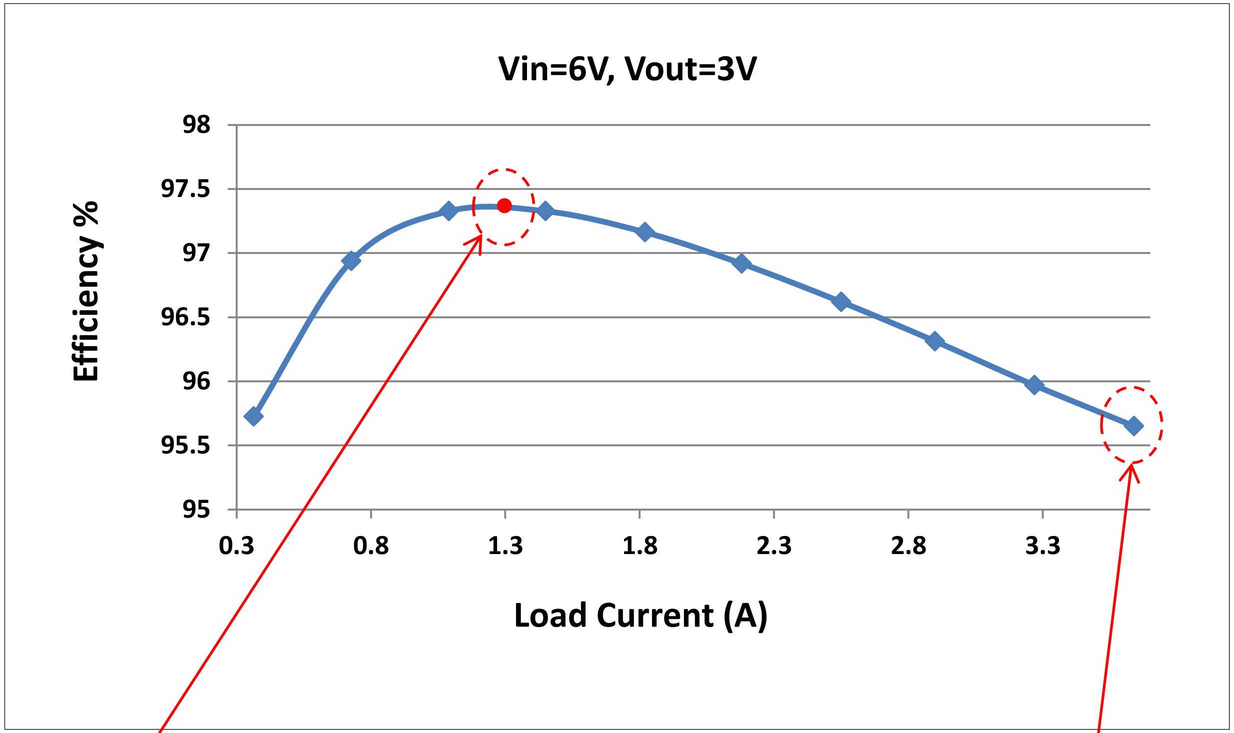
SCC Integration and Simulation Result (Cont..)

Gate-source signals of the four Power MOSFETs



SCC Integration and Simulation Result (Cont..)

- Efficiency of designed SCC



Efficiency at maximum current= 95.7%

Maximum Efficiency = 97.3%

2MHz Integrated Buck Converter Design

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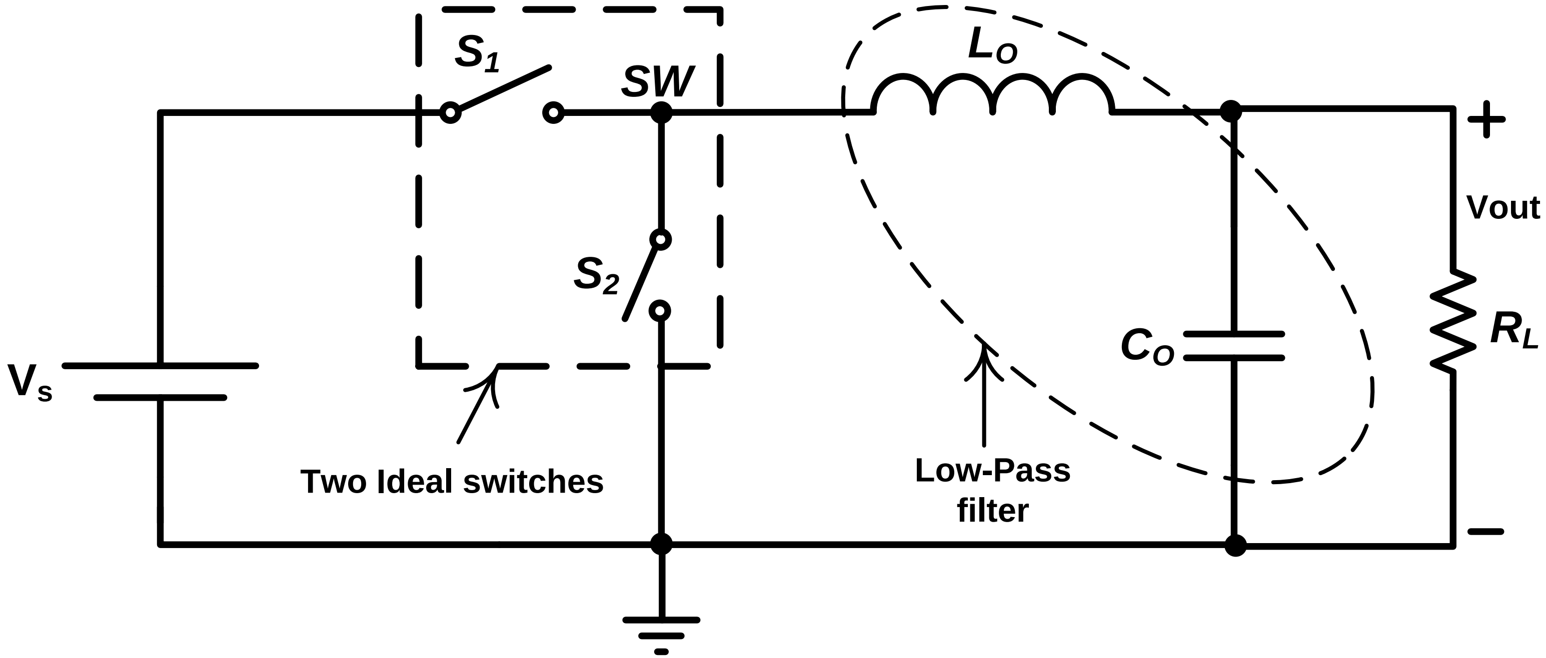
Operation Theory of Buck Converter

❑ Buck Converter ideal circuit:

- Two ideal switches followed by LC low-pass filter

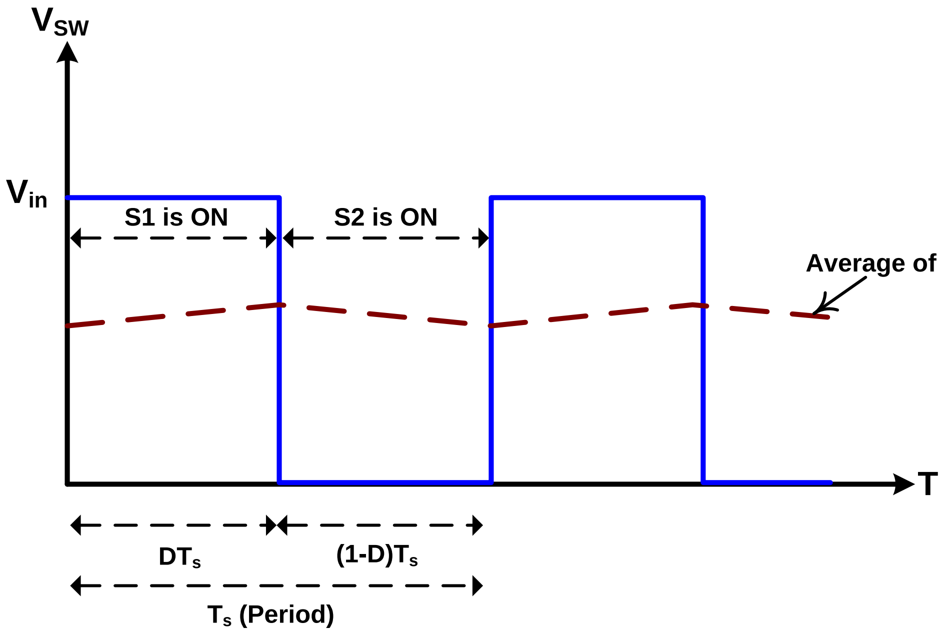


Operation Theory of Buck Converter (Cont..)

❑ Voltage at switching node

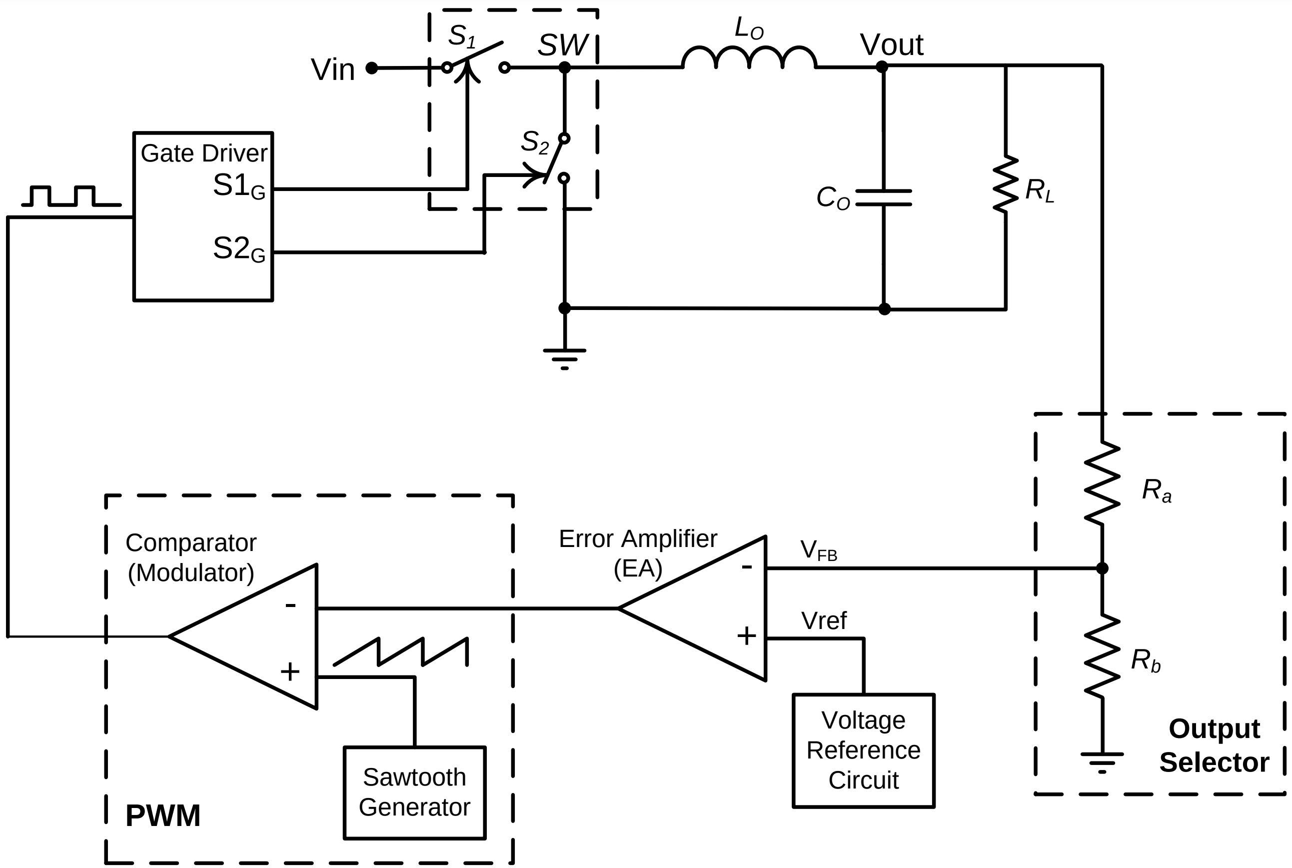
- Input-output relation:

$$V_{OUT} = D.V_{IN}$$



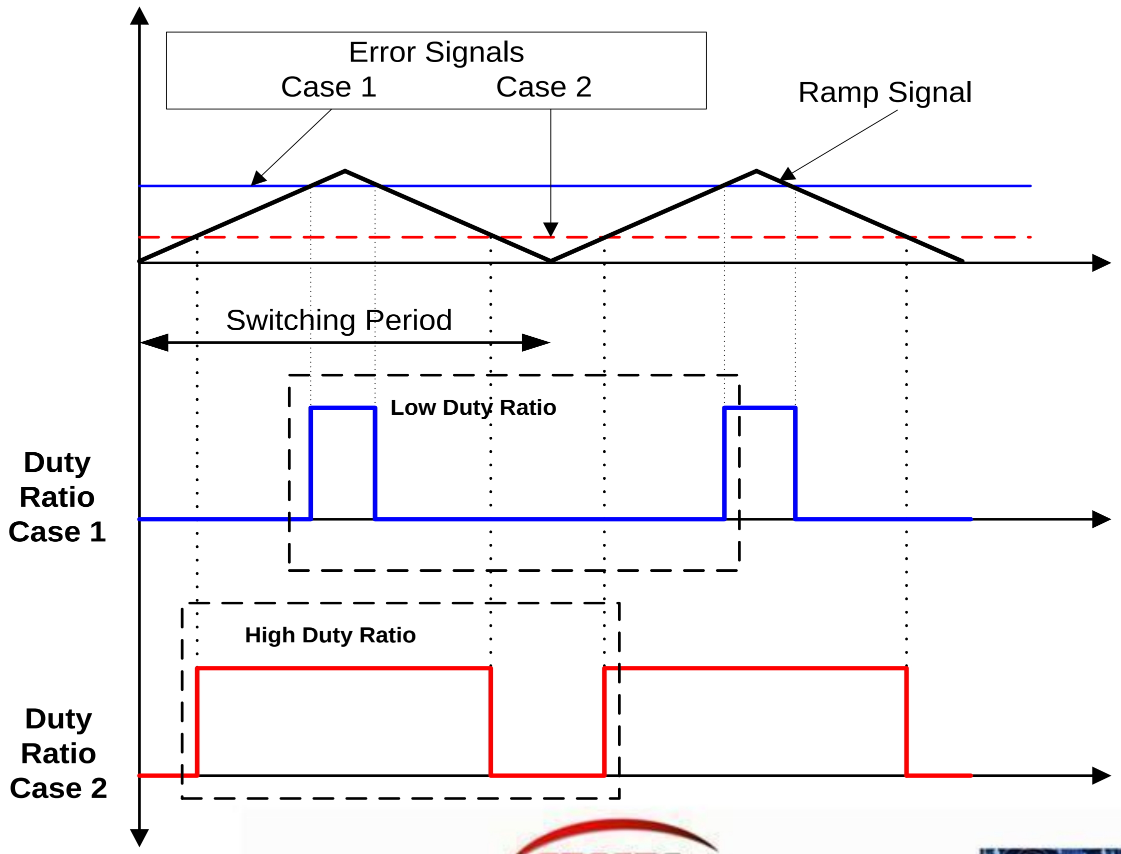
❑ **Output voltage value is adjusted by adjusting duty cycle.**

Pulse Width Modulation Control For Buck Converter



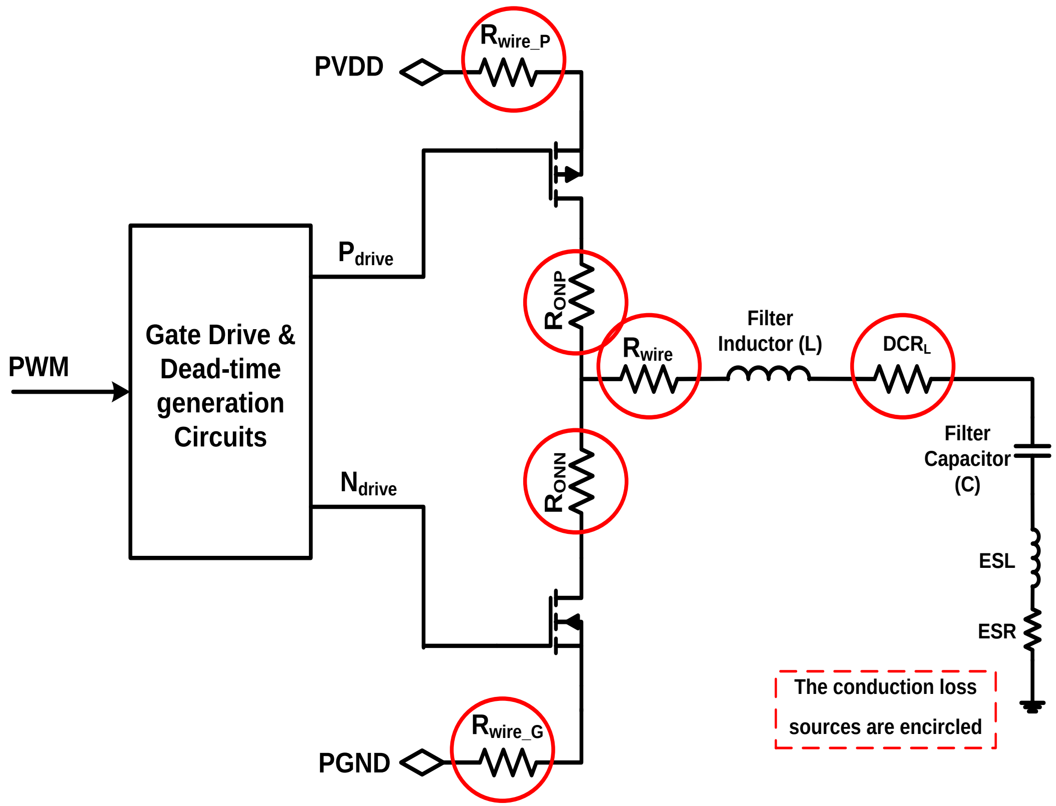
Pulse Width Modulation Control For Buck Converter

❑ Pulse width modulation concept



Power Losses in Buck Converter

- Conduction losses.



Power Losses in Buck Converter (Cont..)

- Switching losses.
  - MOSFET Switching Loss.
    - Power loss during turn-on and turn-off of Power MOSFETs.

$$P_{SW(FET,ON)} = \frac{1}{2} . V_{in} . I_{valley} . (t_{sw(ON)}) . F_{SW}$$

$$P_{SW(FET,OFF)} = \frac{1}{2} . V_{in} . I_{peak} . (t_{sw(OFF)}) . F_{SW}$$

  - Gate Drive Loss.

$$P_{GD} = P_{gate\,(HS)} + P_{gate\,(LS)} = (Q_{g(HS)} + Q_{g(LS)}) . V_{Driver} . F_{SW}$$

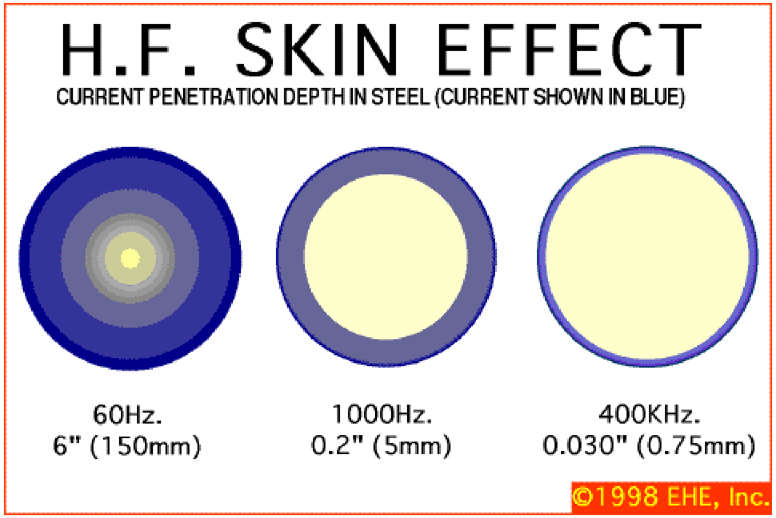
  - Body Diode Loss.
    - Dead-time loss (diode conduction loss).
    - diode reverse-recovery loss.

Power Losses in Buck Converter (Cont..)

- Inductor Related Power Loss.
  - Inductor Core Loss.

$$P_{core} = K_1\, f^x B^y\, V_e \quad (mW)$$

  - Inductor AC Loss in Windings.
    - Skin effect at high frequency.
    - $R_{AC} = \rho \frac{L}{[\pi\, r^2 - \pi(r - D_{PEN})^2]}$



Design Specifications For Buck Converter

- Buck converter should be capable of powering recent Intel Atom ™ processor families.

  - Output voltage range 0.75 V to 1.5 V
  - High output current capability up to 10 A
  - High efficiency higher than 90%
  - High switching frequency of 2 MHz
  - Small output voltage ripple (<3%)
  - Fast transient response

Power Stage Design

❑ Inductor Selection

➢ Minimum inductor value should be used to ensure CCM operation.

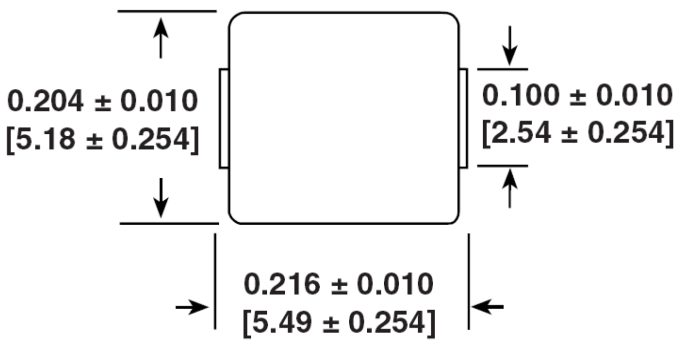
$$L_{min} = \frac{(1-D)V_O}{2f_S I_L}$$

$$L_{min} = 167nH$$

Power Stage Design (Cont..)

❑ Inductor Selection

- ➢ For safety, the inductor value is chosen higher than 167 nH.
- ➢ An inductor with a value of 220 nH from Vishay is selected

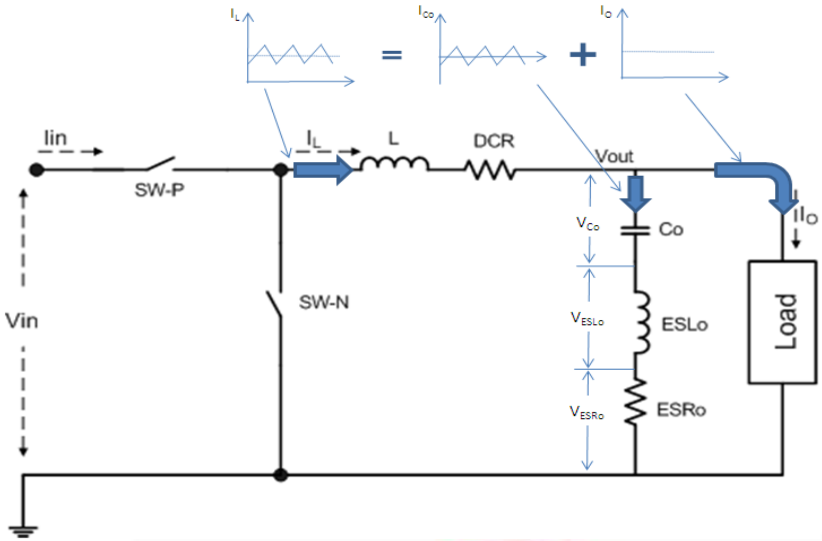


Selected inductor has a maximum DC resistance of 5.2 mΩ

Power Stage Design (Cont..)

❑ Output Capacitor Selection

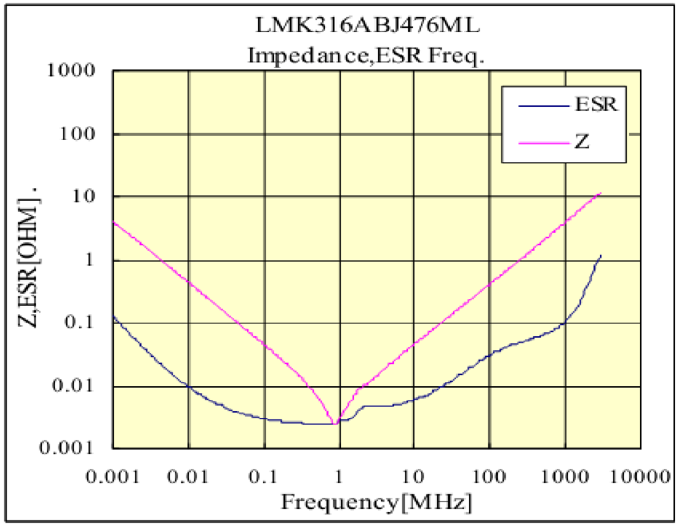
- ➢ High capacitance value could help in minimizing undershoot/overshoot percentage.
- ➢ Capacitor with low ESR and ESL should be selected.



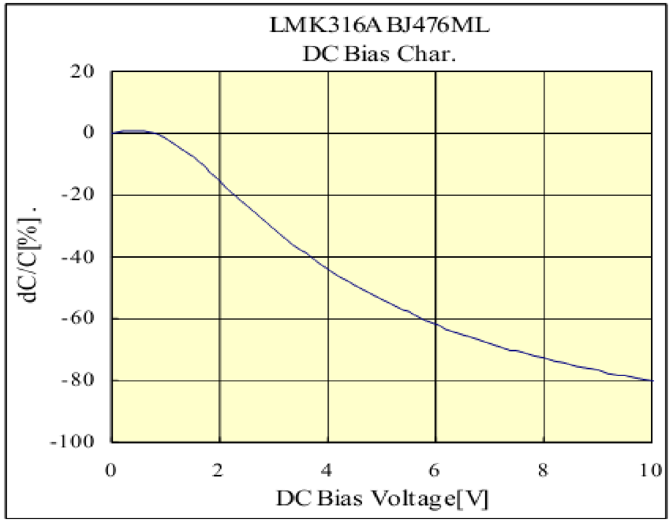
Power Stage Design (Cont..)

❑ Output Capacitor Selection

- Two parallel 47 µF capacitors are used in order to minimize the output ripple and the output undershoot/overshoot at the same time.



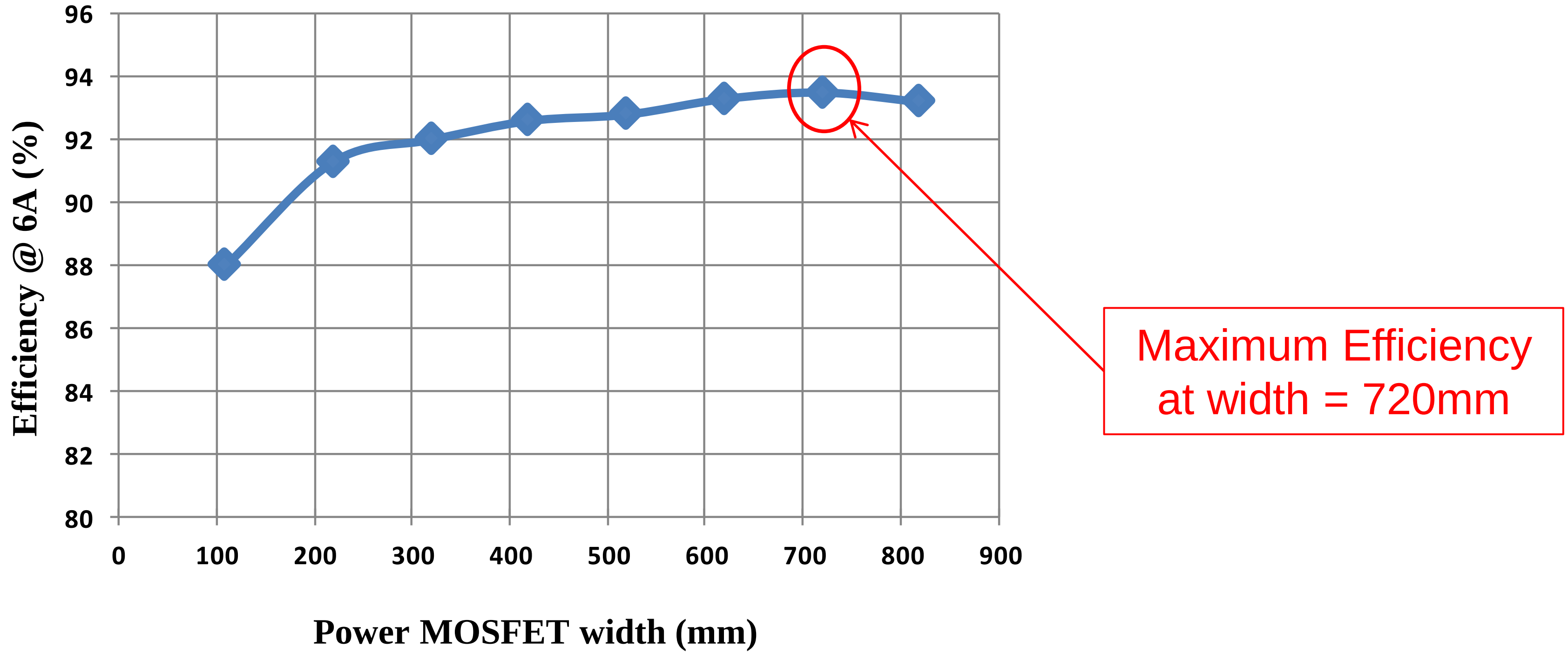
Impedance and ESR



Capacitance vs. DC biasing

Power Stage Design

❑ Power MOSFETs Design

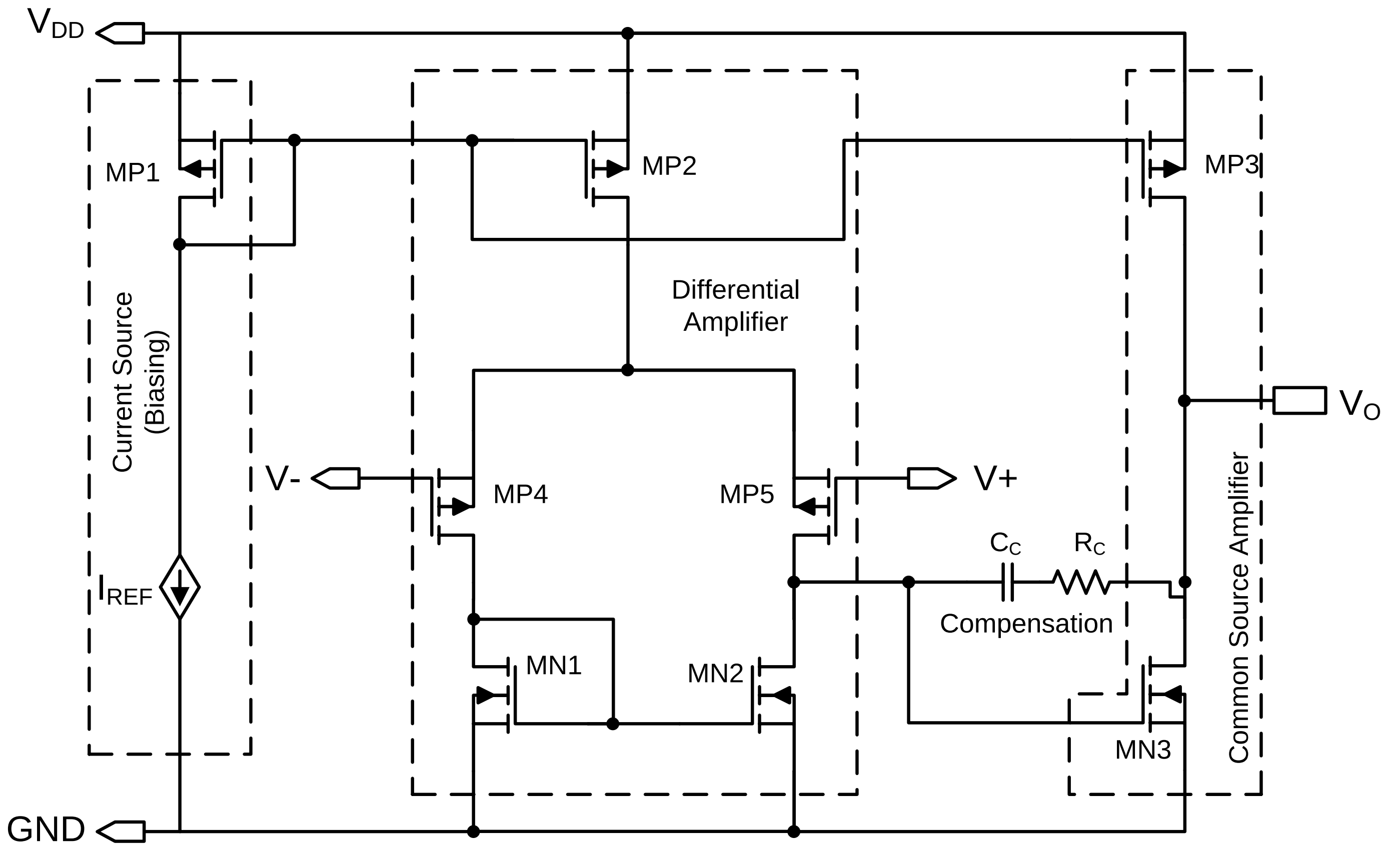


Error Amplifier Design

- The error amplifier is simply an operational amplifier.
- The *EA* is concerned by detecting the difference between V_{ref} and V_{FB}.
  - This difference is called "*error signal*".
- for the buck converter to operate properly at high switching frequencies:
  - High gain.
  - Wide bandwidth.
  - High slew rate.

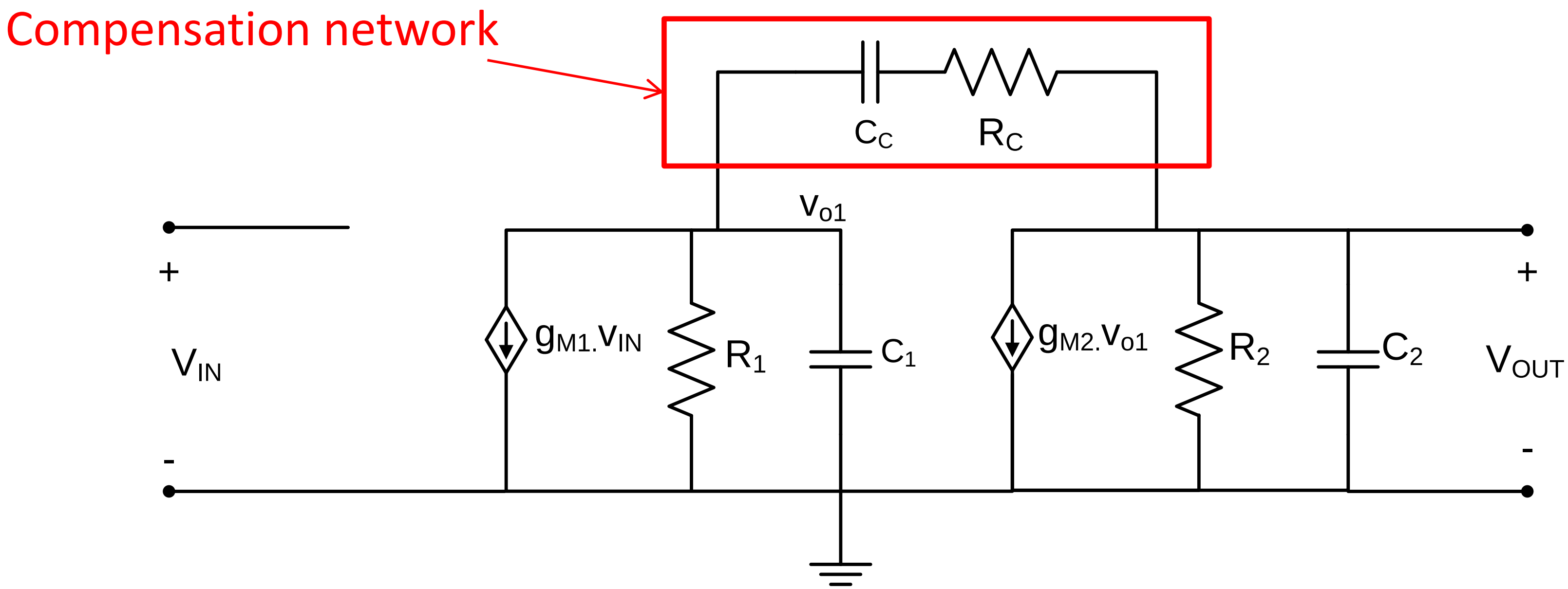
- The two-stage Op Amp is sufficient.

Error Amplifier Design (Cont..)

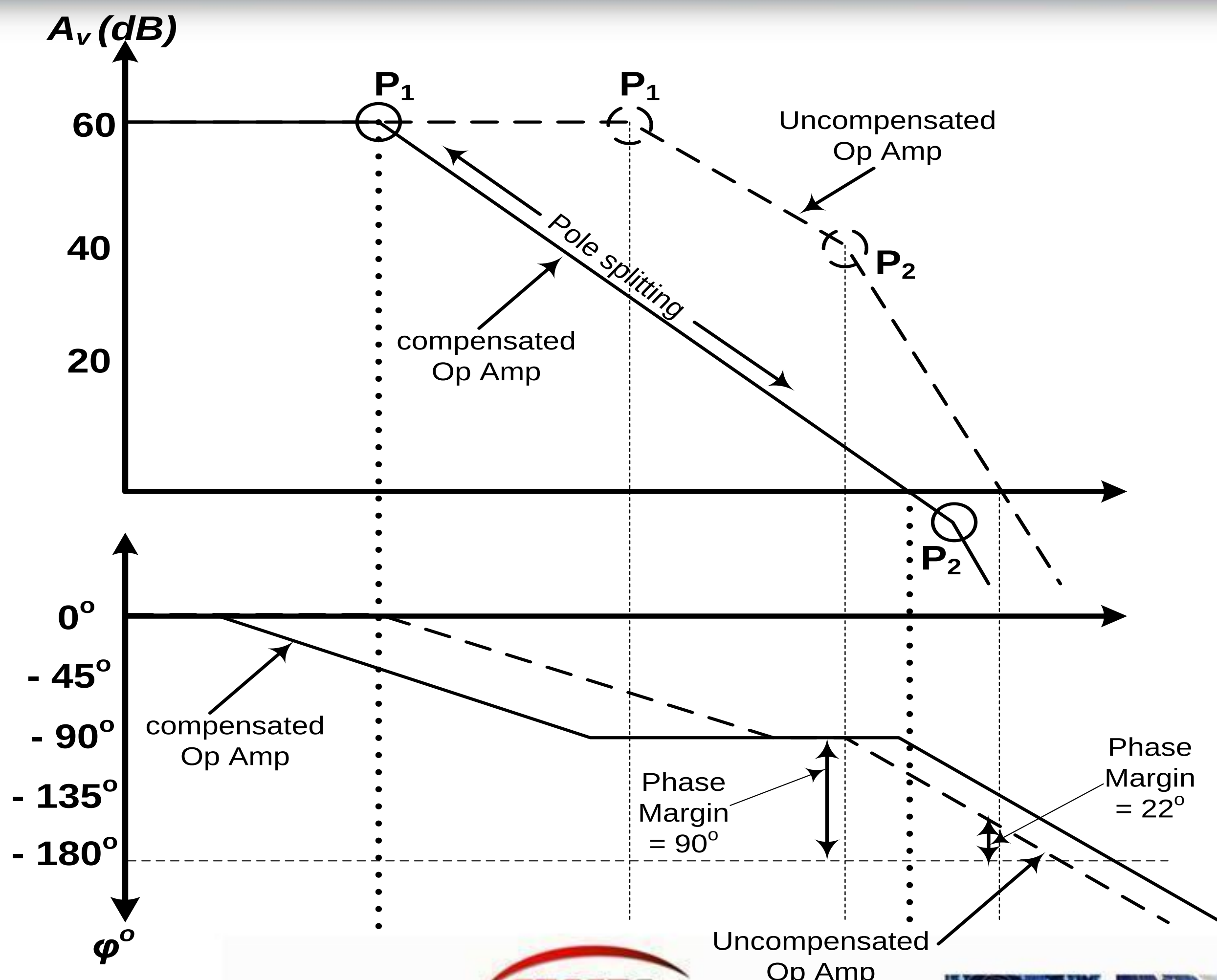


Error Amplifier Design (Cont..)

- Compensation network is used to ensure the Op Amp stability if the Op Amp is configured as a closed-loop.

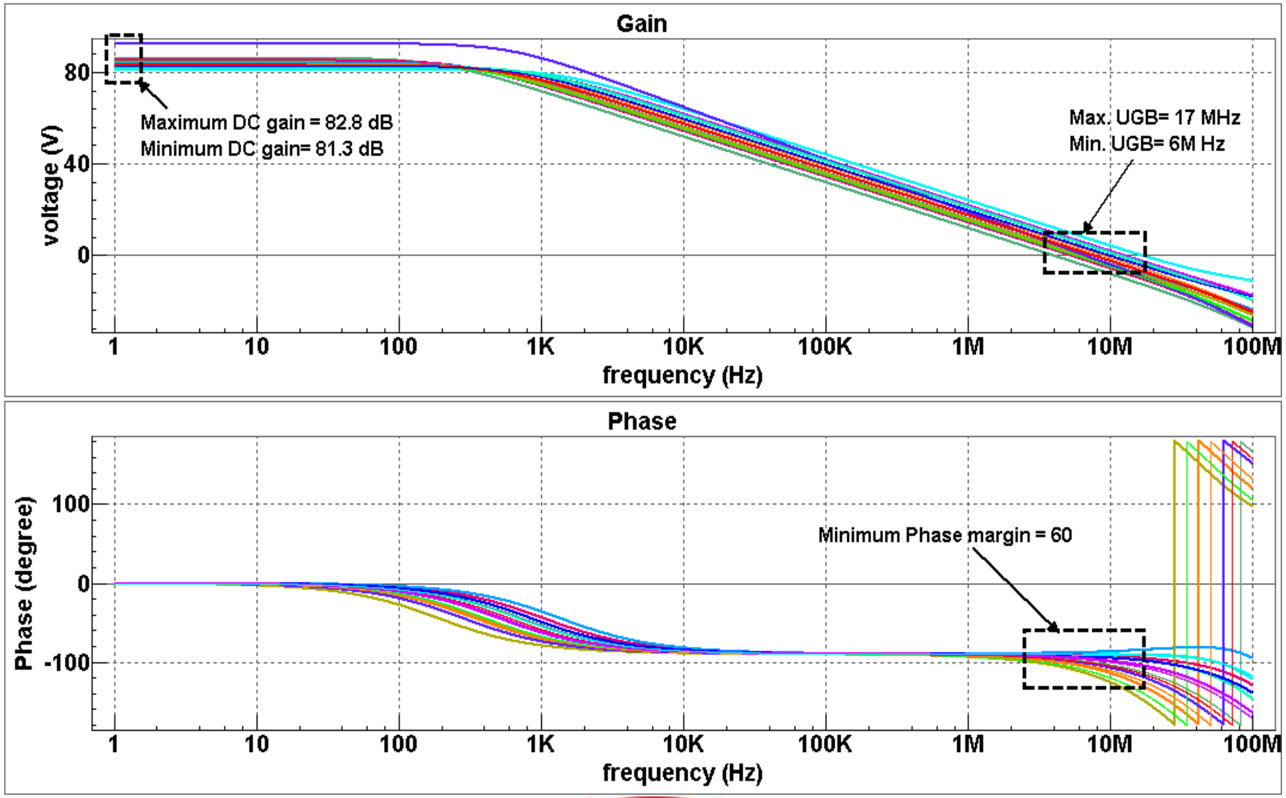


Error Amplifier Design (Cont..)



Error Amplifier Design (Cont..)

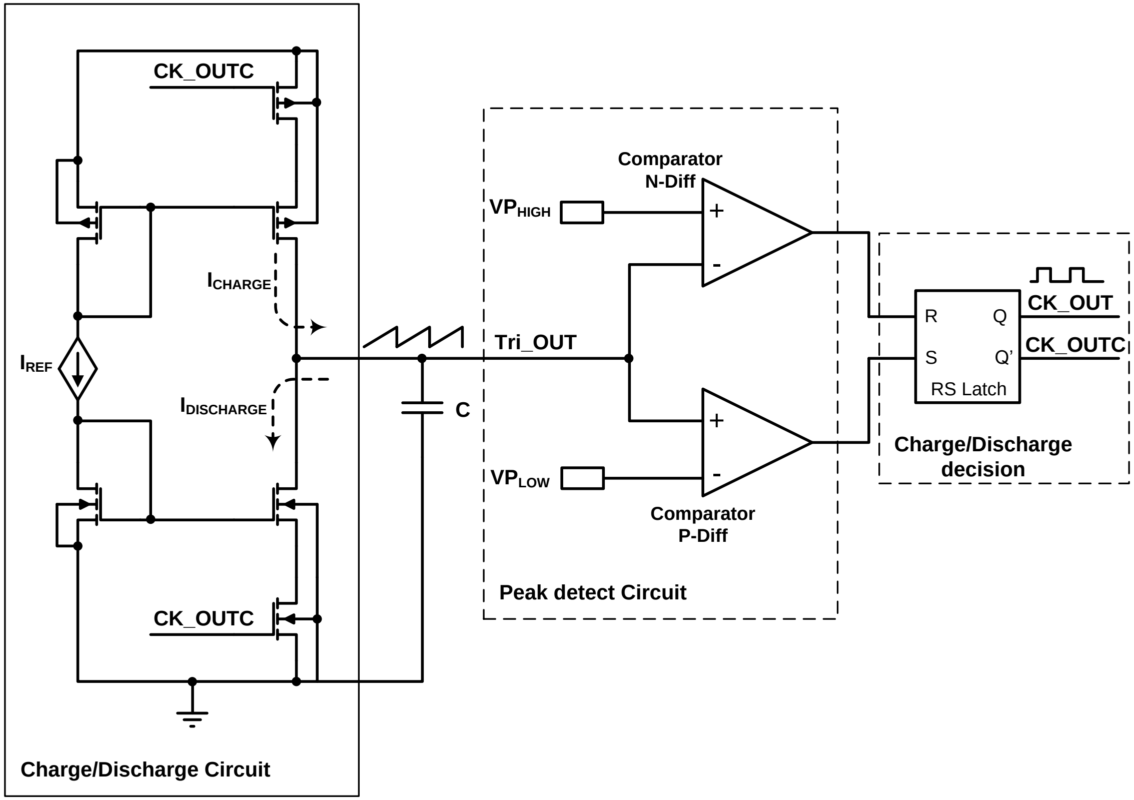
Op Amp gain and phase with supply [±10%] and Temperature [-40, 25 and 125 C] and process node variations



Triangular Signal Generator

The main idea:

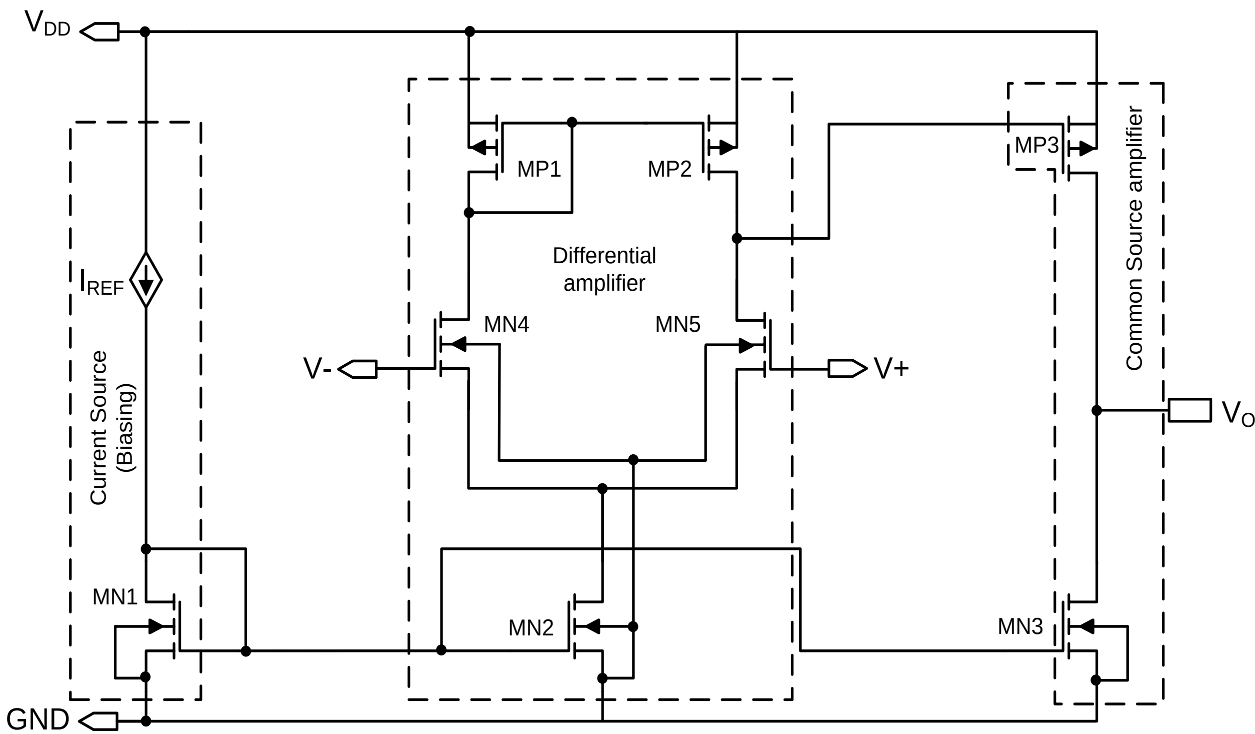
- Charge and discharge a capacitor with a constant current.
- Capacitor voltage is compared to VP_{High} and VP_{Low}
- VP_{High} and VP_{Low} determine peak to peak voltage.



Triangular Signal Generator (Cont..)

- Fast and accurate for high input voltages.
- Used to detect the high peak of the triangular signal.

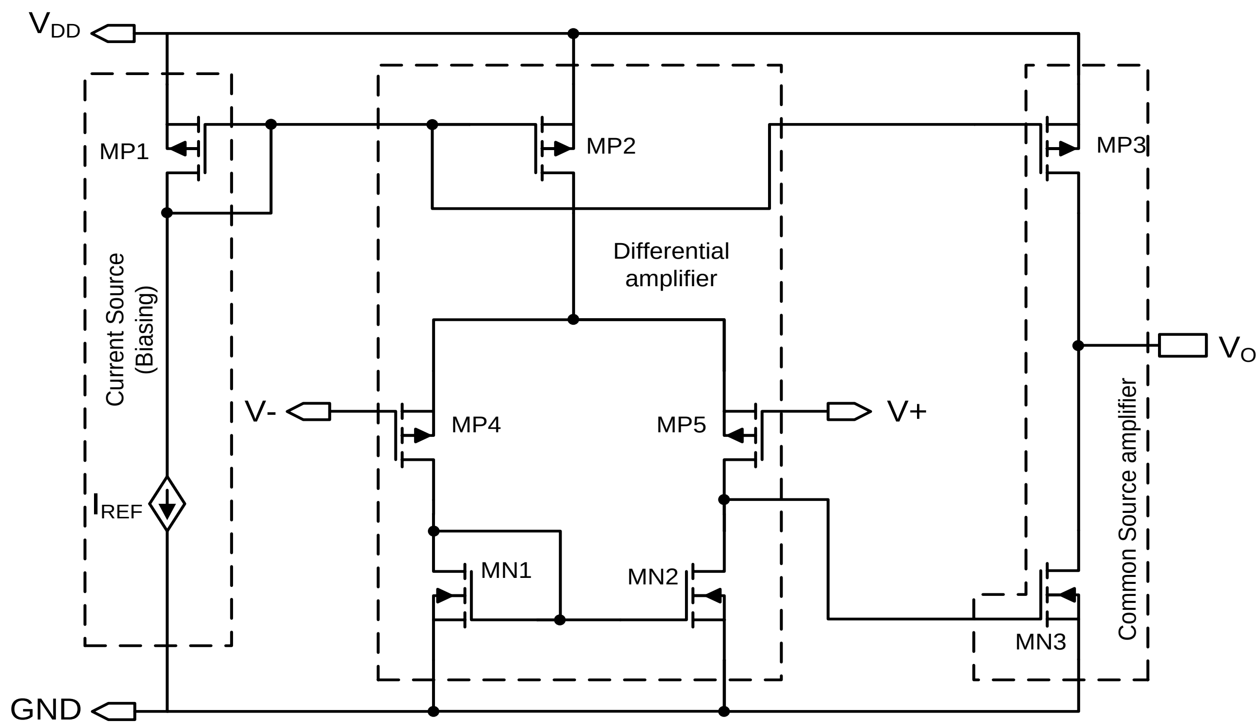
Comparator N-diff



Triangular Signal Generator (Cont..)

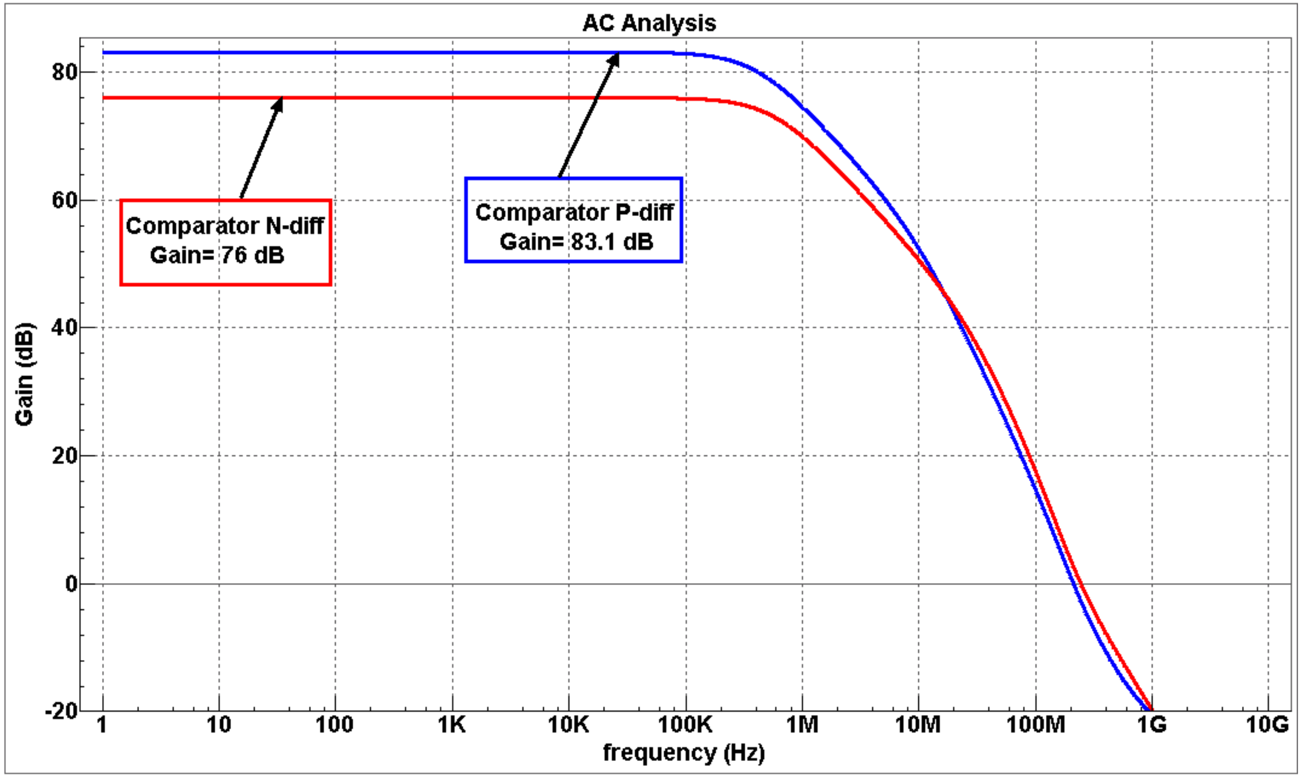
- Fast and accurate for <u>low</u> input voltages.
- Used to detect the <u>low</u> peak of the triangular signal.

Comparator P-diff



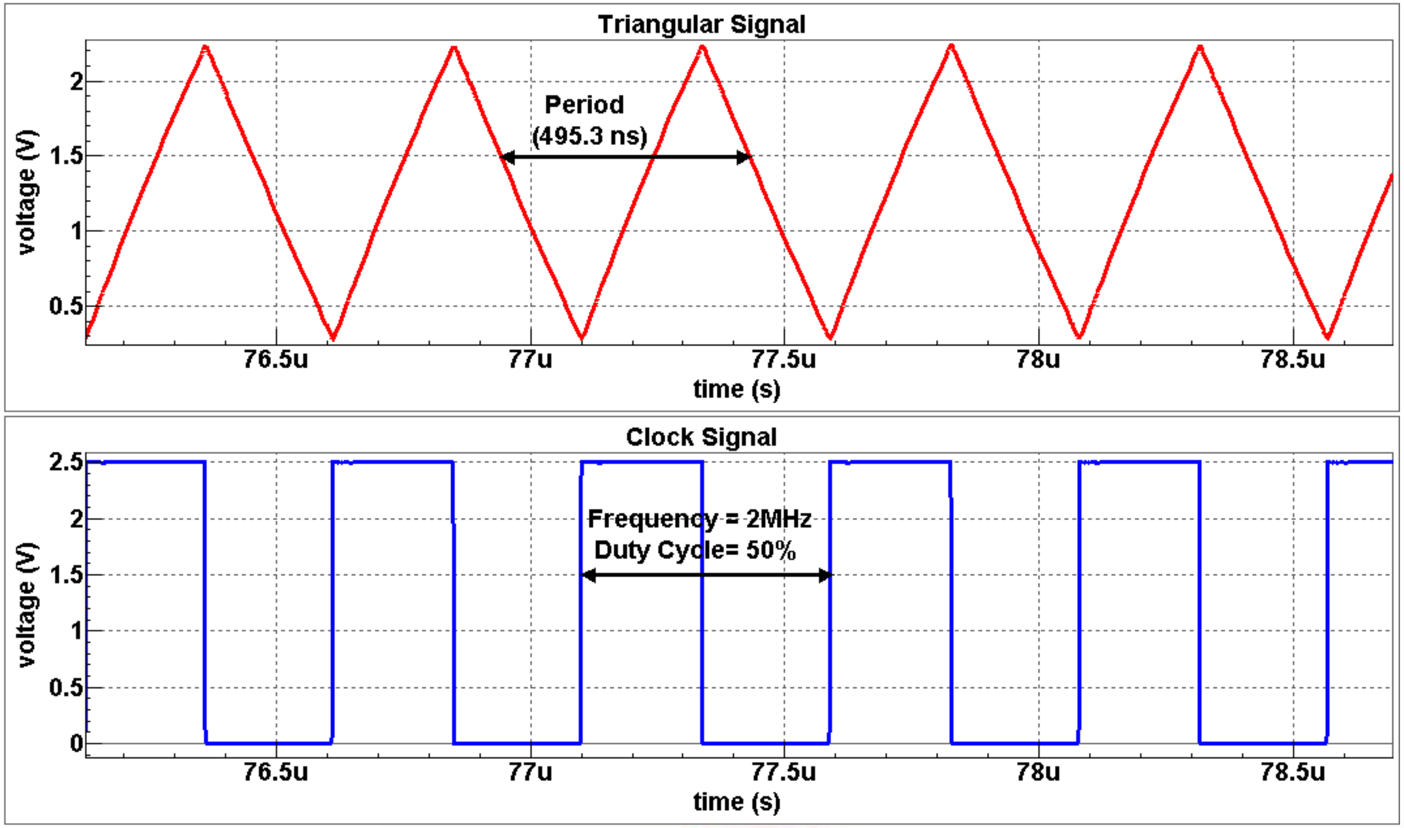
Triangular Signal Generator (Cont..)

Gain vs. frequency for the designed two-stage comparator



Triangular Signal Generator (Cont..)

Simulation results for triangular signal and clock signal

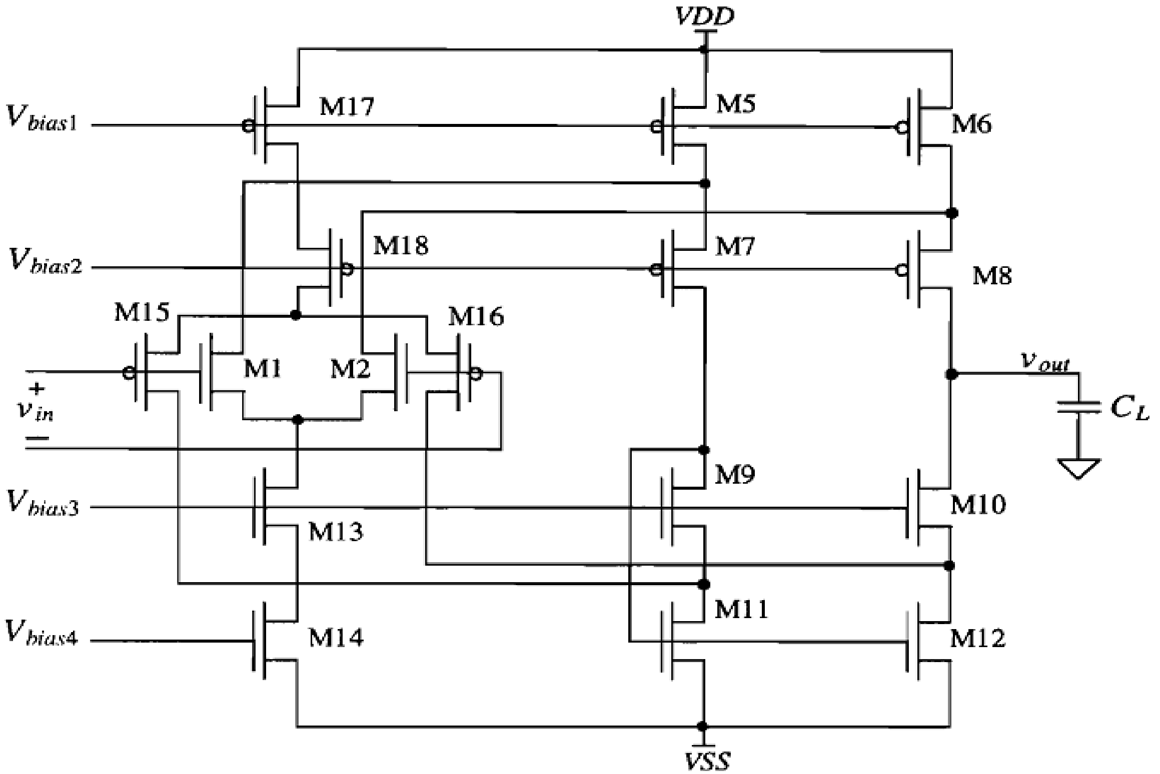


PWM's Comparator

Rail-to-rail input range comparator

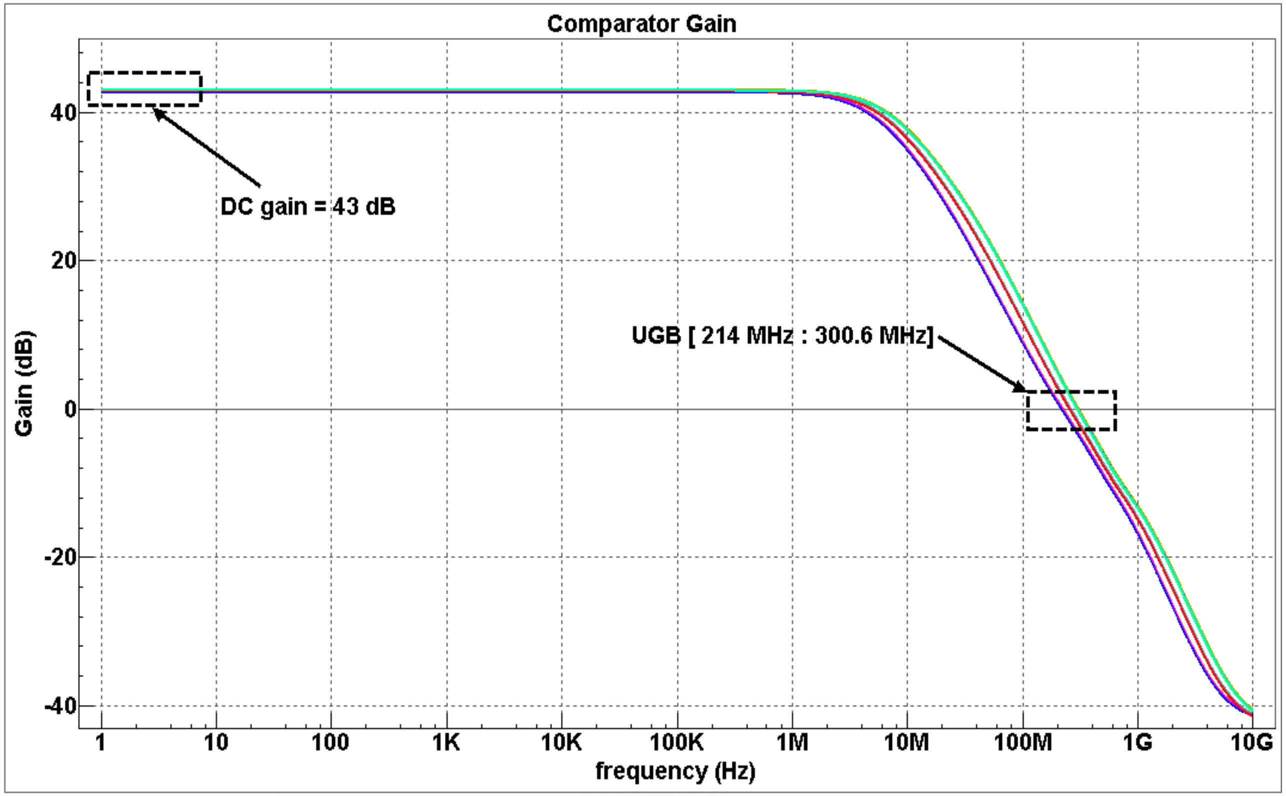
- Used in the PWM controller to generate the required duty cycle

- Consists of:
  - PMOS folded-cascode combined with NMOS folded-cascode.



PWM's Comparator (Cont..)

PMOS/NMOS folded-cascode comparator gain with supply [±10%] and temperature [-40, 25 and 125 C] variations



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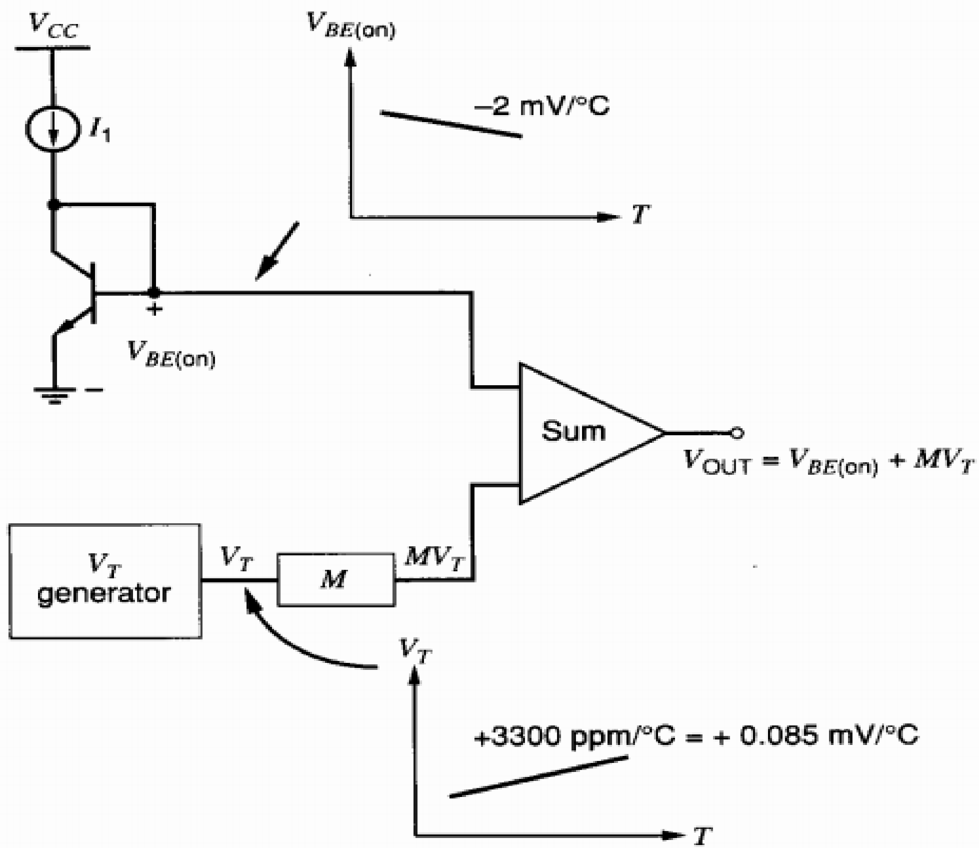
Reference Voltage Circuit

Methodology of bandgap reference voltage circuit



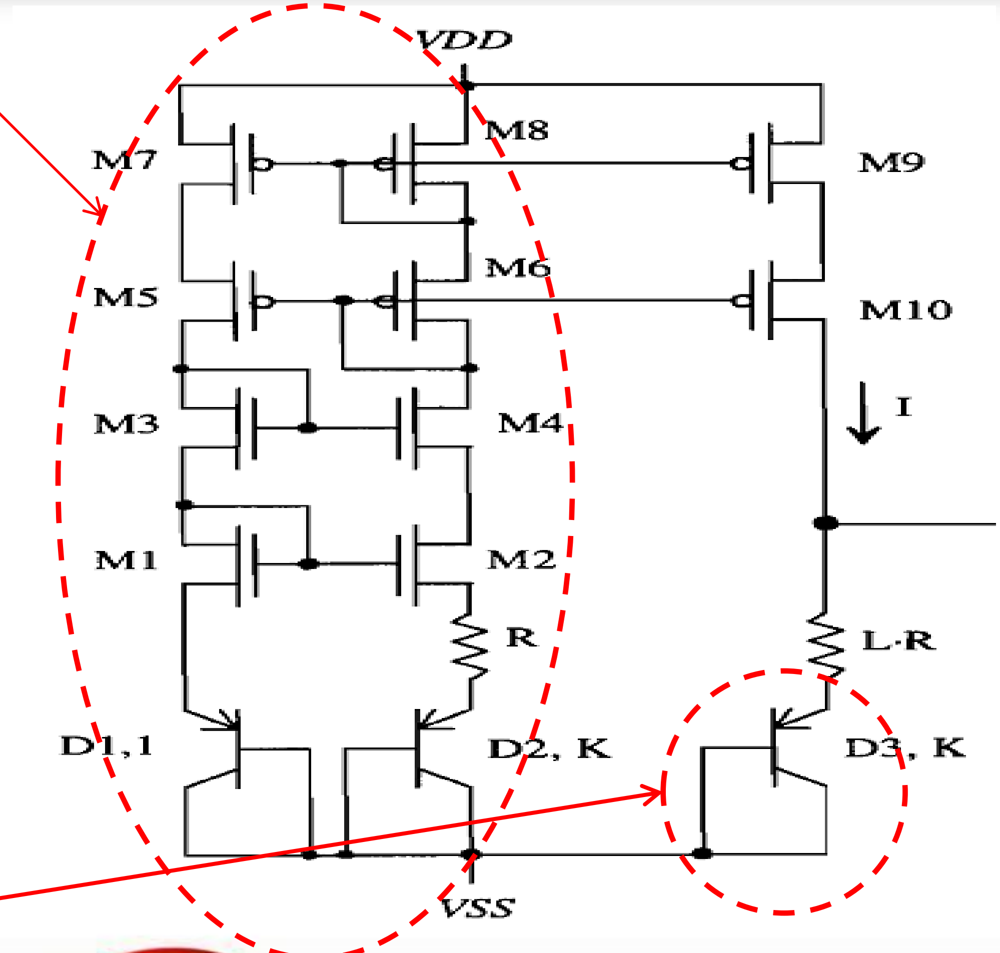
Reference Voltage Circuit (Cont..)

PTAT thermal voltage referenced

$$V_{ref} = I\,L\,R + V_{EB3}$$

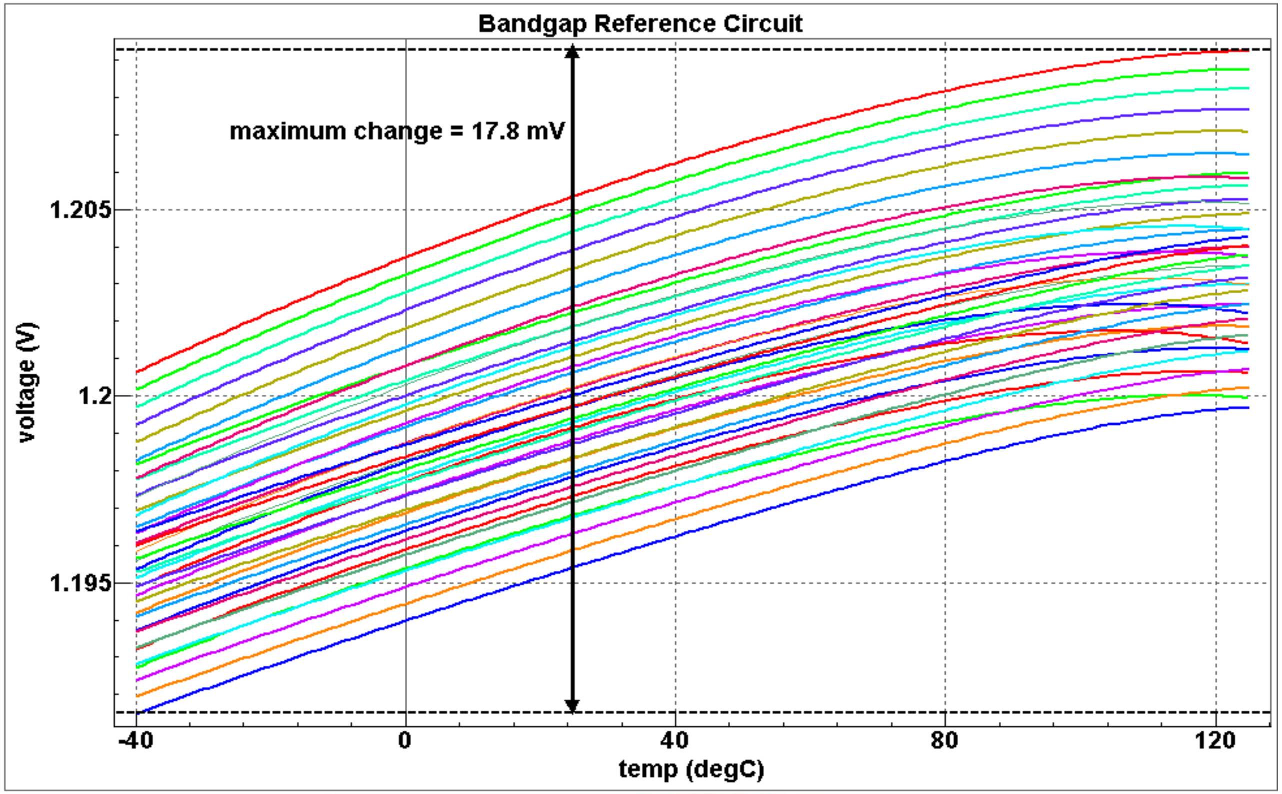
$$V_{ref} = L\,\ln K\,V_T + V_{EB3}$$

CTAT diode referenced



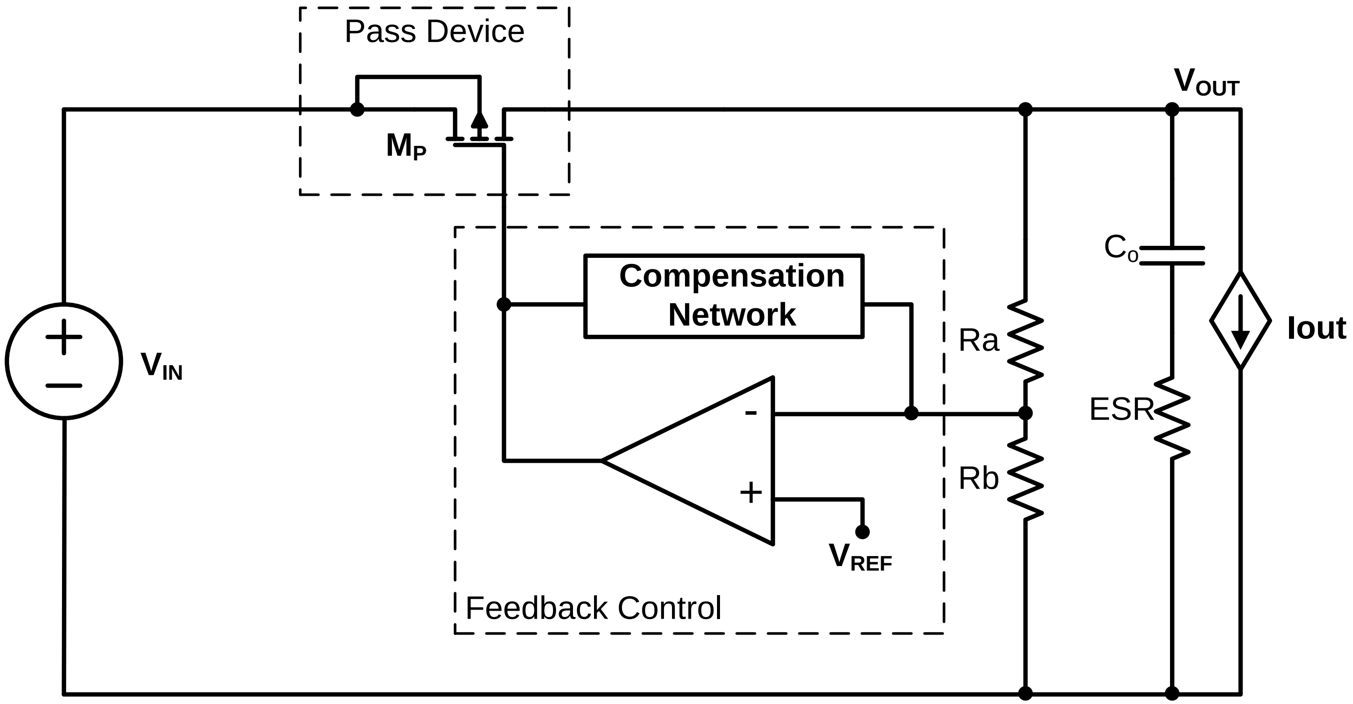
Reference Voltage Circuit

The output voltage of designed bandgap with temperature sweep [-40^{oC}:125^{o}C], ±10% change in supply voltage, and process variations



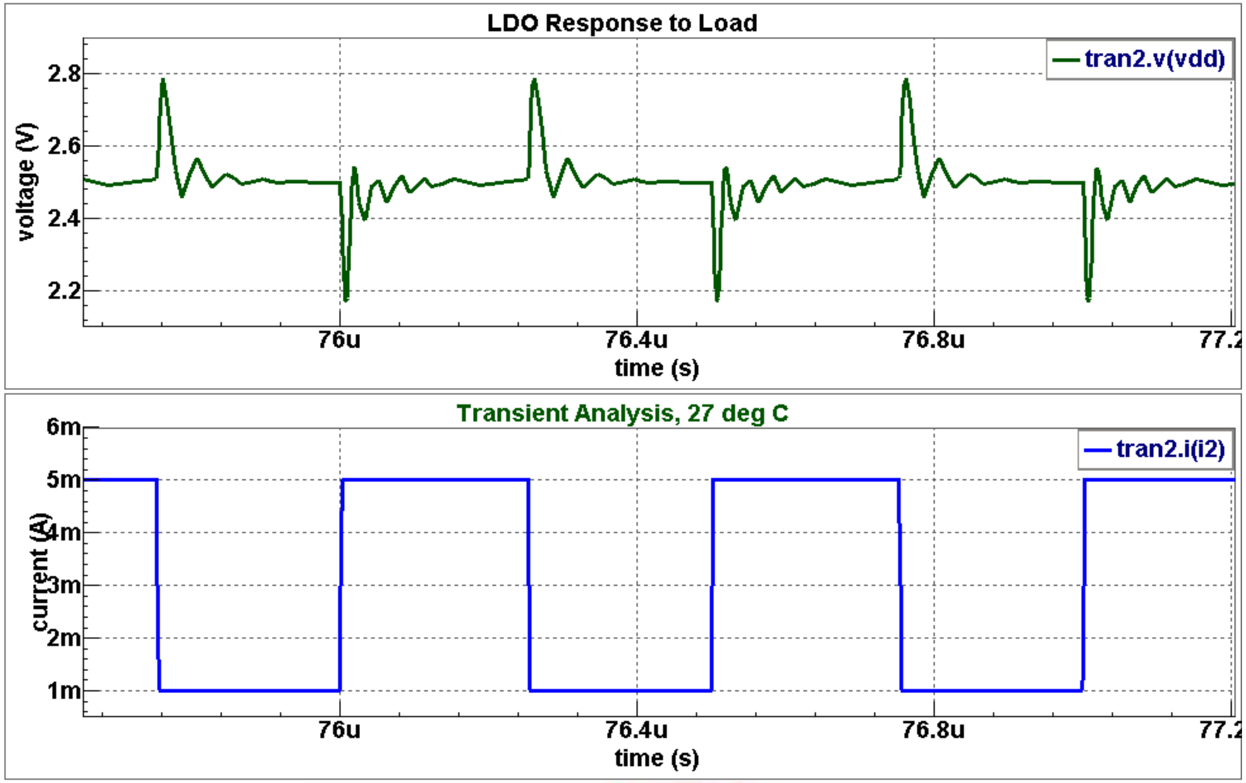
Design of Supply Voltage Generator

- Using of linear regulator to obtain supply voltage for controller circuits



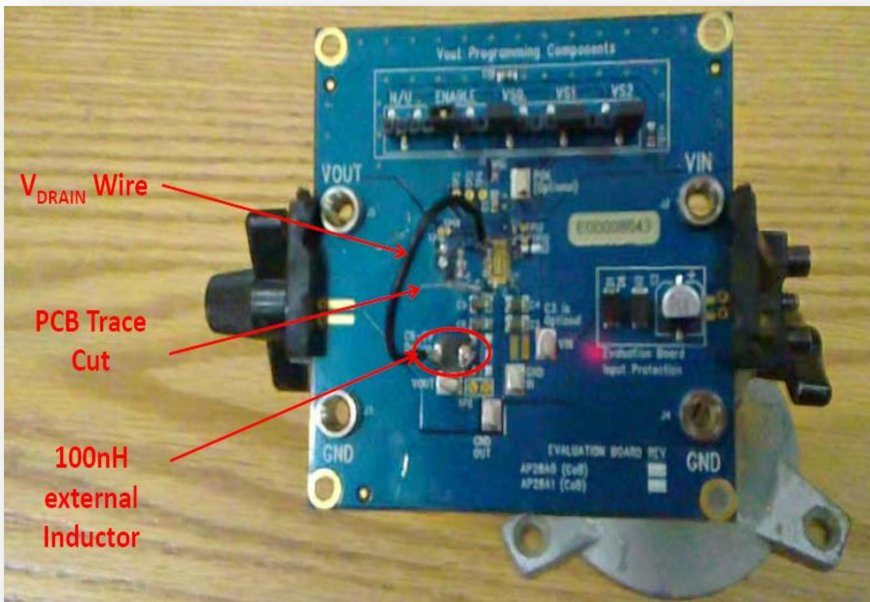
Design of Supply Voltage Generator (Cont..)

Linear regulator response to output current change
Worst case = ±12%

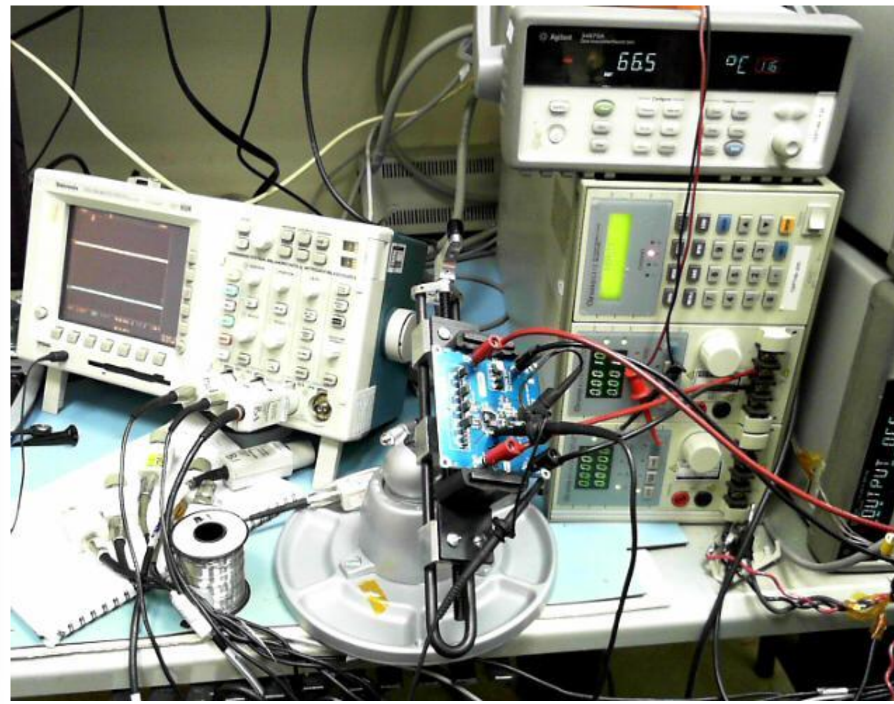


Experimental Results

Close view to PCB

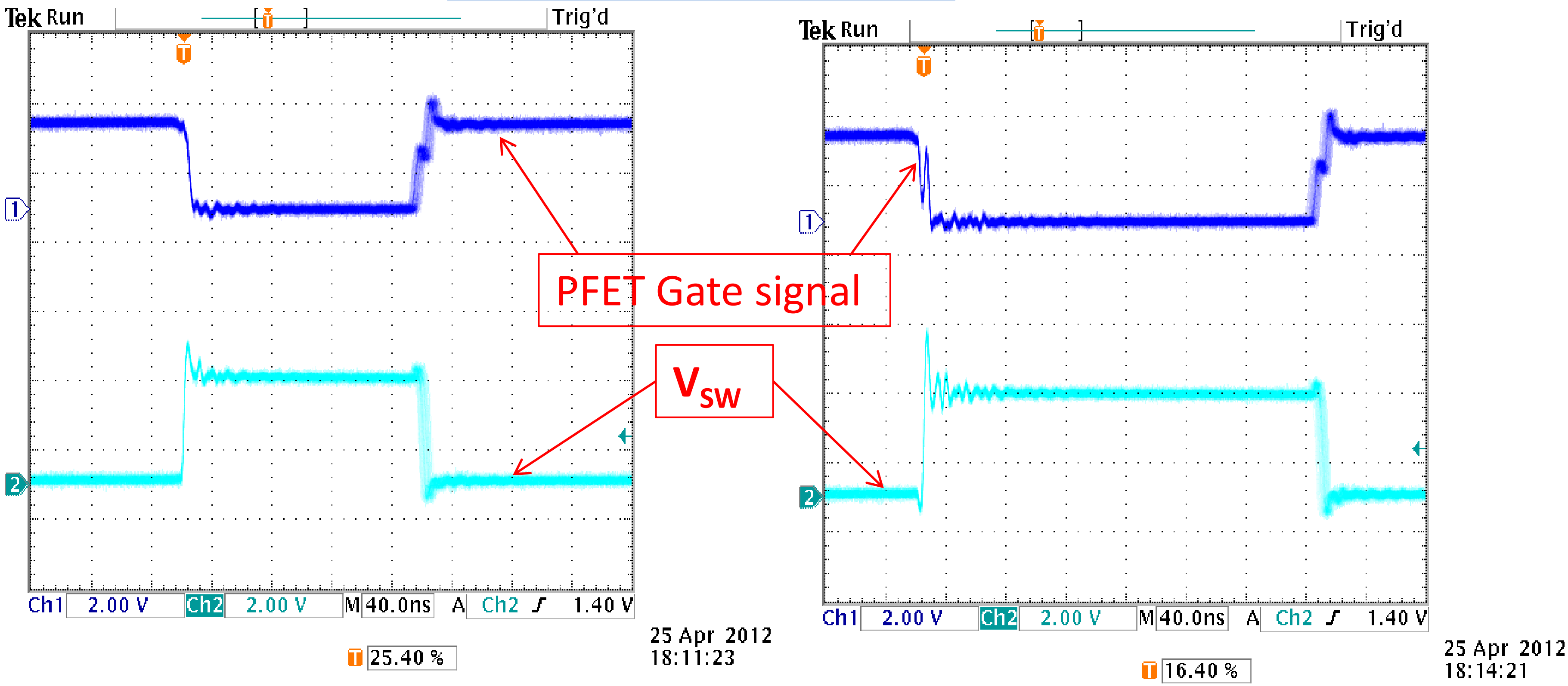


Experimental Setup



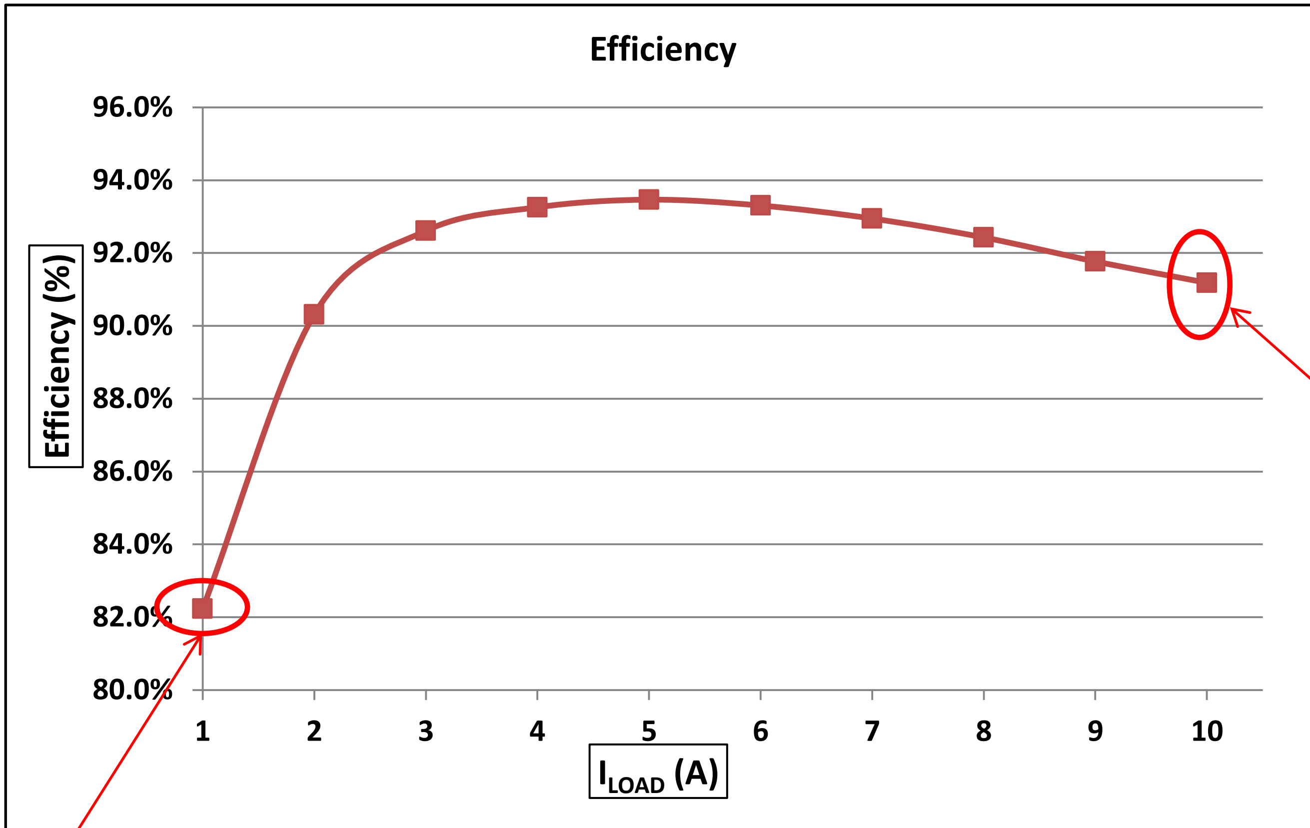
Experimental Results (Cont..)

Vin = 3V and Vout = 1.2V



Load = 0A **Load = 10A**

Experimental Results (Cont..)



Efficiency at Full Load = 91.18%

Efficiency at light load = 82%

Integrated Two-Stage Power Supply Design

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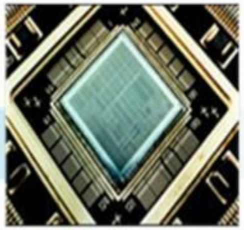


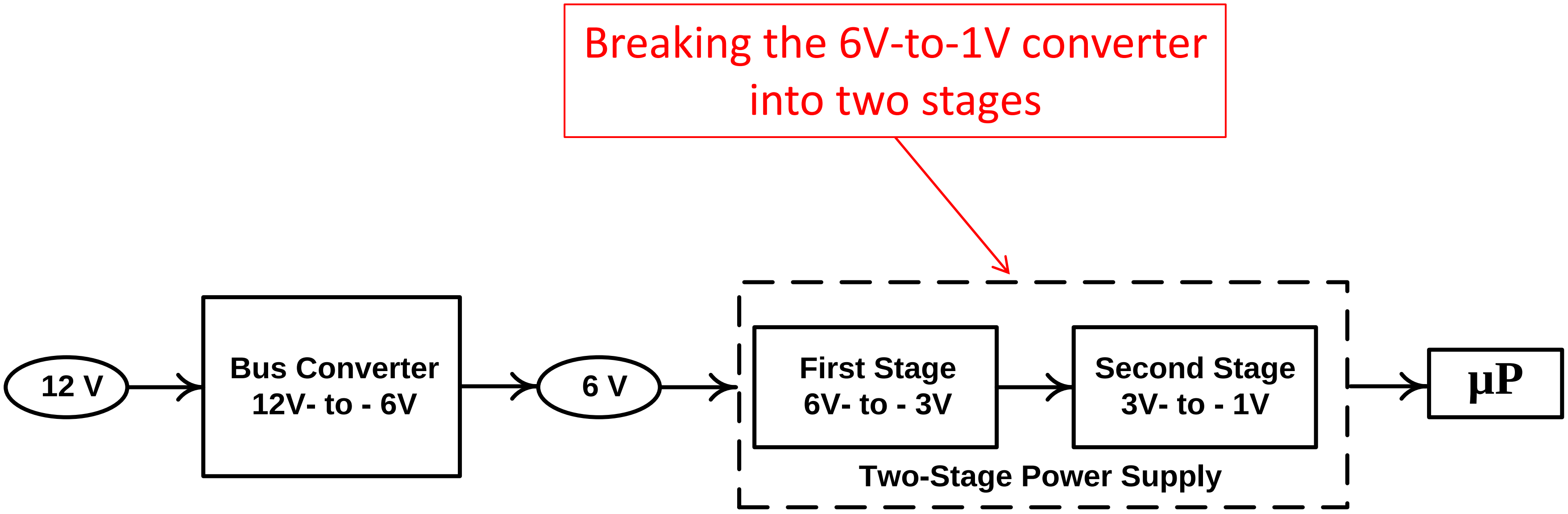
Limitations of Buck Converter

- As the buck input voltage increases and lower output voltages are required.
  - Switching loss increase.
  - Small duty cycle that leads to high peak current in top switch.
  - Degraded transient response.
  - High efficiency cannot be easily obtained.

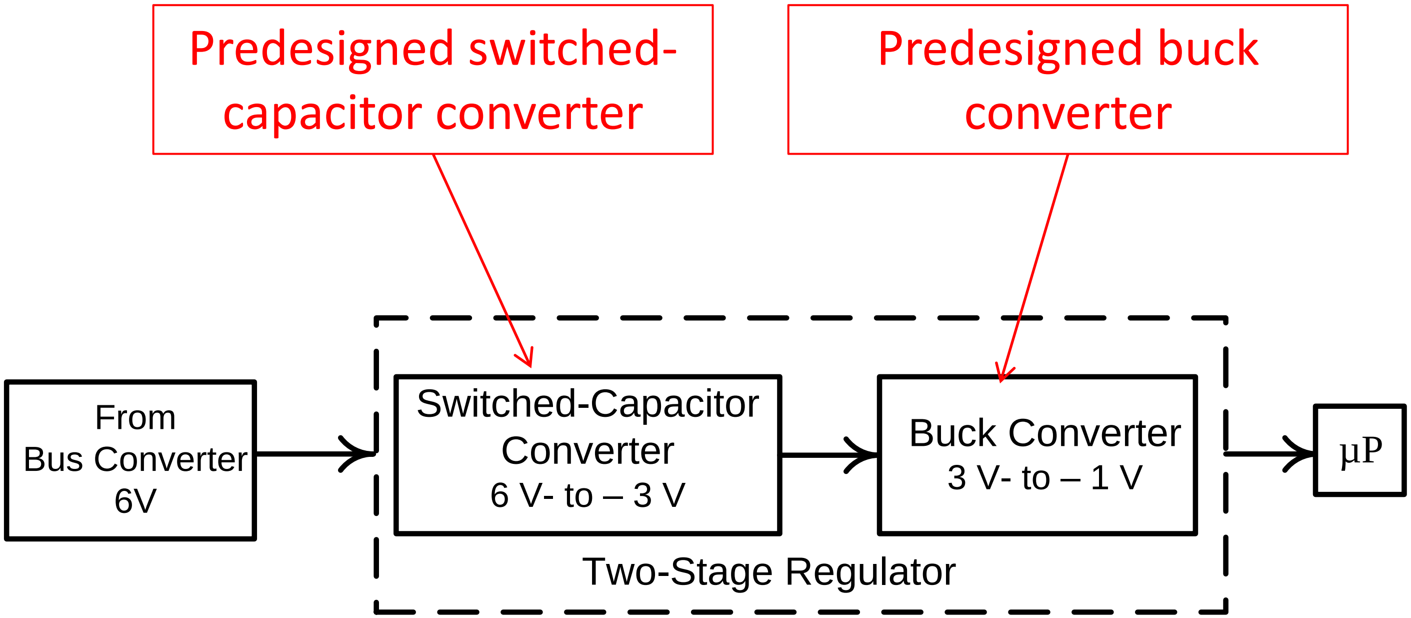
Limitations of Buck Converter

- If we decrease the input voltage for the buck converter
  - Higher efficiency due to the increase in duty cycle and the decrease in switching loss.
  - The ability to use low-voltage (LV) switches.
    - Decrease the solution footprint .
    - Exhibit lower on-resistance.
  - Reduce the fabrication cost.

Proposed Power Architecture



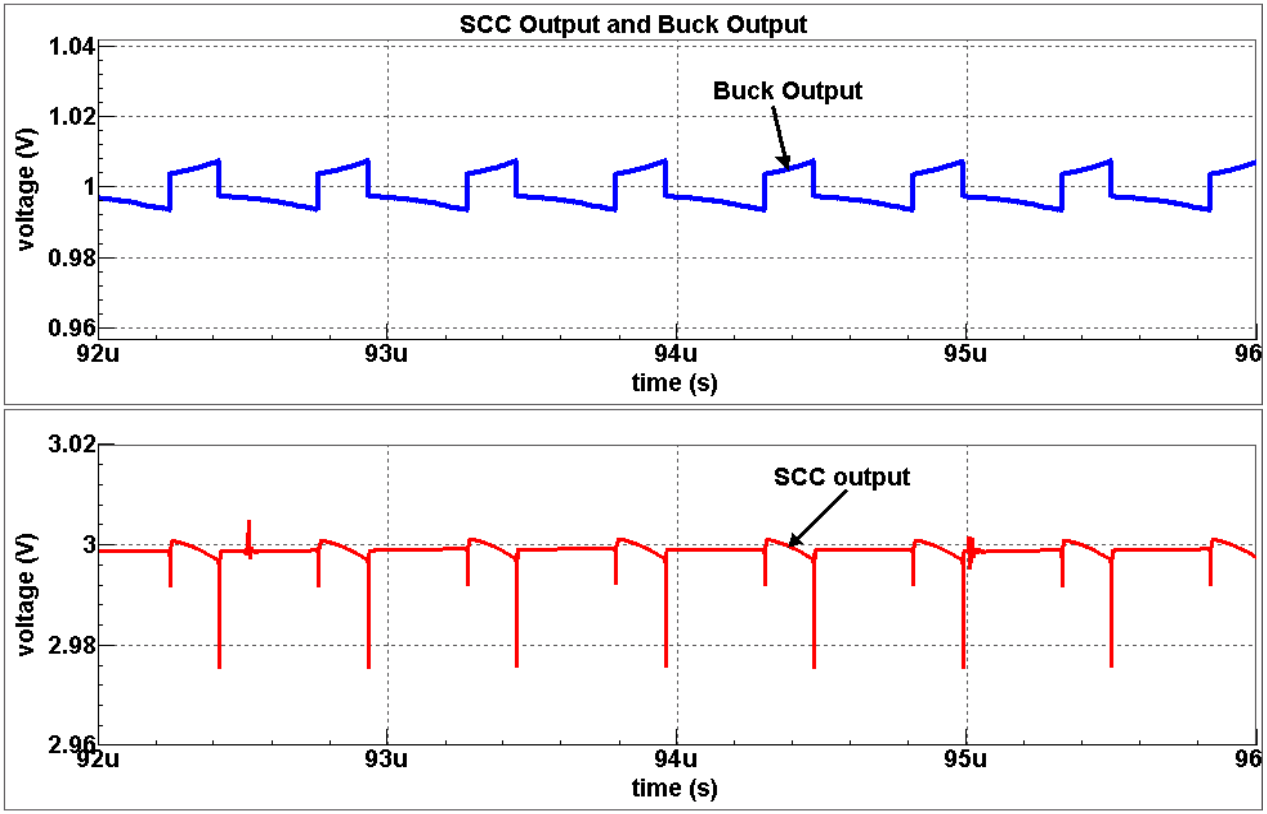
Proposed Power Architecture (Cont..)



Buck converter receive 3V instead of 6V which solves the duty cycle and efficiency issues.

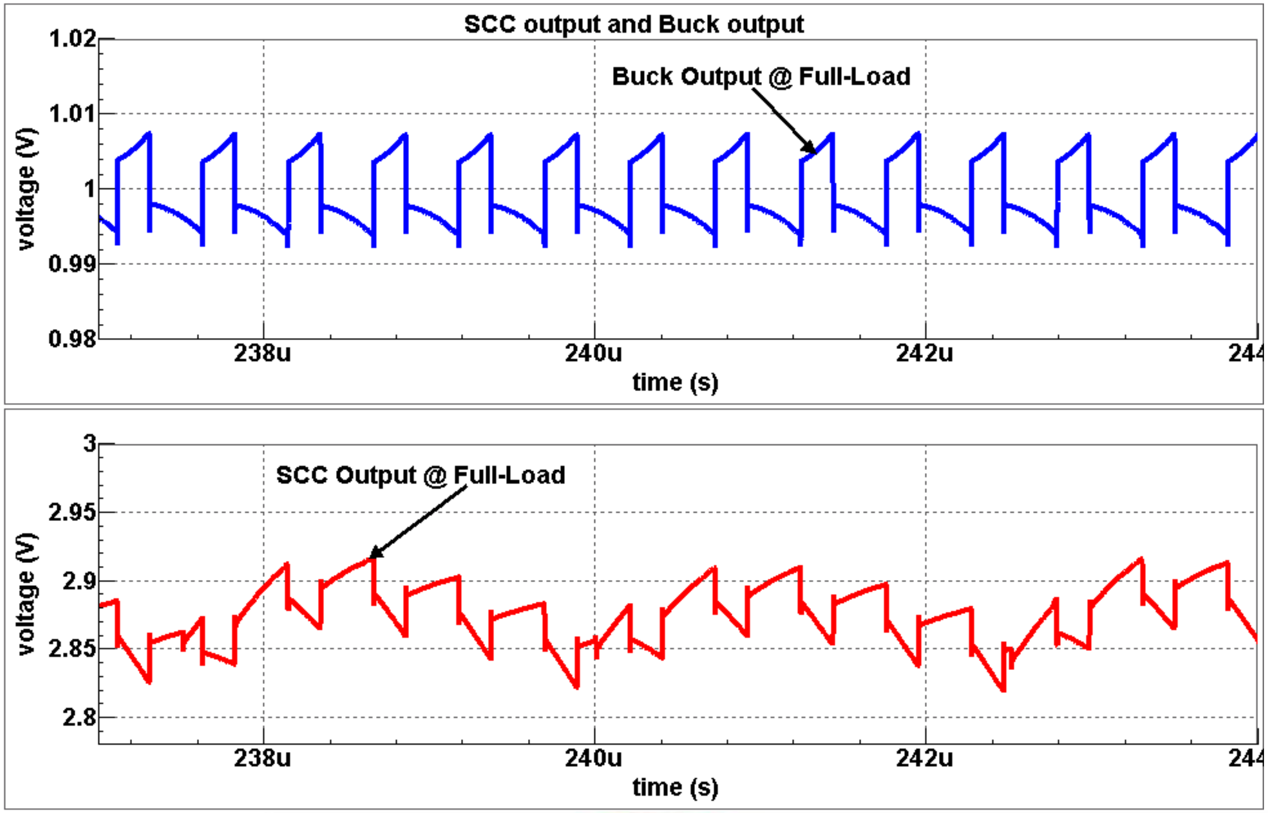
Integration of The Two-Stage System

SCC's output and buck's output of the two-stage system at no-load



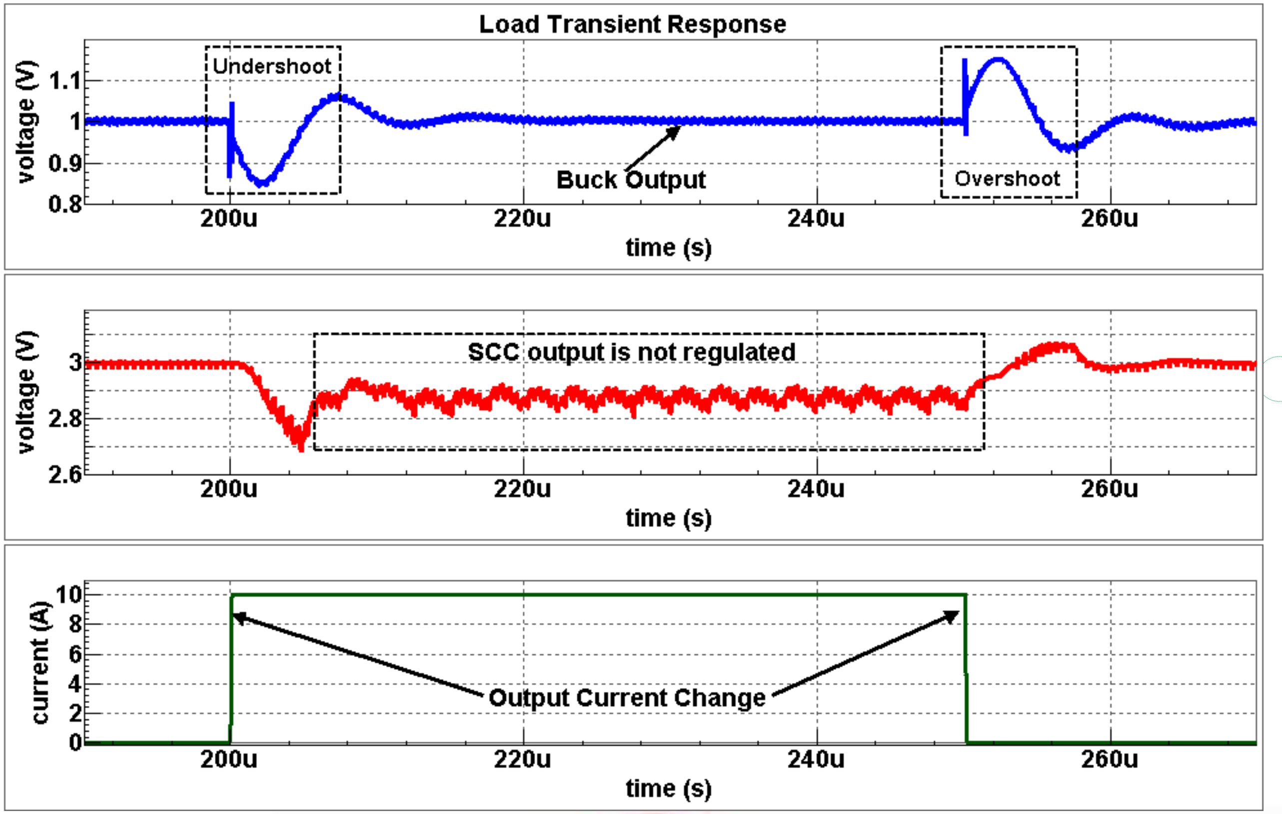
Integration of The Two-Stage System (Cont..)

SCC's output and buck's output of the tow-stage system at full-load

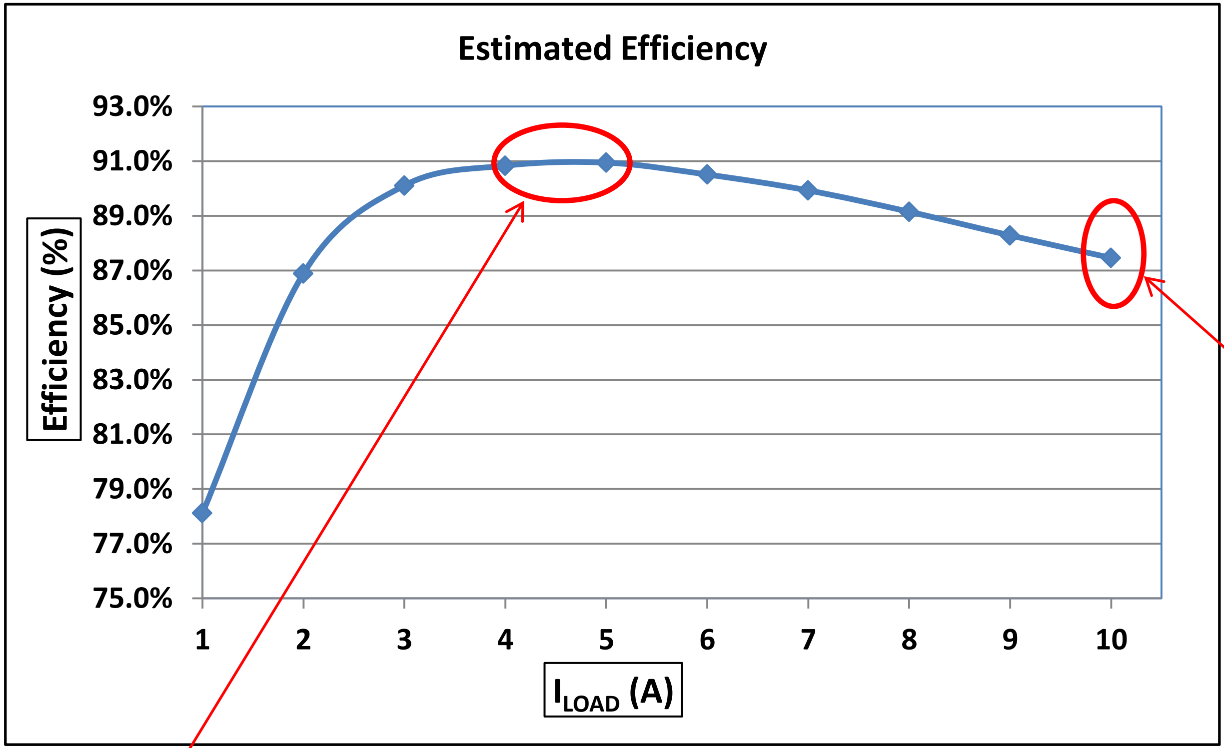


Integration of The Two-Stage System (Cont..)

Load transient response of the two-stage system



Integration of The Two-Stage System (Cont..)

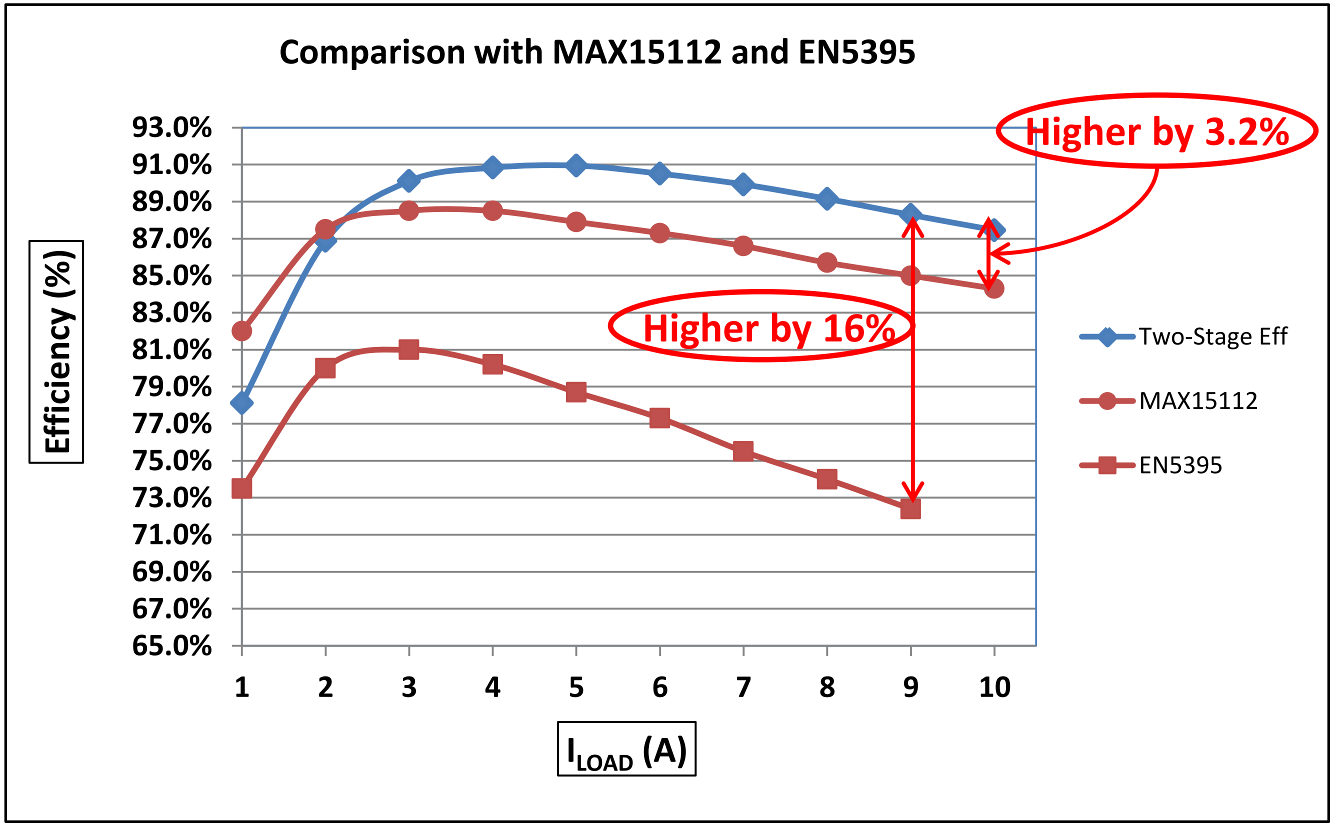


Efficiency at Full Load = 87.5%

Peak Efficiency= 91%

Integration of The Two-Stage System (Cont..)

Comparing two-stage Eff with 2 market examples



Design of Linear-Nonlinear Control Technique for Buck Converter

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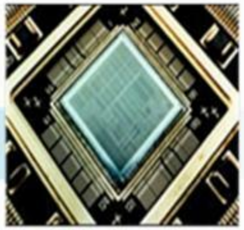
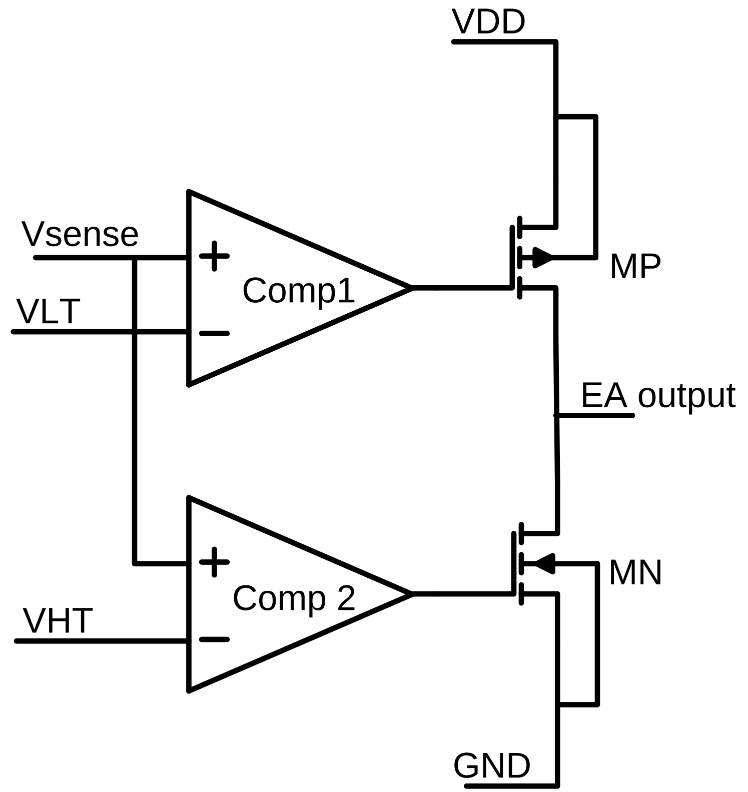


The Proposed Nonlinear Control Technique

❑ Novel nonlinear control:

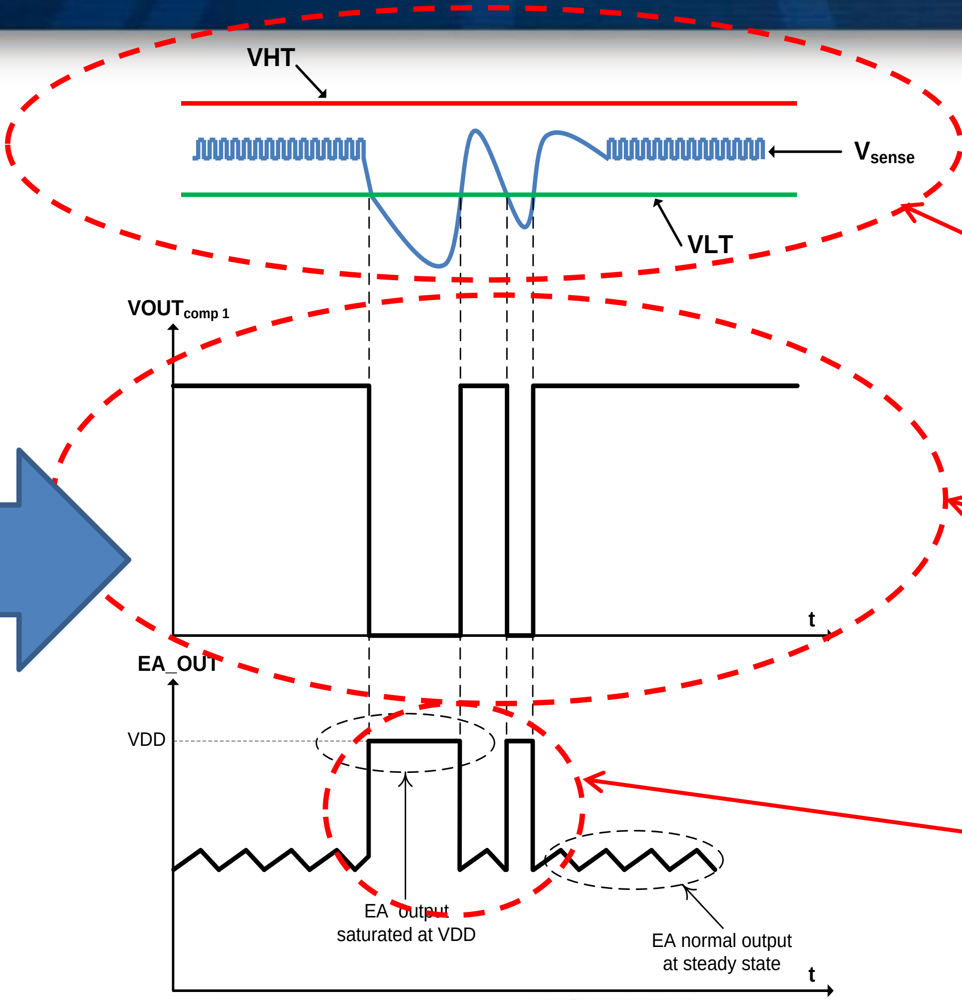
➢ Saturate the EA output at values near the supply voltage or ground voltage.

➢ Nonlinear control is enabled only during load transient.



The Proposed Nonlinear Control Technique (Cont..)

During Step-up load change condition



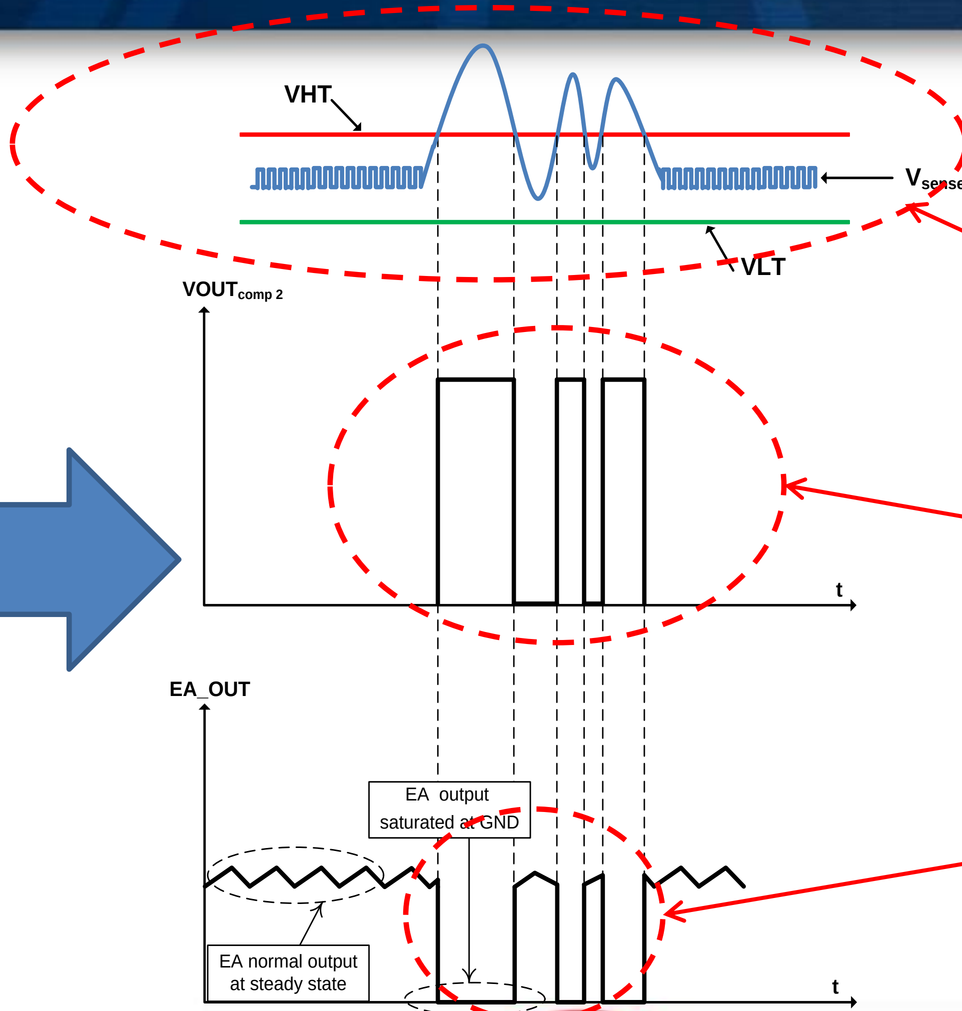
Comparison done to detect undershoot

Comparison result

Effect of nonlinear control on EA

The Proposed Nonlinear Control Technique (Cont..)

During Step-down load change condition



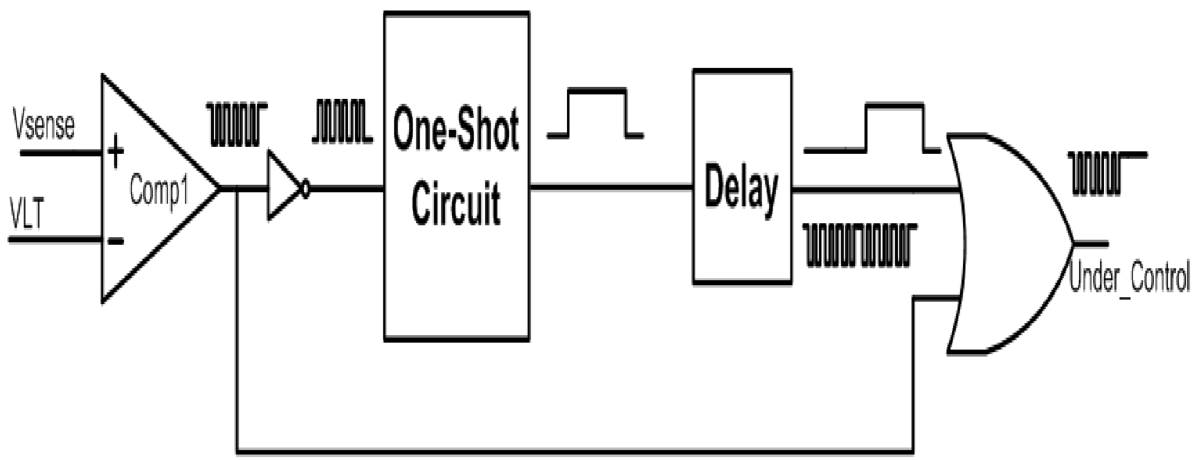
Comparison done to detect undershoot

Comparison result

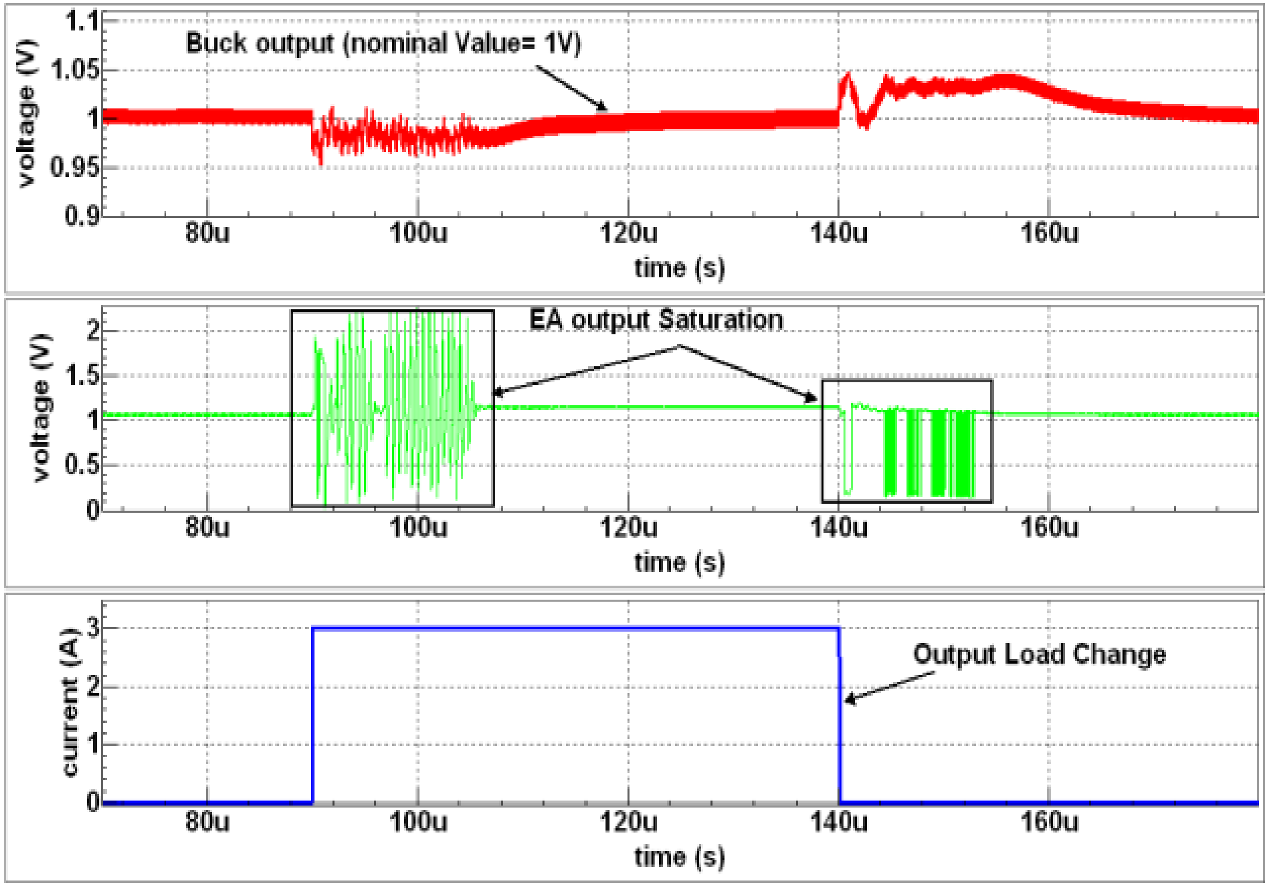
Effect of nonlinear control on EA

Nonlinear Operation Monitoring

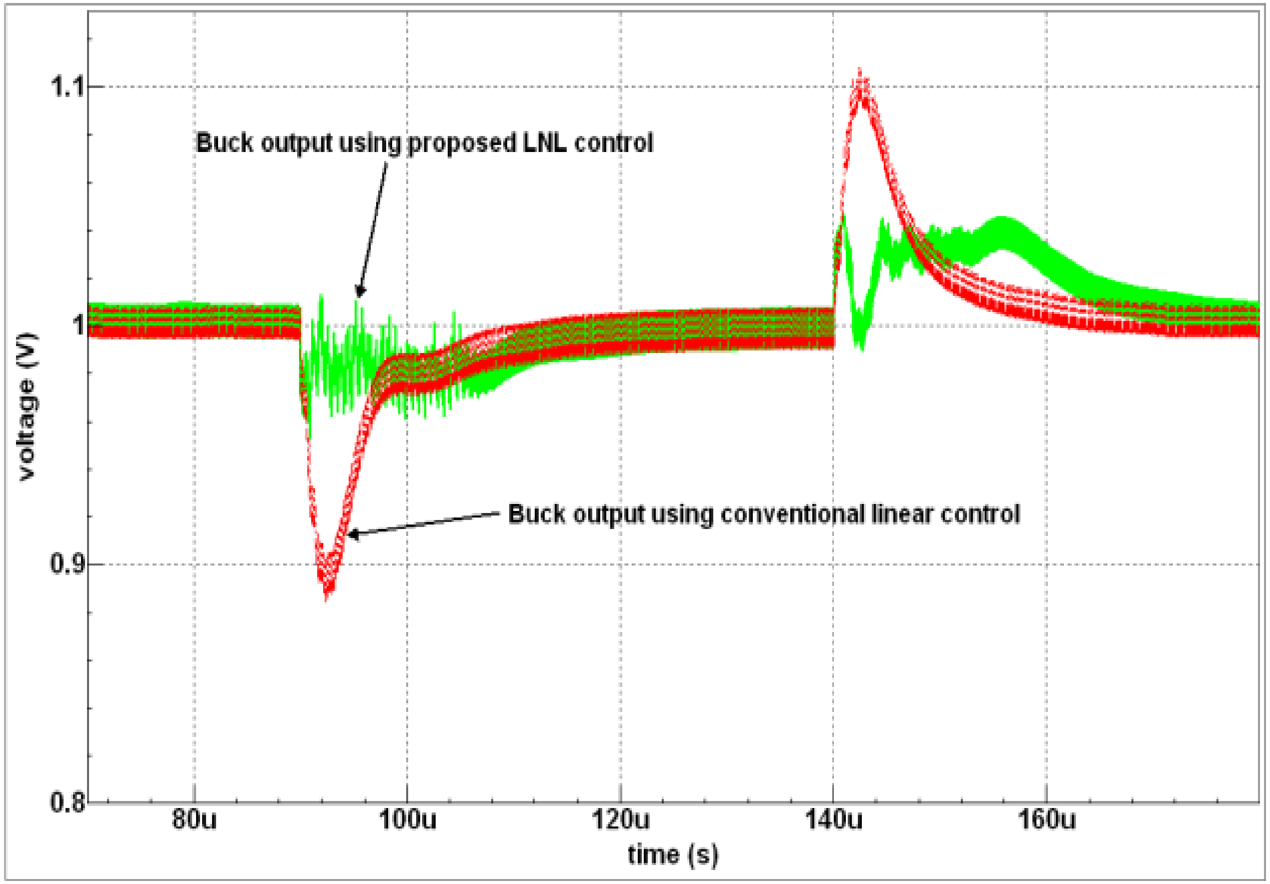
- If the nonlinear control technique is left without monitoring
  - It could continue in operation by fault and make the buck output oscillate.
  - Stability issue.



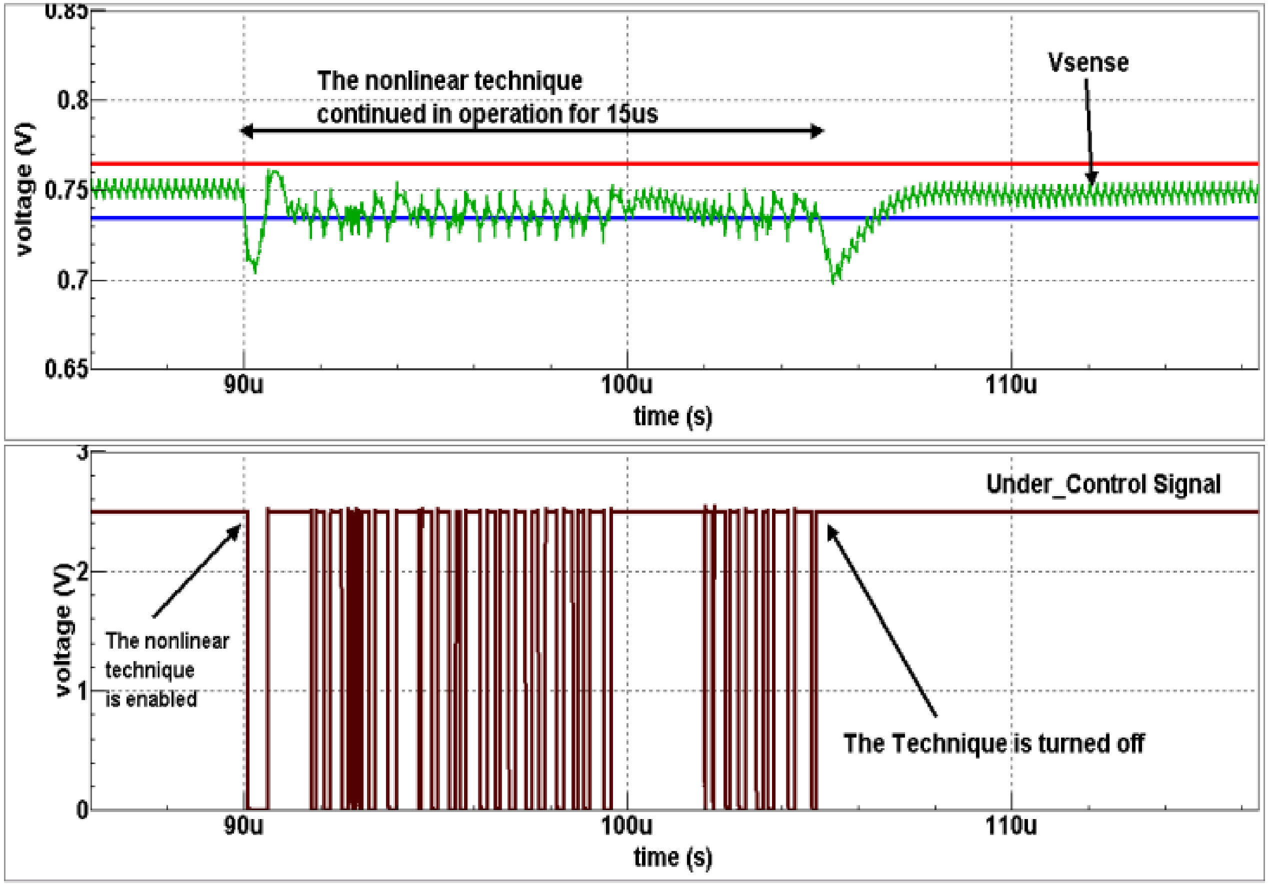
Test and Simulation



Test and Simulation (Cont..)



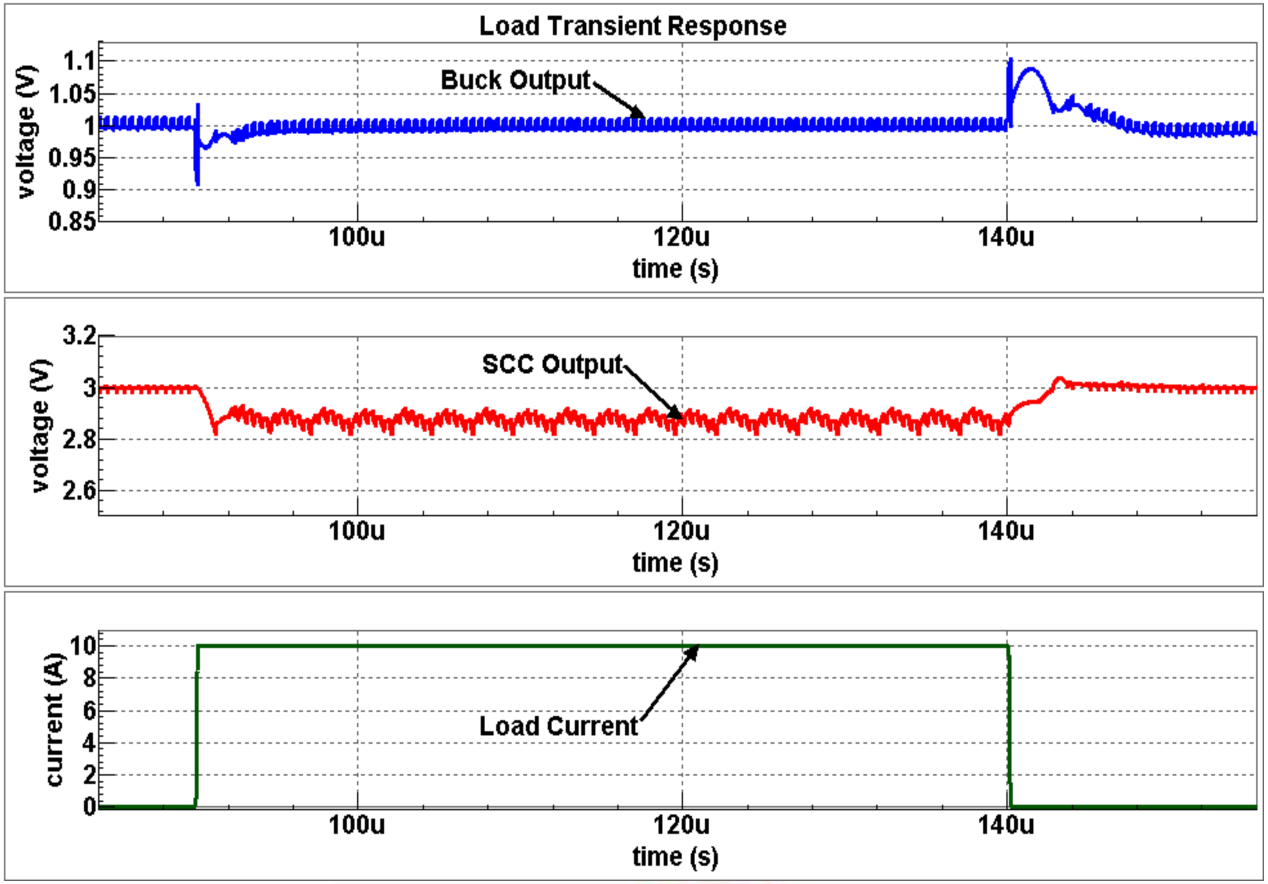
Test and Simulation (Cont..)



Test and Simulation (Cont..)

Output Capacitor Value	The Conventional Linear VM	The proposed LNL technique
47 µF (ESL=1.5 n, ESR=2 m) +10 u (ESL=0.9 n, ESR=1.5 m)	Undershoot =10.6%	Undershoot =3.9%
	Overshoot =10.1%	Overshoot = 4%
2X 12 µF (ESL=0.7 n, ESR=2 m)	Undershoot =11.6%	Undershoot = 4.5%
	Overshoot = 11.1%	Overshoot = 5.2%
12 µF (ESL=0.7 n, ESR=2 m)	Undershoot = 12.2%	Undershoot =6.9%
	Overshoot =12%	Overshoot = 4.8%

Test and Simulation (Cont..)



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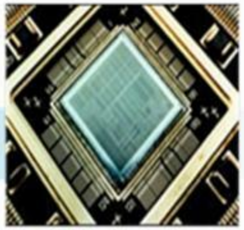
Conclusion and Future Work





Conclusion

- Converter efficiency and size are the most important issues for current consumer electronics.

- There is trade-off between system performance and system complexity.

- Tow-stage DC-DC converters can replace the conventional one-stage buck converter to get higher efficiency and better performance.

- Two-stage DC-DC converters increase the system complexity at the first glance, but replacing the high rating FETs by a lower one decreases the cost and size. At the worst case, the size of the converter would be the same of that of one-stage converters.

Conclusion

- Conventional voltage mode control in buck converter is not sufficient for fast transient response.

- Nonlinear control can be used to side by side with the conventional linear control to enhance the transient response .

- Nonlinear control not only decrease undershoot and overshoot percentages. It can be also used to obtain the same percentages with smaller output capacitor.

- Two-stage converter in addition to nonlinear control can be used to design a high performance DC-DC converter for low-power processors.

Future Work

- **Different techniques used to decrease the losses of buck converter at light loads.**
  - Most portable devices are put in idle mode (stand-by mode) when there is no operation. At this mode, the load current of DC-DC converter become very low. Efficiency at light load can shorten the battery life.

- **Design of low cost, efficient, and small size power supply for PA used in modern smart phones.**
  - PAs are very sensitive for noise comes from DC-DC converters. Linear regulator are brilliant choice for such applications. Linear regulator is not efficient. Cascading a step-up/step-down switched capacitor converter followed by a linear regulator would be more advantageous.

Publications

- Yasser Noor, Shimaa Nagar, **Mohamed Saad**, Mohamed Orabi, "MOSFET gate drive circuit design considerations for integrated high switching frequency buck converter", Published in the first International Conference of Energy Engineering, Dec 2008 Egypt.

- **Mohamed Saad**, Mohamed Orabi, El-Sayed Hasaneen, Ashraf Lotfi, " Design of Integrated High Efficiency Two Stage POL DC-DC Converter", Published in the International Middle-East Power System Conference, Dec 2010 Egypt.

- **Mohamed Saad**, Mohamed Orabi, El-Sayed Hasaneen, Ashraf Lotfi, "A Novel Linear-Nonlinear Technique for Fast Transient Buck Converter", IEEE Telecommunications Energy Conference, 2011, INTELEC 2011.

- **Mohamed Saad**, Mohamed Orabi, El-Sayed Hasaneen, Ashraf Lotfi, "Low-Cost Efficient Tow-Stage POL Power Supply", IEEE Telecommunications Energy Conference, 2012, INTELEC 2012.

Discussion

Thanks