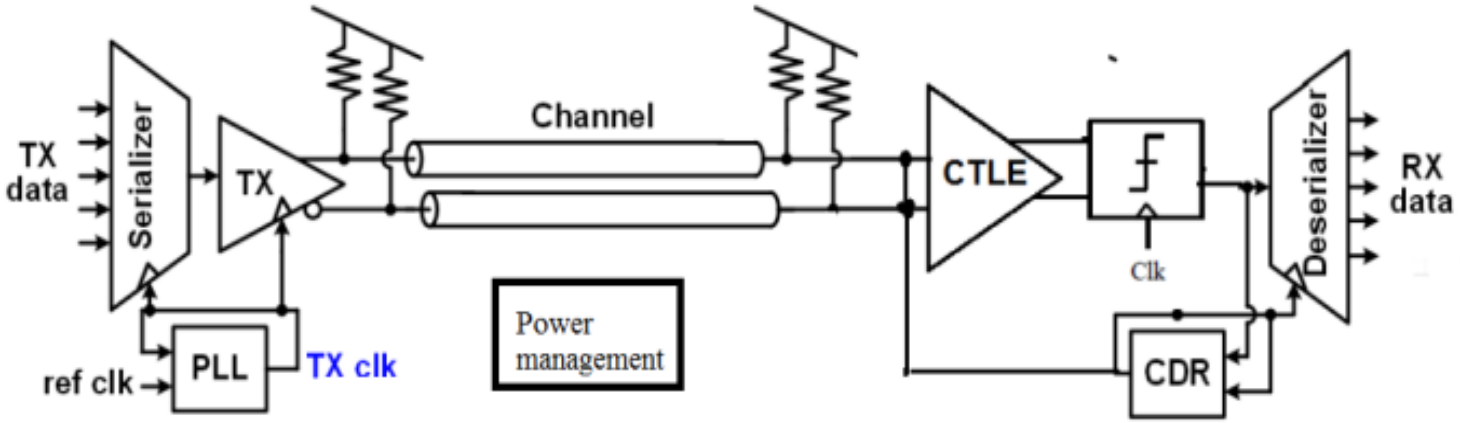
ASU-MIPEX Graduation Project 2013

High Speed Serial Links

Supervised by: Dr. Sameh Assem Ibrahim

High Speed Serial Links



System Block Diagram

Outlines

- Bias Cell
- LDO
- Transmitter
- Receiver
- PLL

Bias Cell

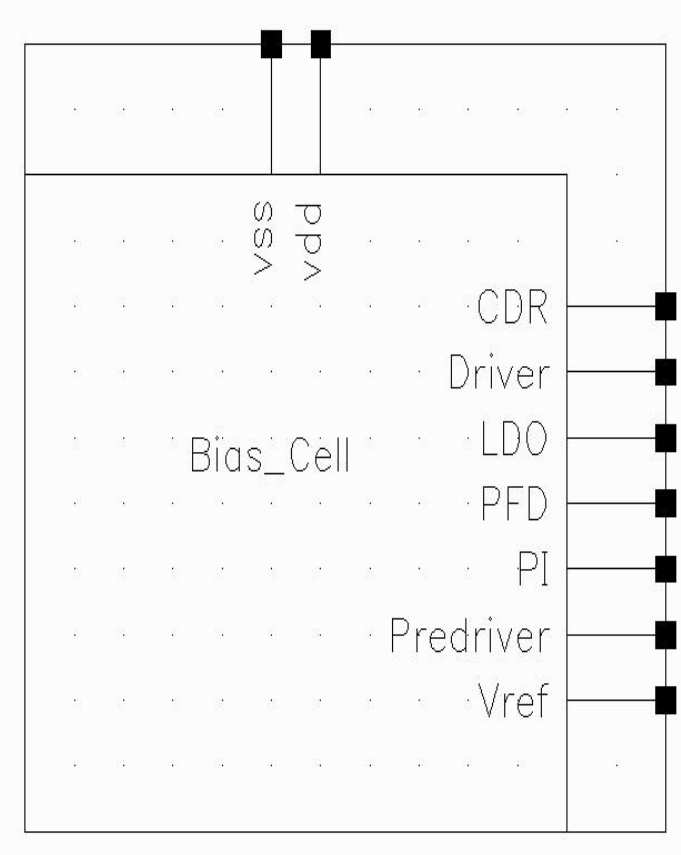
Presented by : Salma El-Sawy

Outlines

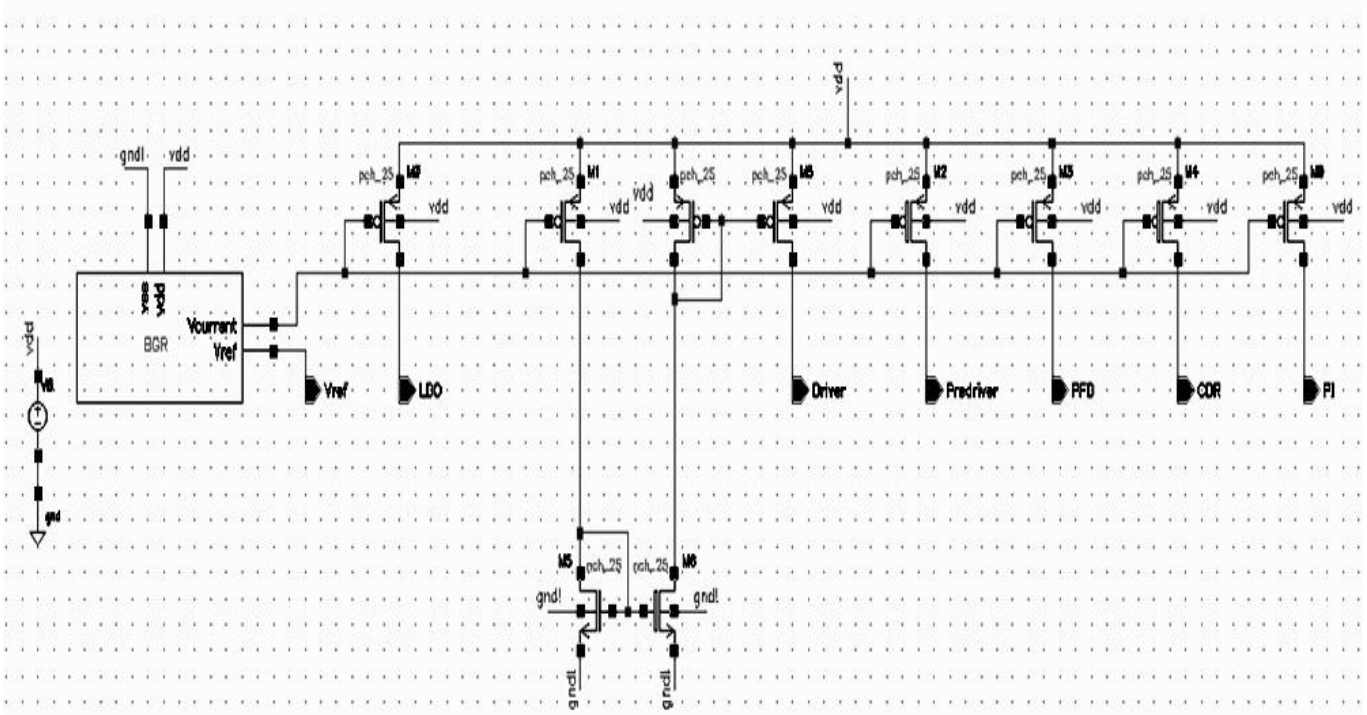
- Bias Cell
- Band gap Reference circuit1
- Band gap Reference circuit2
- Comparison and Decision
- Startup circuit
- Folded Cascode OTA
- Biasing Folded Cascode
- Corners

Bias Cell

- The bias Cell is an important block, to provide the system block the desired Currents
- It is also necessary for providing a Constant reference voltage with the variations of the Supply and temperature



Bias Cell

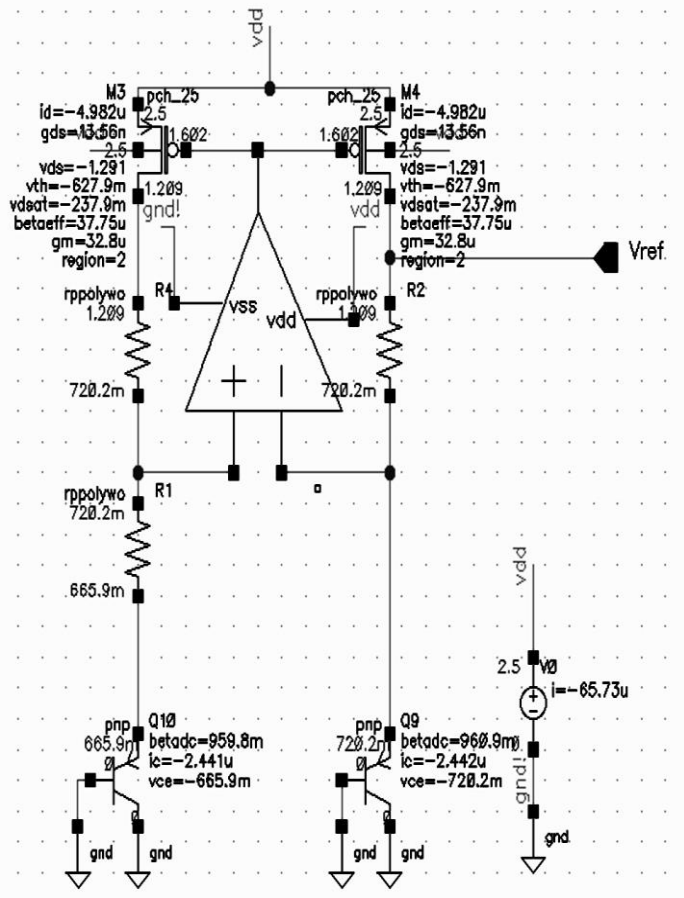


- The Bias Cell is a simple circuit that is constructed from a BGR circuit and current mirrors providing the blocks the current they desired

Band Gap Reference Circuit

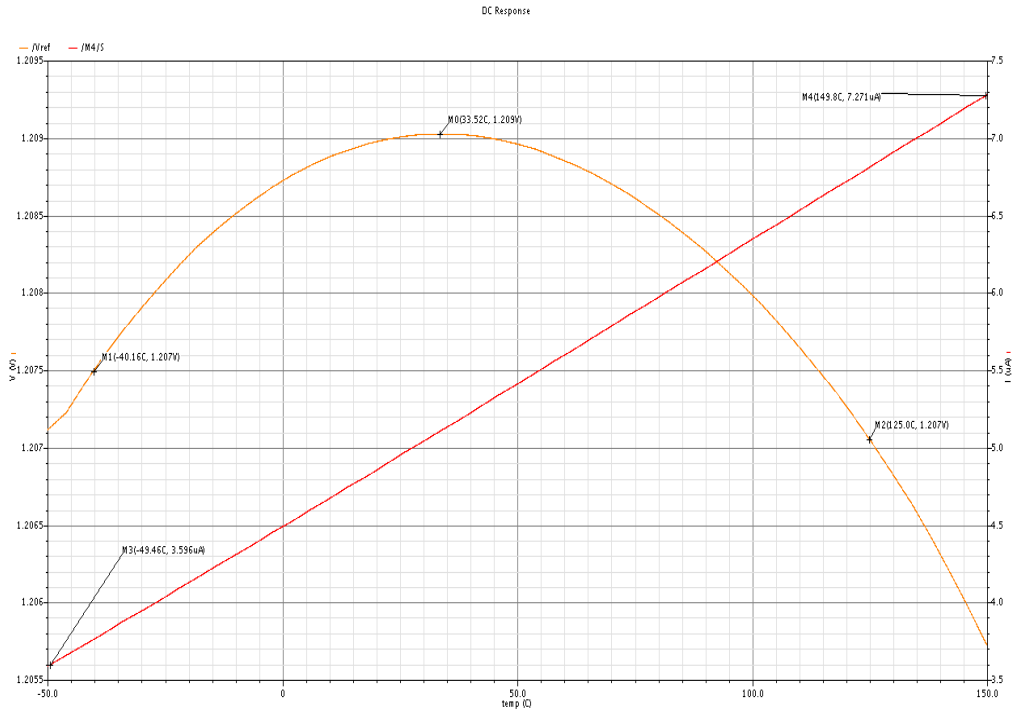
BGR with PTAT current

- This band Gap Circuit Provide Constant Vref across PVT
- And Provide a PTAT current that increases with the Temperature



Band Gap Reference Circuit

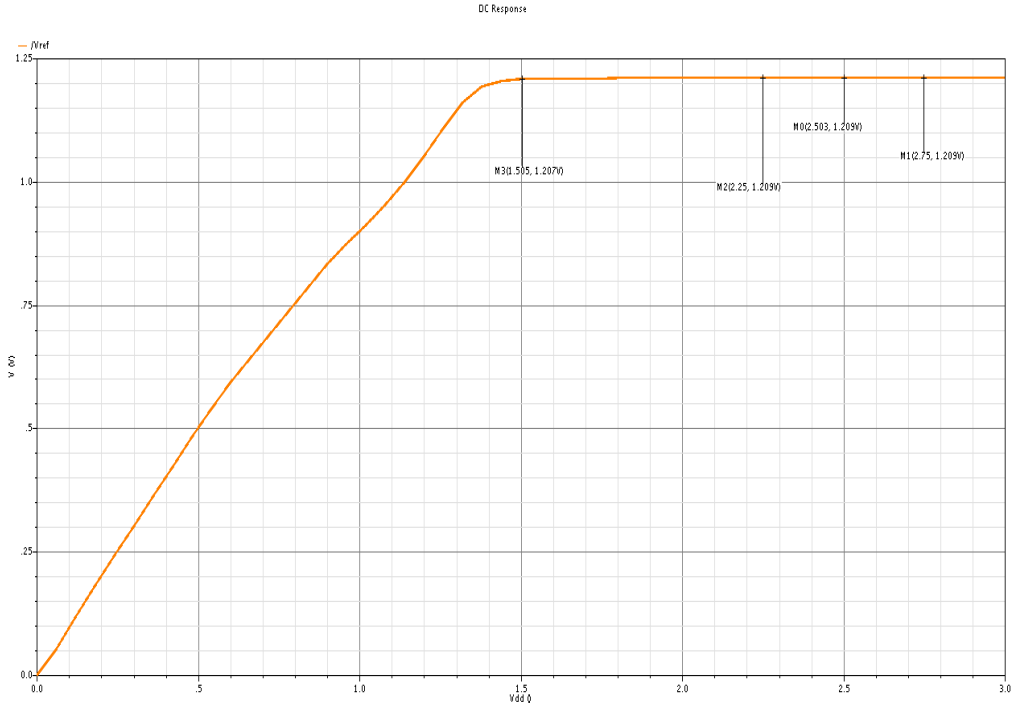
BGR with PTAT current Outputs :-



- This shows Vref and Iref Vs. Temperature
- Where the Voltage varies 2mV in the temperature interval [-40,125]

Band Gap Reference Circuit

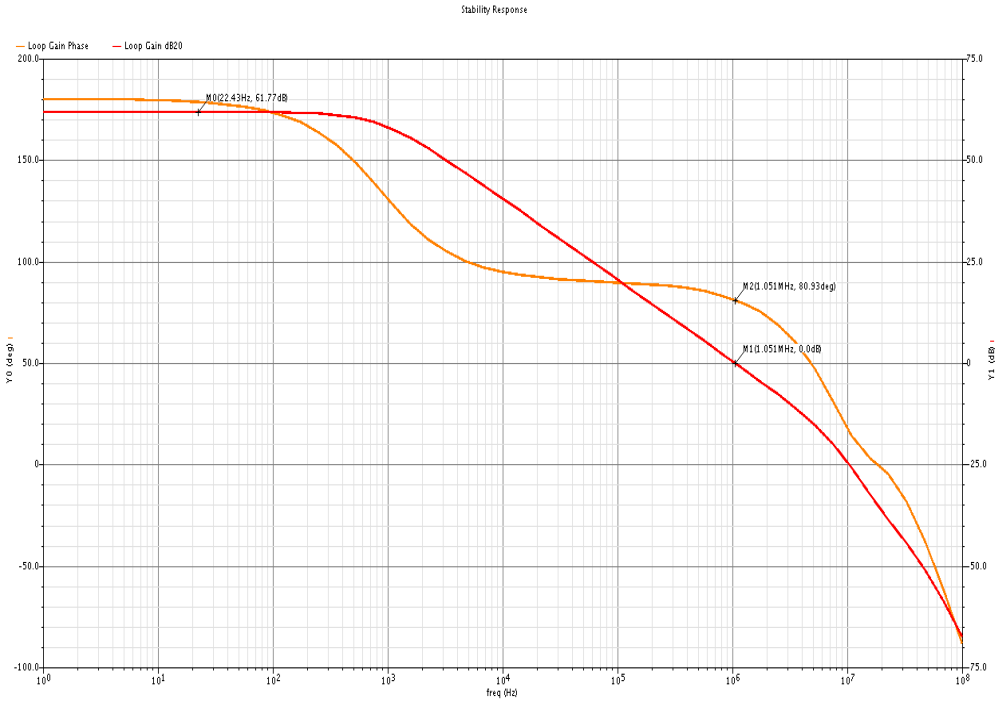
BGR with PTAT current Outputs :-



- This shows Vref Vs. supply variations
- Which shows that Vref is almost unchanged for 10% variation of the supply, also the circuit will function properly till 1.5v supply

Band Gap Reference Circuit

BGR with PTAT current Outputs :-

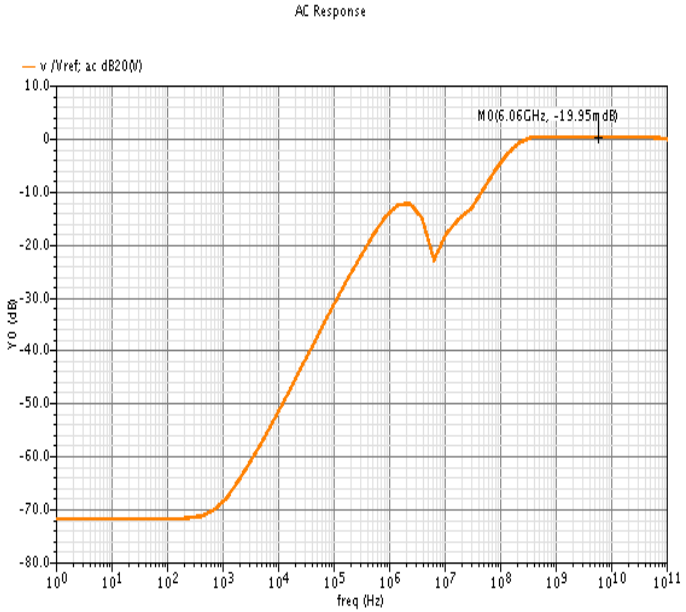


- This shows the stability analysis of our BGR
- Where the PM=80.93 degree

Band Gap Reference Circuit

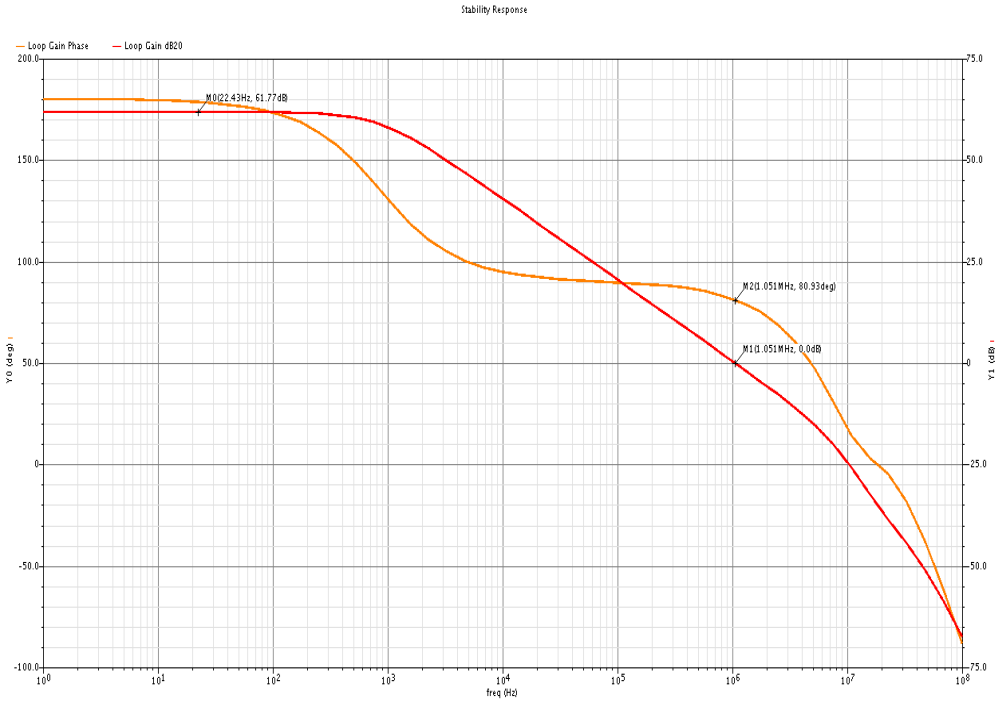
BGR with PTAT current Outputs :-

- The PSR is as shown in figure =19.95m dB
- Which isn't a good rejection ratio



Band Gap Reference Circuit

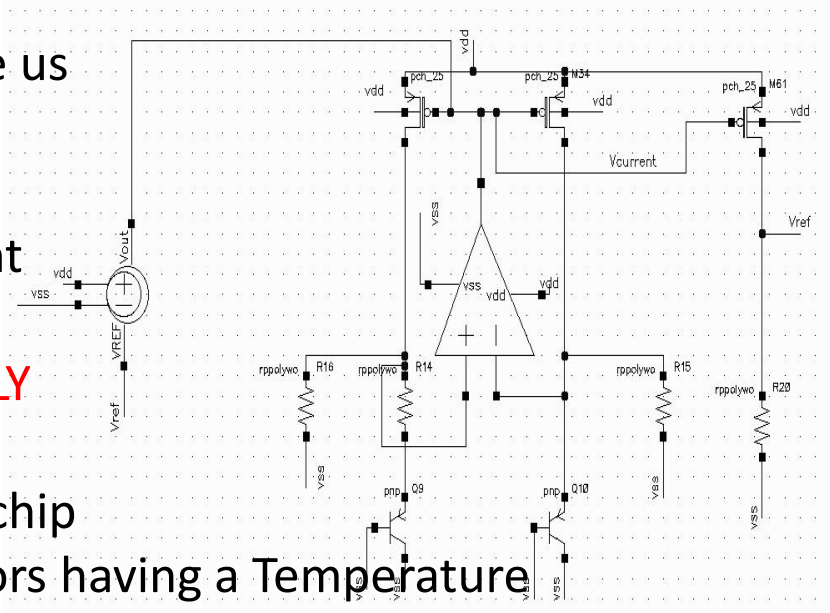
BGR with PTAT current Outputs :-



- This shows the stability analysis of our BGR
- Where the PM=80.93 degree

Band Gap Reference Circuit

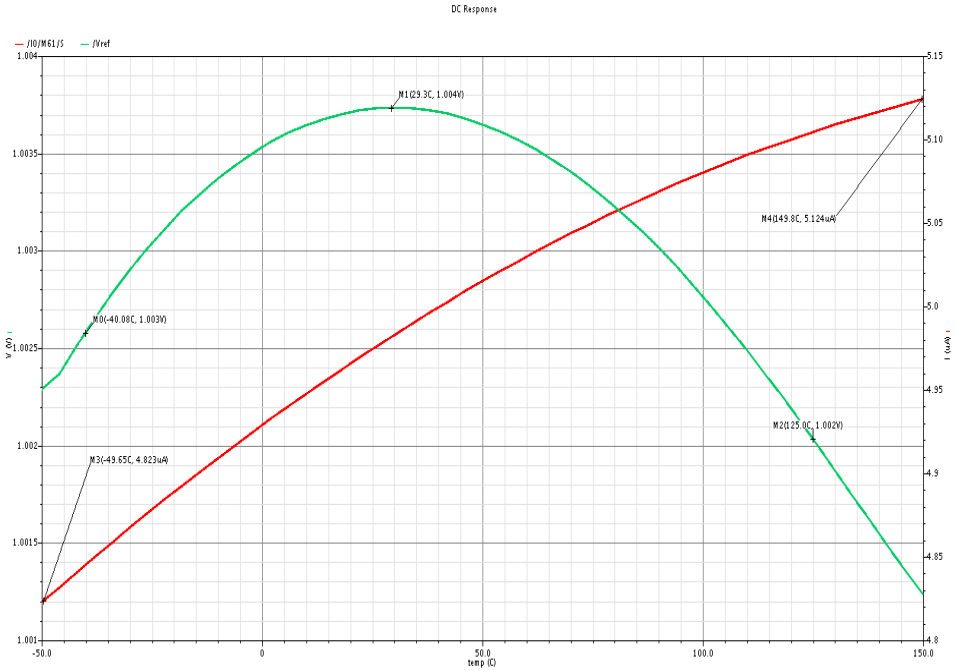
CMOS BGR with Sub-1-V operation.



- This BGR Provide us Both Constant Voltage and Constant Current references
- BUT, PRACTICALLY due to that our resistors are on chip non ideal resistors having a Temperature Coefficient.it is not the case
- You can get either Constant current OR Constant Voltage by adjusting the Resistors ratios

Band Gap Reference Circuit

CMOS BGR with Sub-1-V operation “Outputs”.



- This shows Vref and Iref Vs. Temperature
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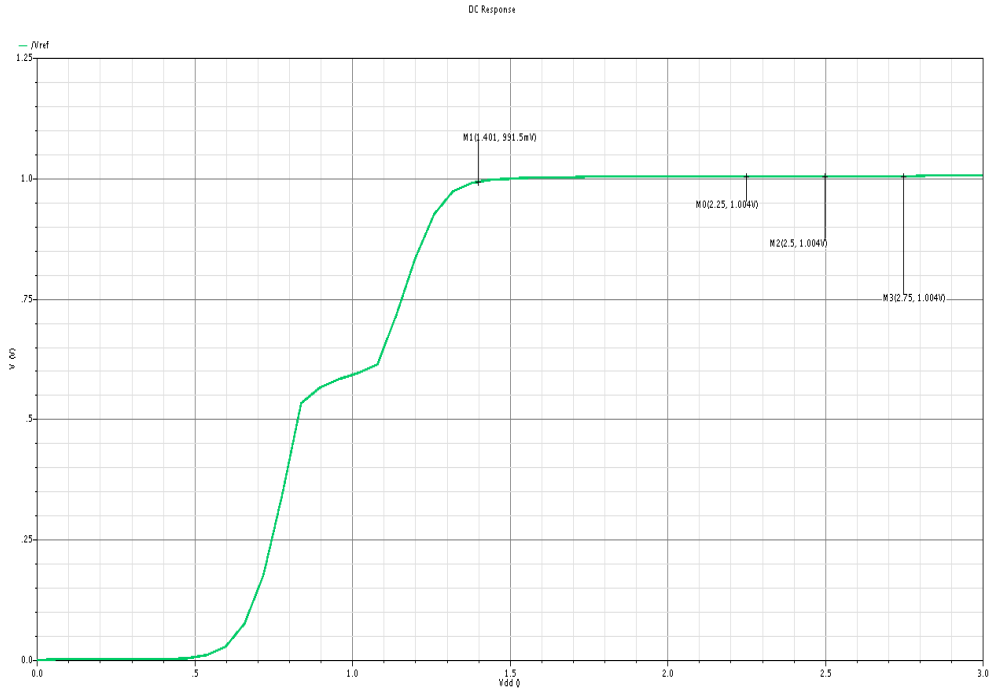
Band Gap Reference Circuit

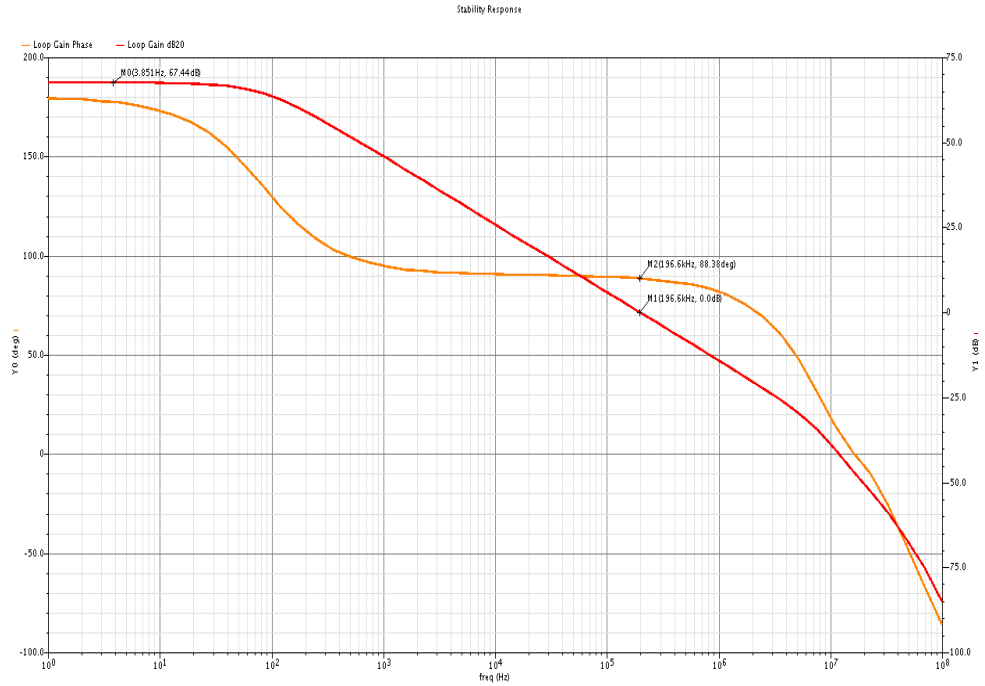
CMOS BGR with Sub-1-V operation “Outputs”.



- This shows Vref Vs. supply variations
- Which shows that Vref is almost unchanged for 10% variation of the supply, also the circuit will function properly till 1.4v supply

Band Gap Reference Circuit

CMOS BGR with Sub-1-V operation “Outputs”.

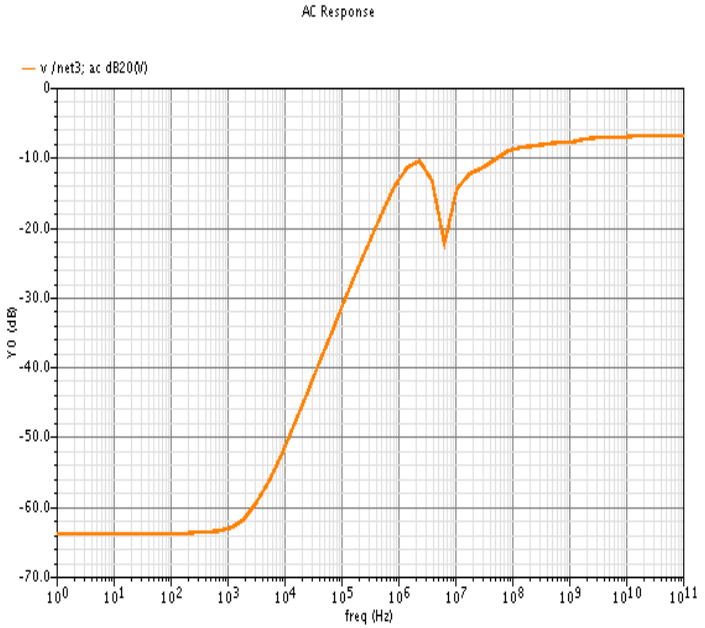


- This shows the stability analysis of our BGR
- Where the PM=88.38 degree

Band Gap Reference Circuit

CMOS BGR with Sub-1-V operation “Outputs”.

- The PSR is as shown in figure =-7 dB
- Which is a better Ratio.



Comparison and Decision

Points of Comparison	BGR with PTAT Current Output	BGR with Sub 1-V oper
VREF	Can't be controlled always =1.206v Varies with temp 2mV	Designed to be 1V "adj Varies with temp 2
IREF	PTAT current Increase with Temperature	Constant current , BU due to no ideal Resi
Stability	Good stability Depending on the design of the OTA	
PSR	Bad	Good
TC	$10.034 * 10^{-6}$ppm/c	$12.0849 * 10^{-6}$ pp

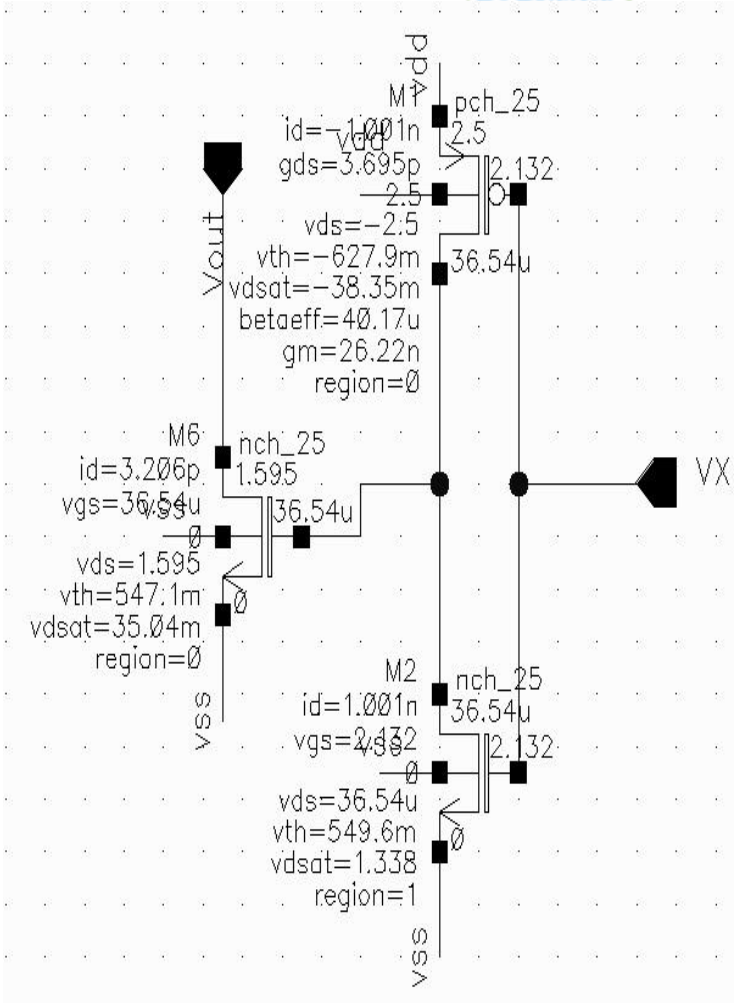
That is Why I Decide to Use the BGR with 1-V operation

Startup Circuit

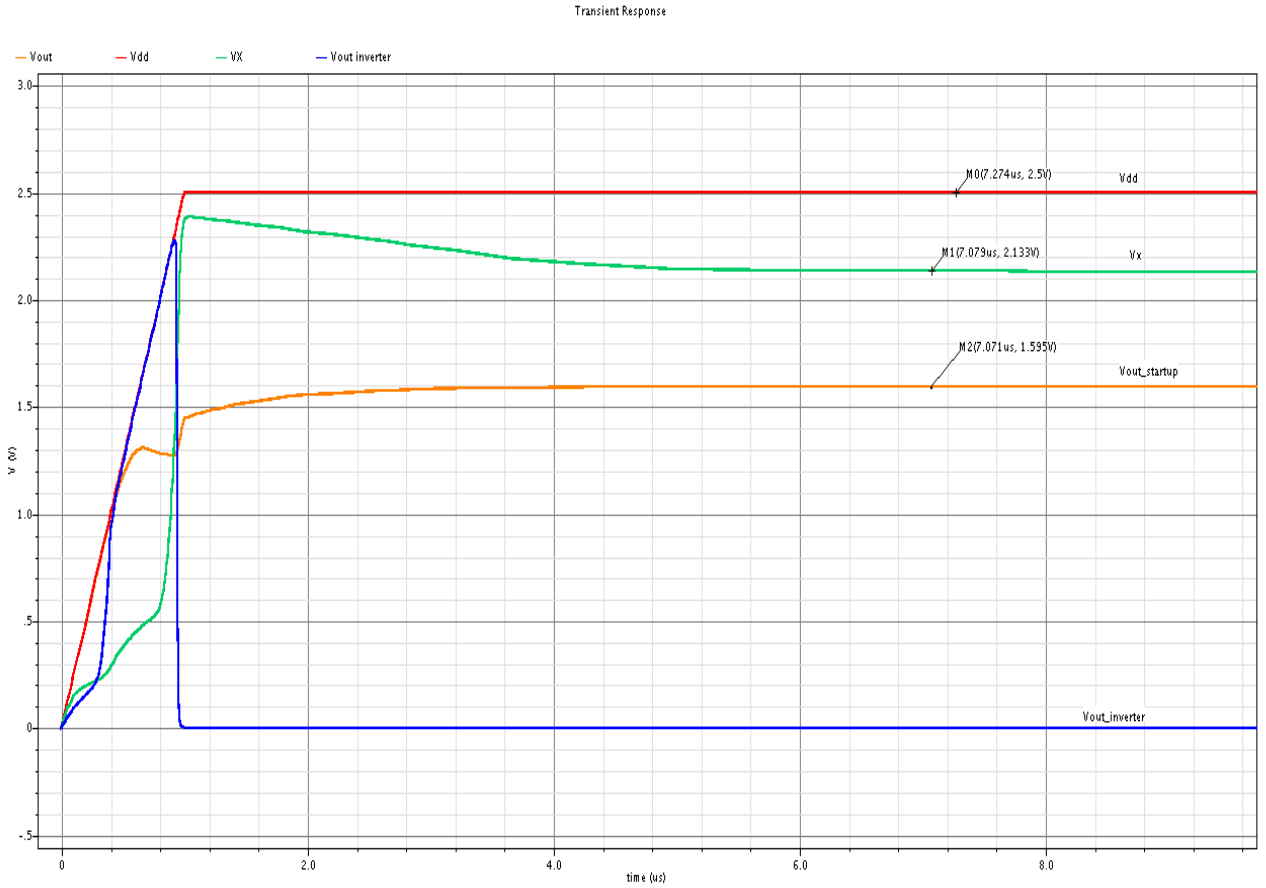
- This startup Circuit is an important part of the BGR circuit
- Where the BGR have a parasitic operating point when the Current is equal to zero
- In order to move from this point to the desired operating point we inject a current in the band Gap at its startup.
- Then the Startup Circuit is Designed to be switched off when the BGR reach its steady State.

Startup Circuit

- This startup circuit consist of an inverter and an NMOS.
- Initially I=0, then Vx=0 so the output of the inverter is Vdd
- so M6 is ON passing current in the BGR so Vx start to increase till the output of the inverter is Low M6 is OFF, when we reached the steady state.



Startup Circuit

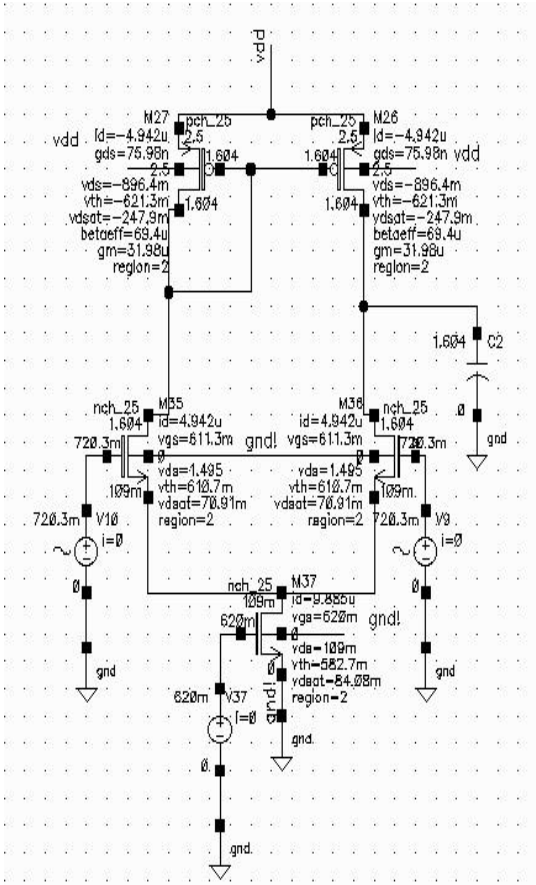


OTA's

- OTA is used as a Feedback Element To adjust the 2 point VA and VB for the functionality of the BGR.
- Also it is used for biasing the BGR PMOS with its desired input
- In this part of the presentation I will be discussing Different Topologies of OTA and why Did I made that Choice.

OTA's

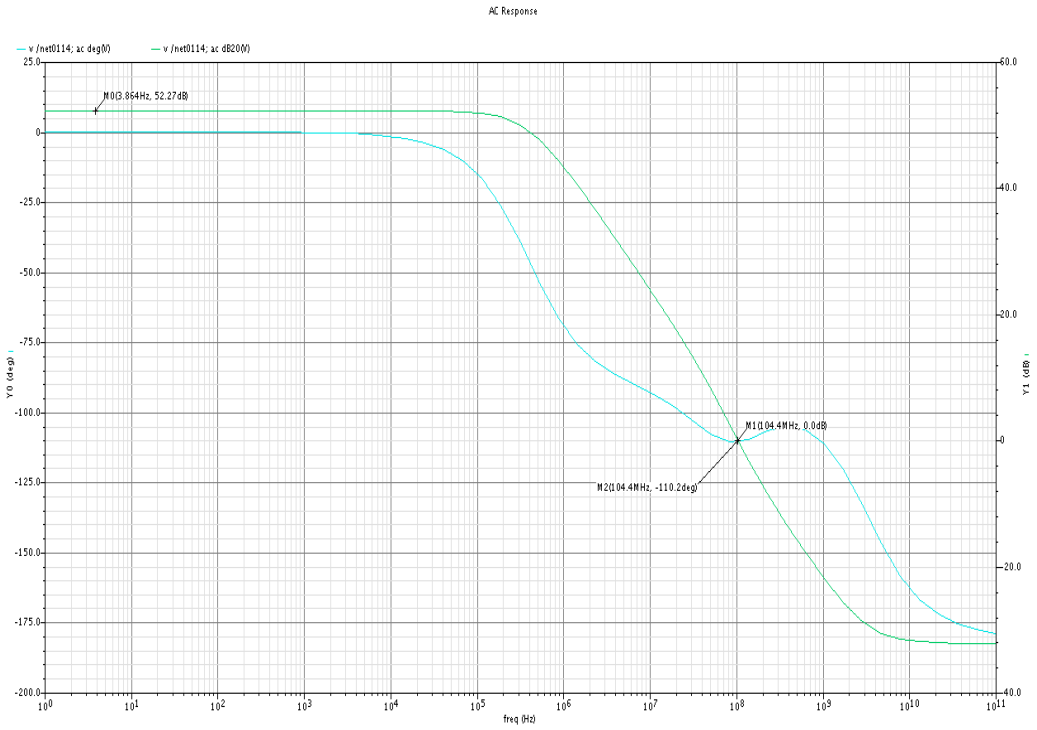
NMOS single ended Simple OTA:-



- In order to Get the Desired VCM.
- We found that the Transistors Vod is <100m
- Which leads to increasing the probability for the mosfet to enter the Sub threshold.

OTA's

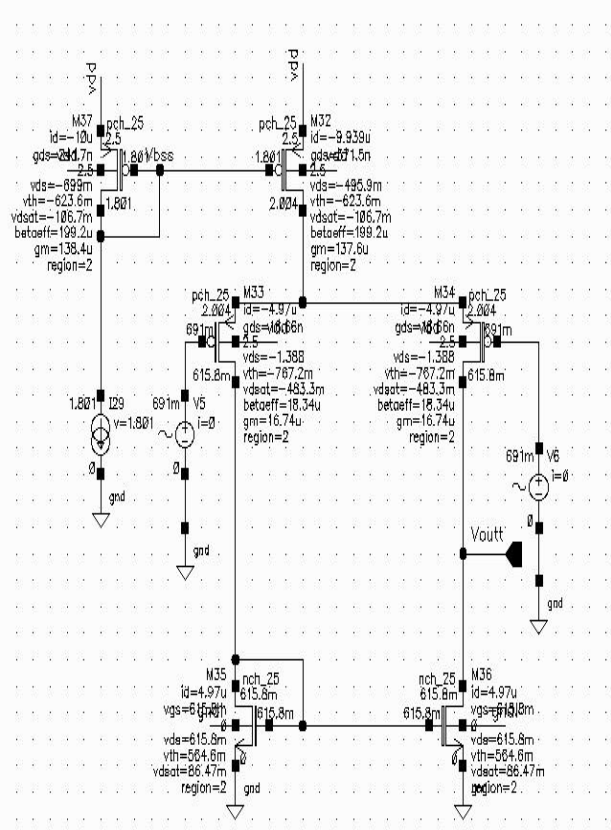
NMOS single ended Simple OTA:-



- OTA Stability and Gain . Where the gain is 52dB and the PM is 69.8degree.

OTA's

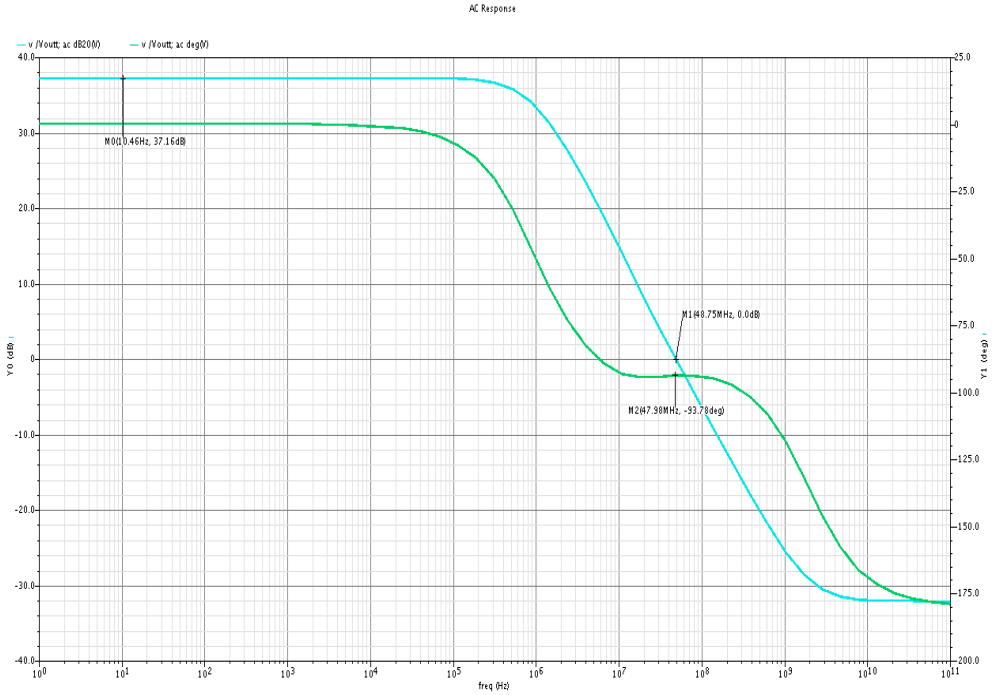
PMOS single ended Simple OTA:-



- Finding that the input CM is so small so I used PMOS Simple OTA
- We found that the Transistors Vod is <100m
- Which leads to increasing the probability for the mosfet to enter the Sub threshold.
- And also couldn't achieve the desired Output VCM.

OTA's

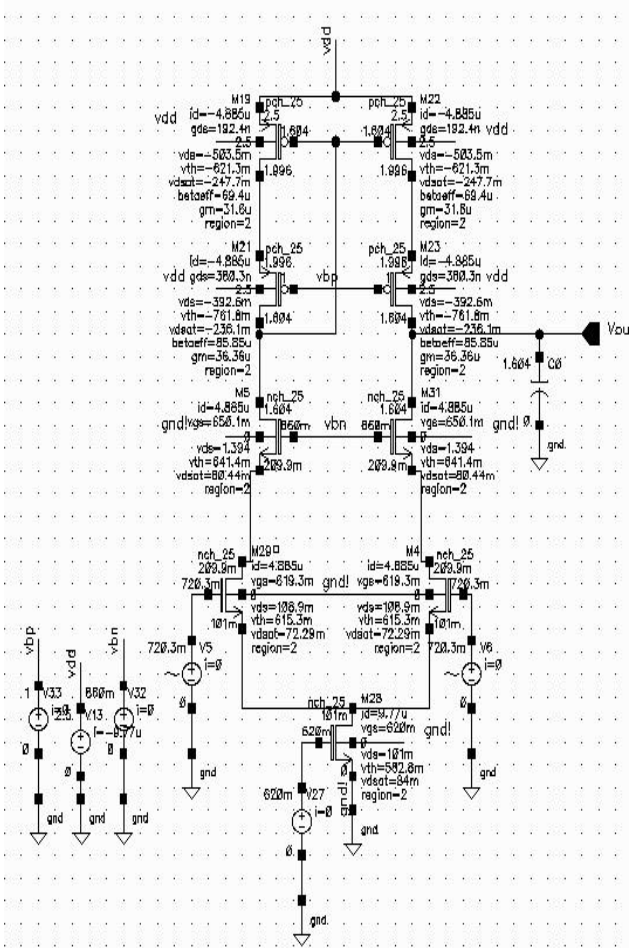
PMOS single ended Simple OTA:-



- OTA Stability and Gain . Where the gain is 37dB and the PM is 86.25degree.

OTA's

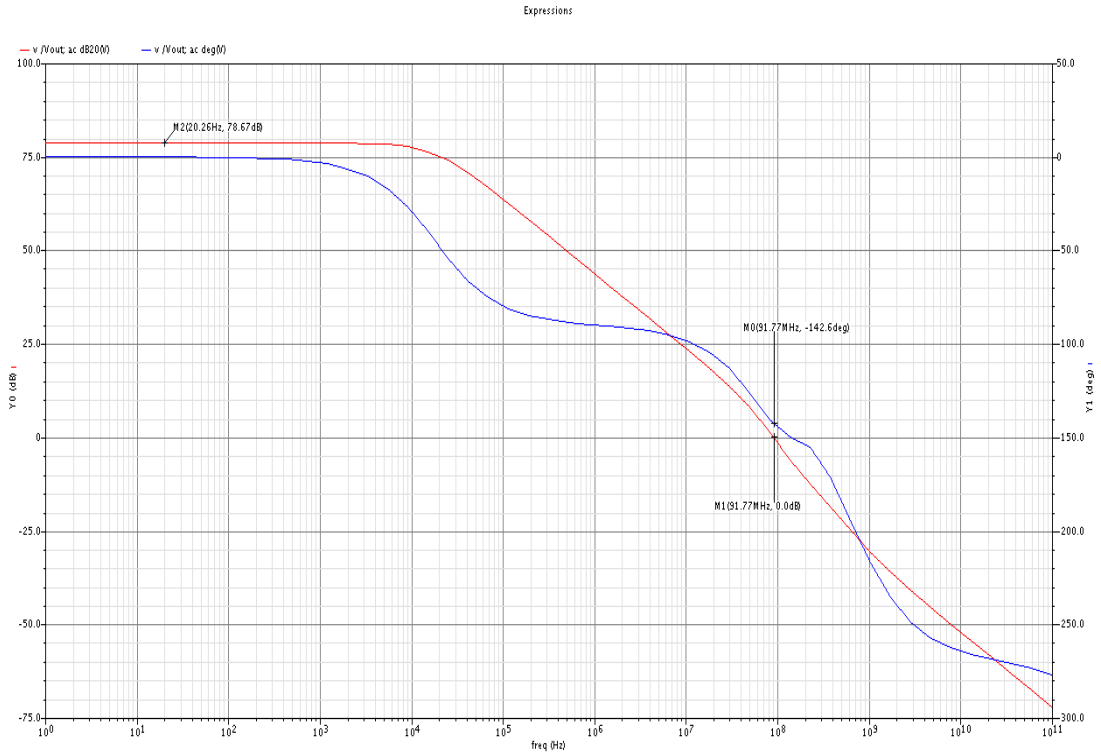
NMOS single ended Telescopic OTA:-



- In order to Get the Desired VCM.
- We found that the Transistors Vod is <100m
- Which leads to increasing the probability for the mosfet to enter the Sub threshold.

OTA's

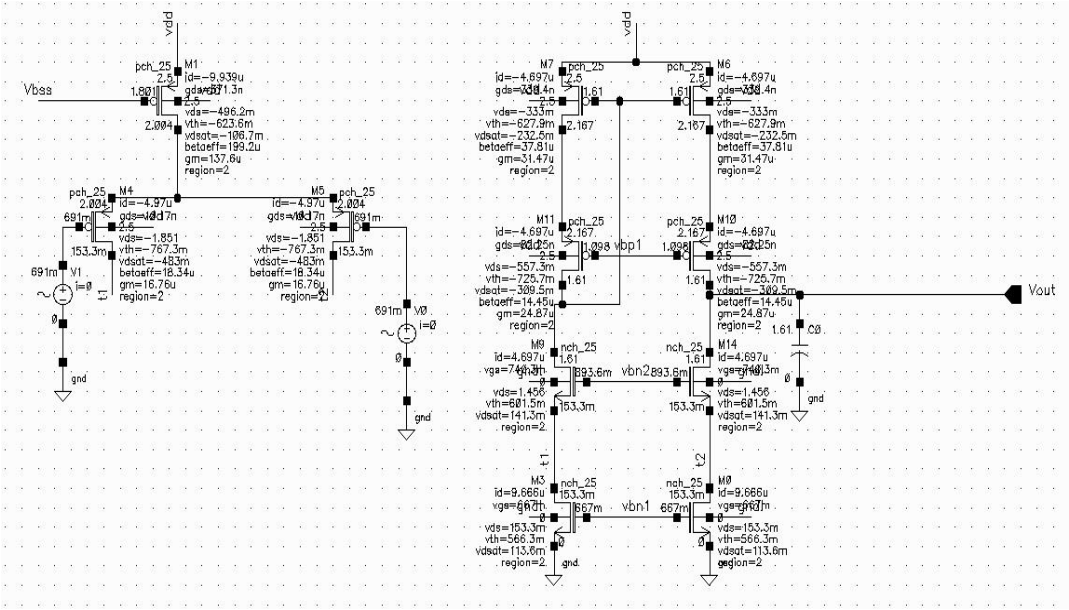
NMOS single ended Telescopic OTA:-



- OTA Stability and Gain . Where the gain is 78dB and the PM is 37.4 degree.

OTA's

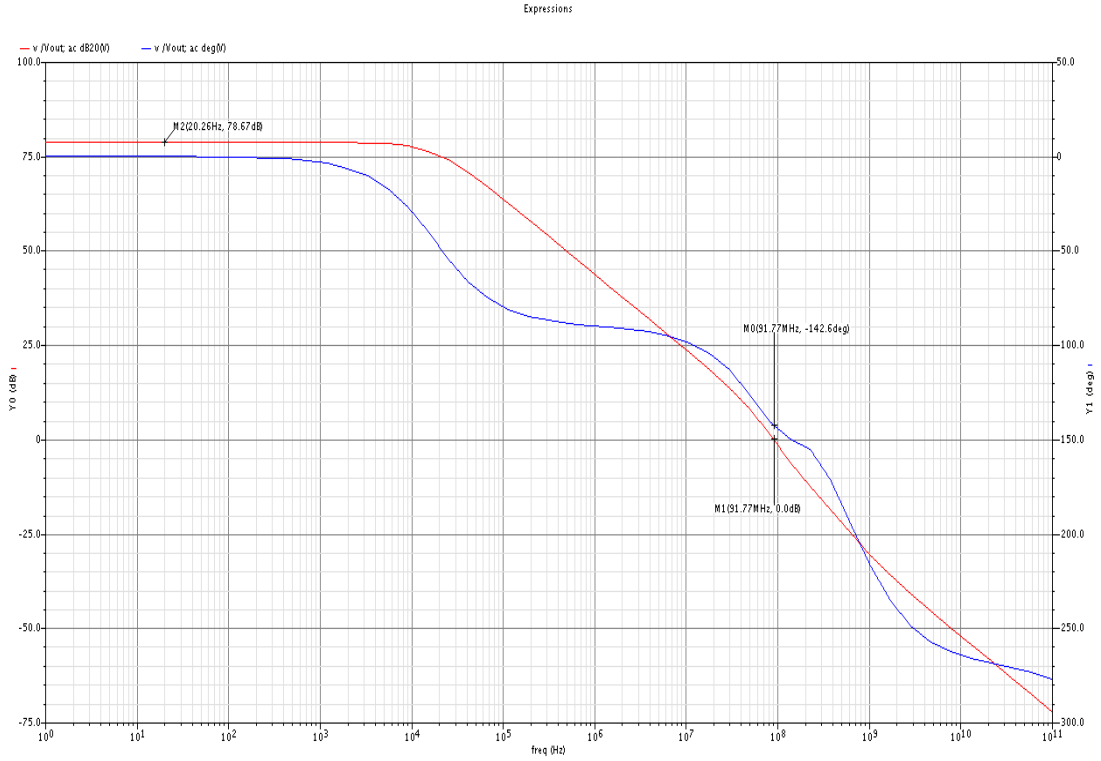
PMOS single ended Folded Cascode OTA:-



- Since my input is small I used PMOS input
- Getting the desired VCM output
- All transistors Vod>100m decreasing Prob. Of entering region 3

OTA's

PMOS single ended Folded Cascode OTA:-



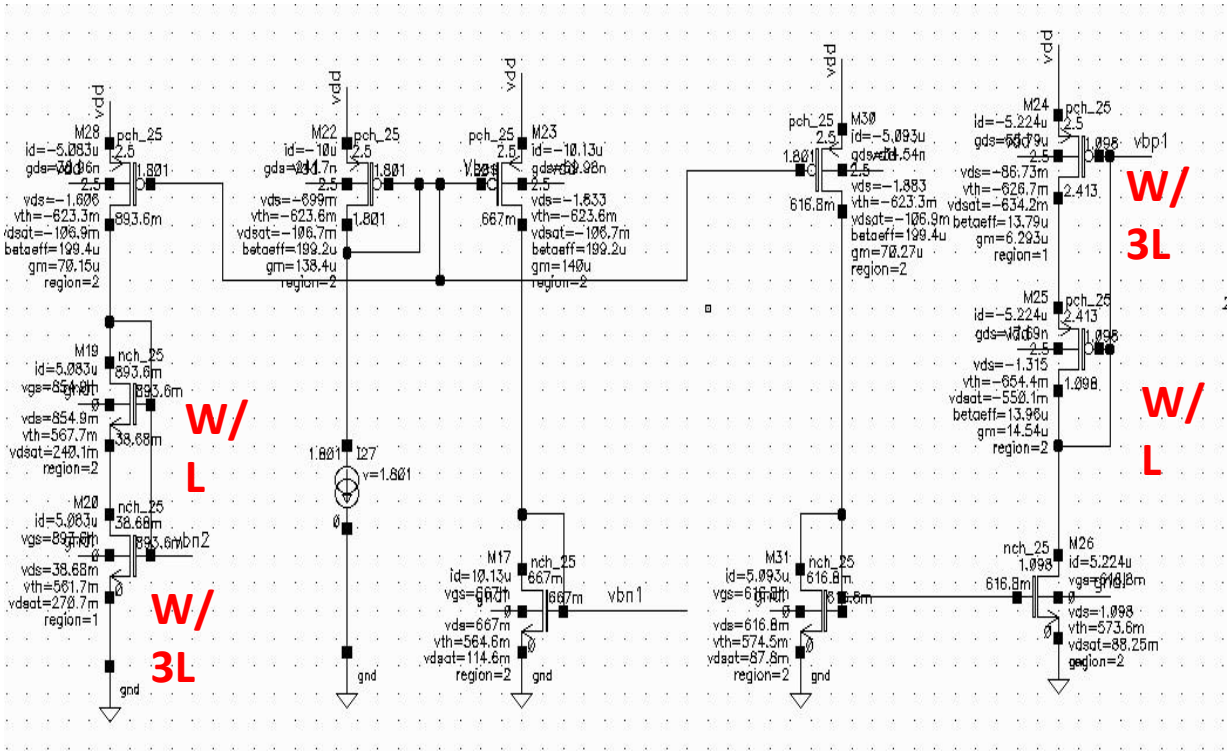
- OTA Stability and Gain . Where the gain is 70.5dB and the 68 PM is degree.

Comparison and Decision

Points of Comparison	NMOS i/P Simple OTA	PMOS i/P Simple OTA	NMOS i/P Telescopic	PMOS i/P Folded cascode
Gain	Small	Small	Large	Large
Stability	Uncondition ally	Stable	Conditionall y	Stable
Vod	<100mV	<100mV	<100mV	>100mv
Input Voltage	Vi= Vodss +Vod1+Vth Large	Vi=Vdd-Vodss- Vod1-Vth Small	Vi= Vodss +Vod1+Vth Large	Vi=Vdd-Vodss- Vod1-Vth Small

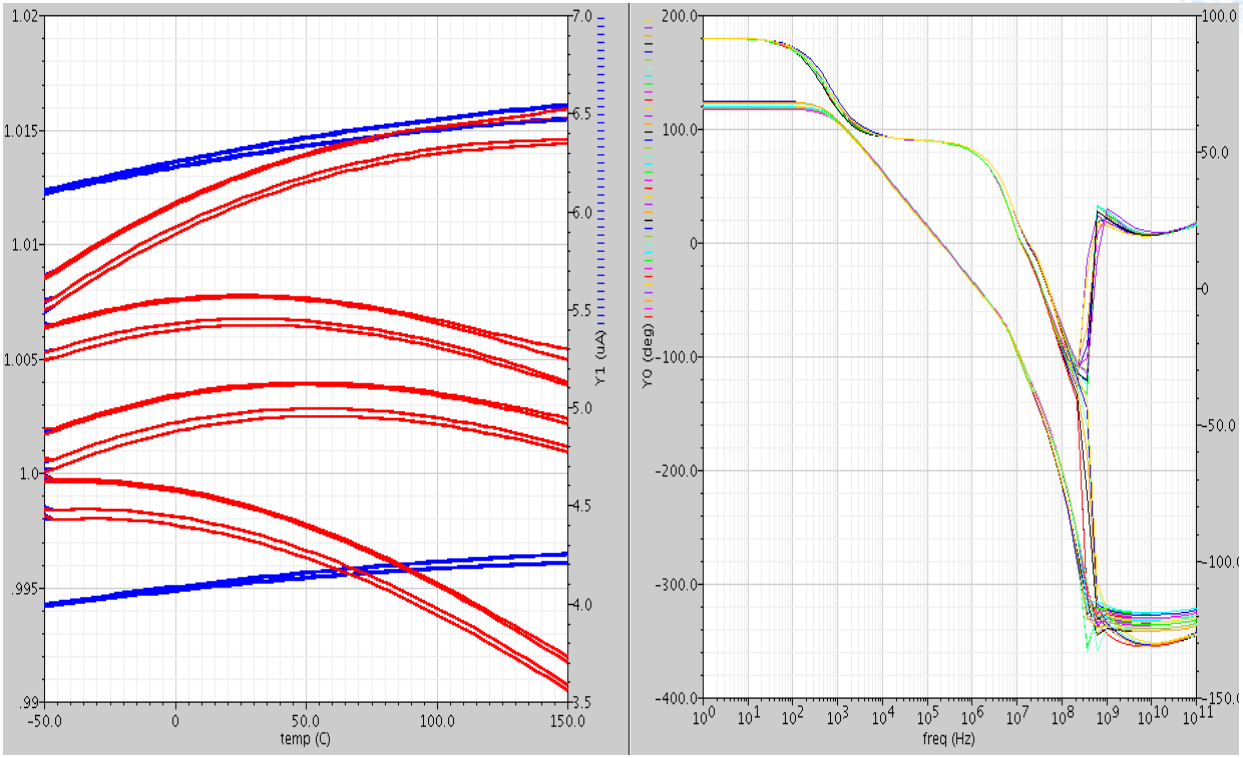
- I chose the Folded Cascode to give me a reasonable gain, desired Output Common mode and chose it to be PMOS input for My Small input Common Mode.

Biasing Folded cascode



- Used To bias the Folded Cascoded OTA Circuit

Corners



- Using an Ocean Code to run all Possible corners to get that the Stability is almost the same across corners

LDO

Presented by : Sherif El-Hosainy

Outlines

- LDO introduction
- External Cap LDO
- Cap Less LDO
- Final Circuit
- Conclusion

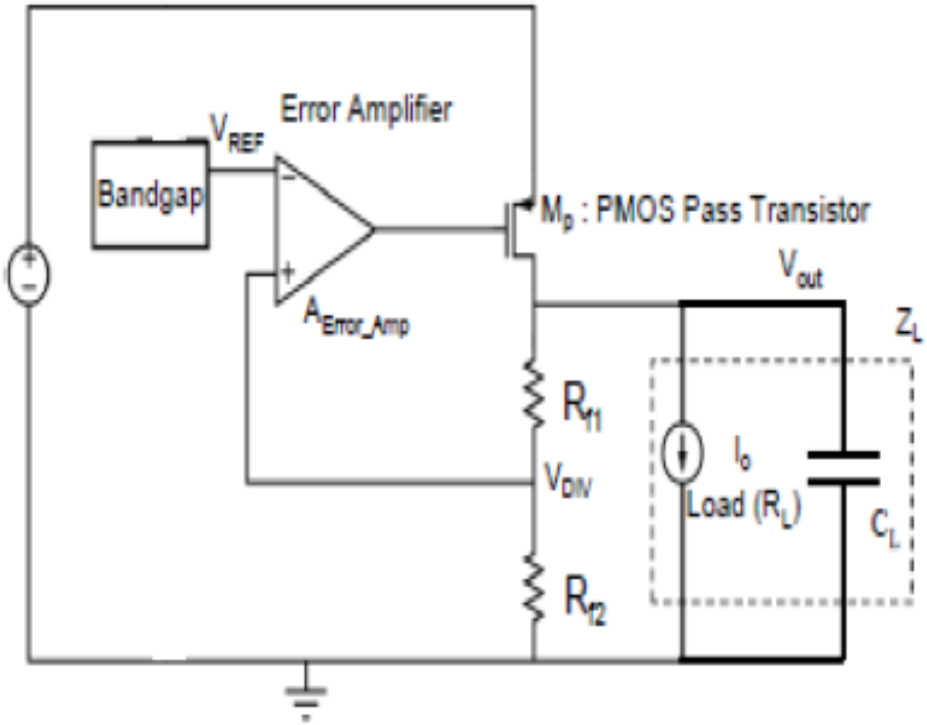
LDO introduction

- LDO Block Diagram
- Stability
- Transient

$$\Delta Vtr = \frac{Imax \,.\, \Delta t}{Cout}$$

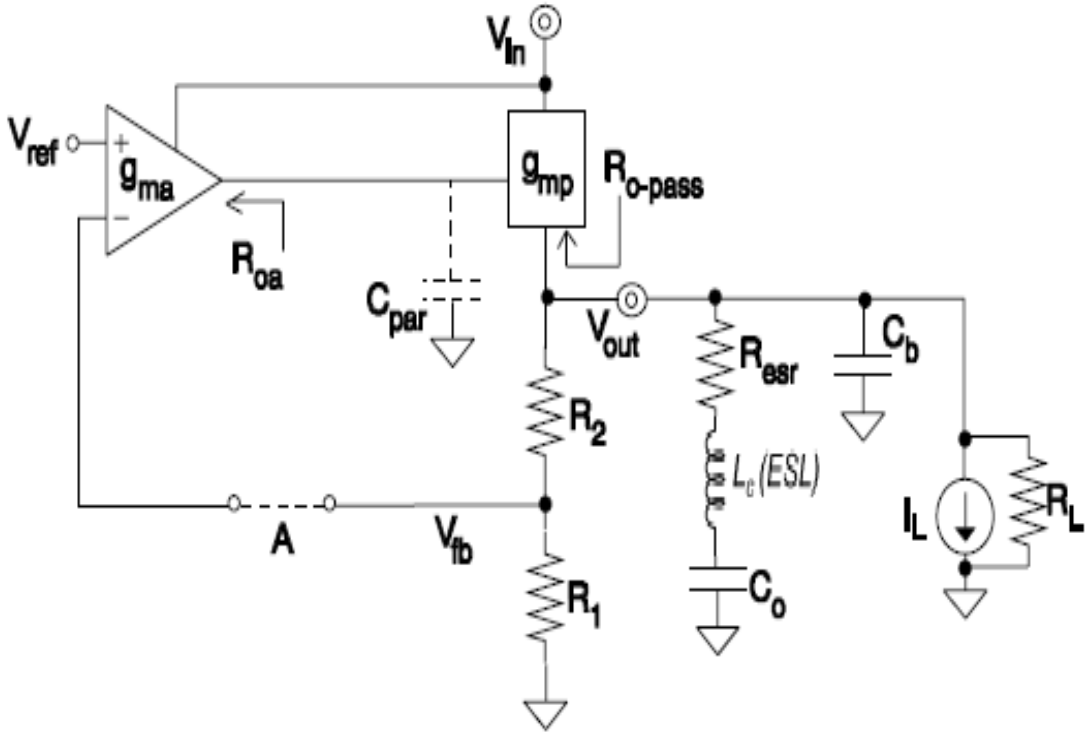
$$\Delta t = \frac{1}{BW}$$

- Two Topologies of LI
  1. External Cap LDO
  2. Cap Less LDO



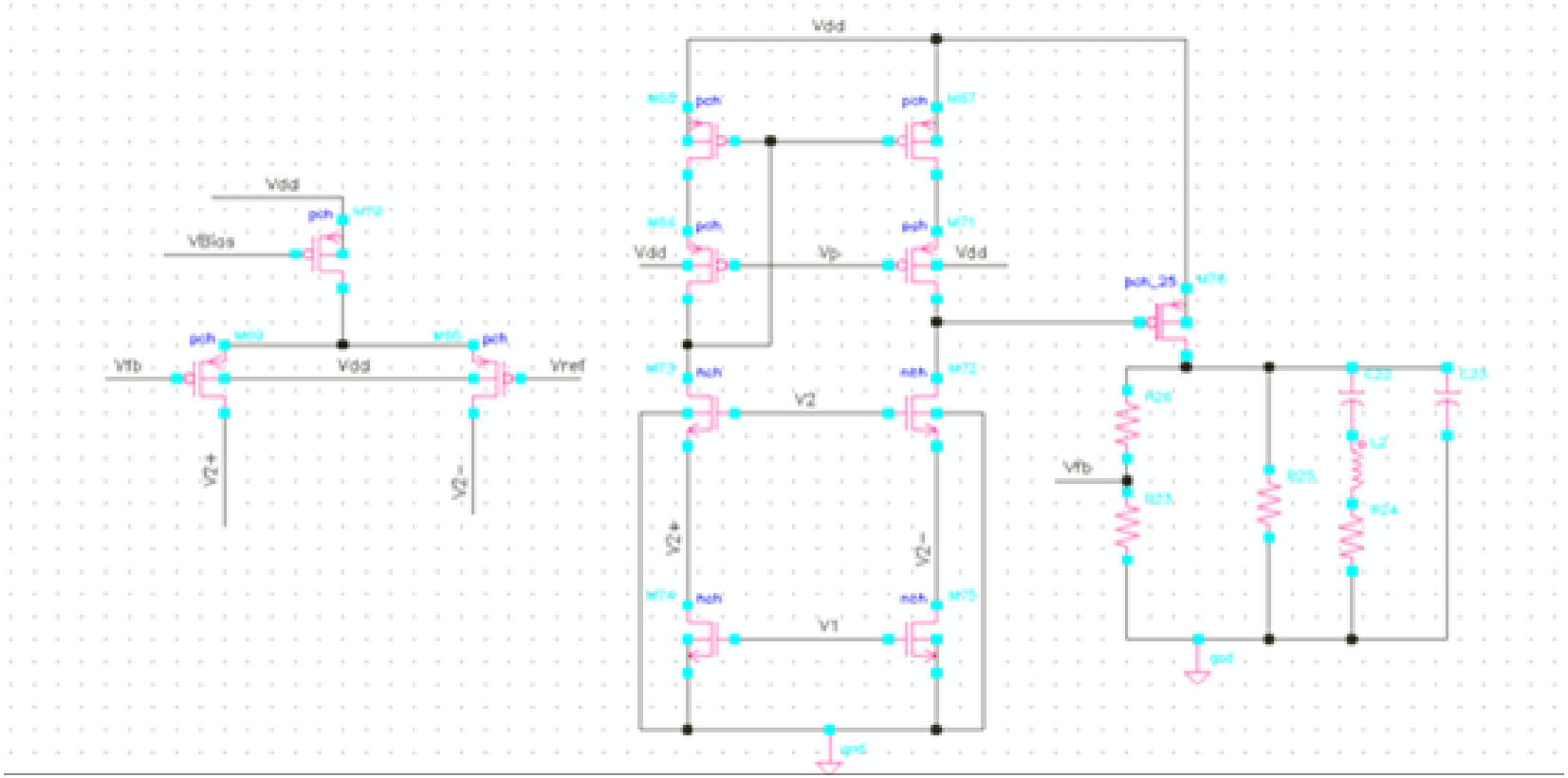
External Cap LDO

- Model for External Cap LDO



External Cap LDO continue

- Circuit Schematic



External Cap LDO continue

- Total gnd current =67u Integrated Cap =5p
- Efficiency = 38.7% Loop Gain=60dB
- Non integrated cap model as:

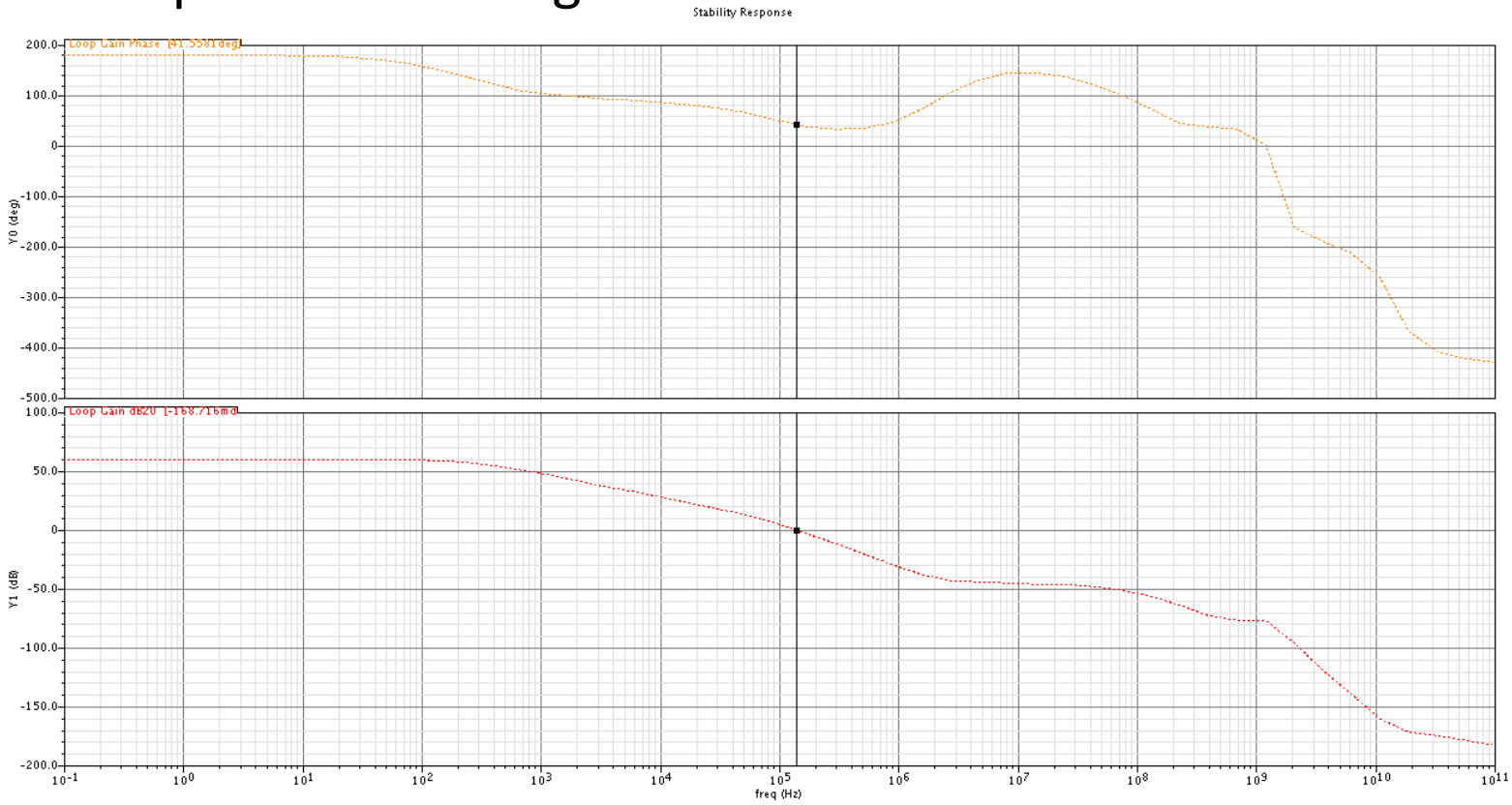
  C=4uF

  Resr=32m ohm

  Lesl=1.5nH

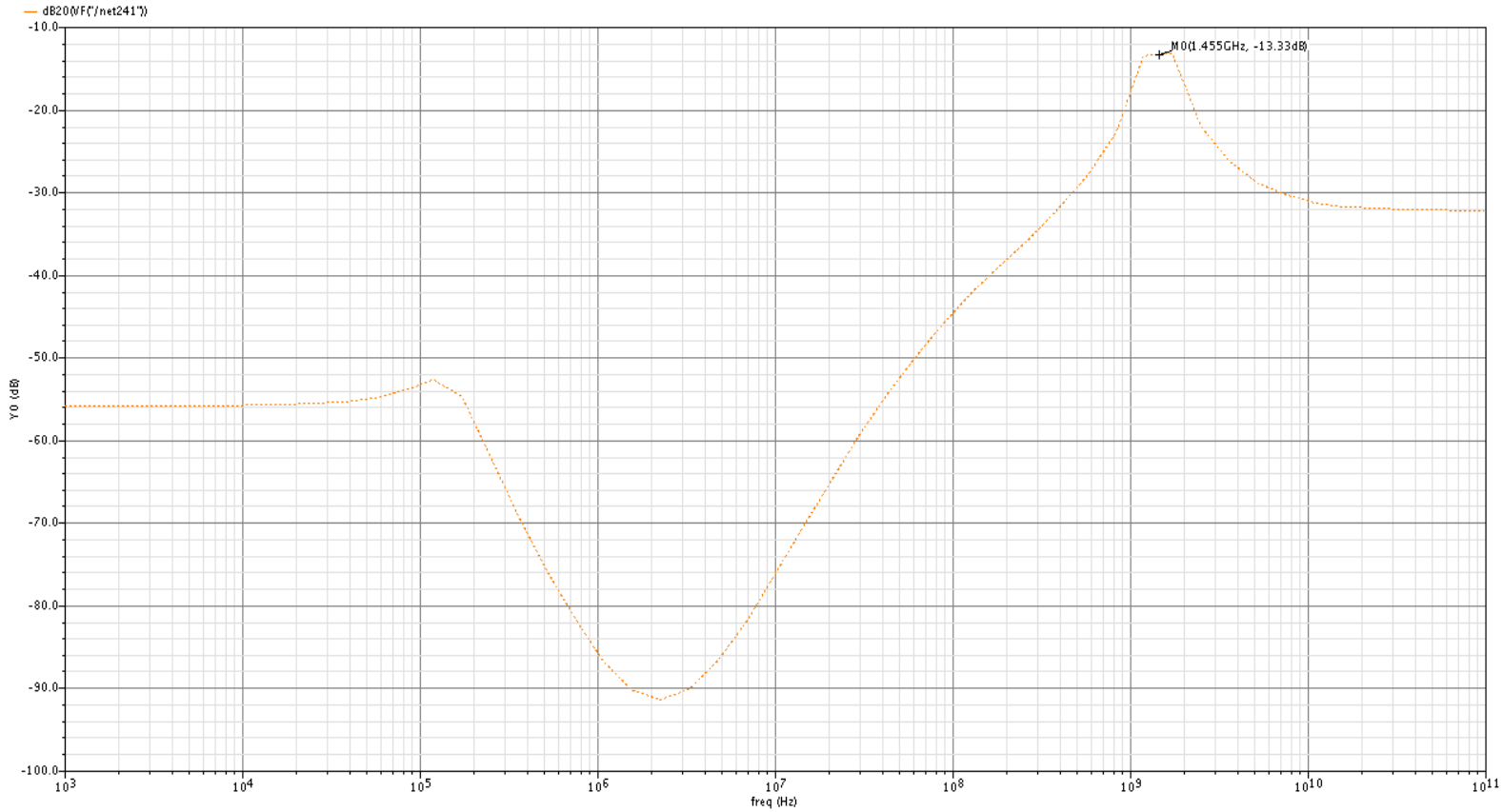
External Cap LDO continue

- Circuit Stability analyses under load condition
- Loop Phase =41 degree at 0dB



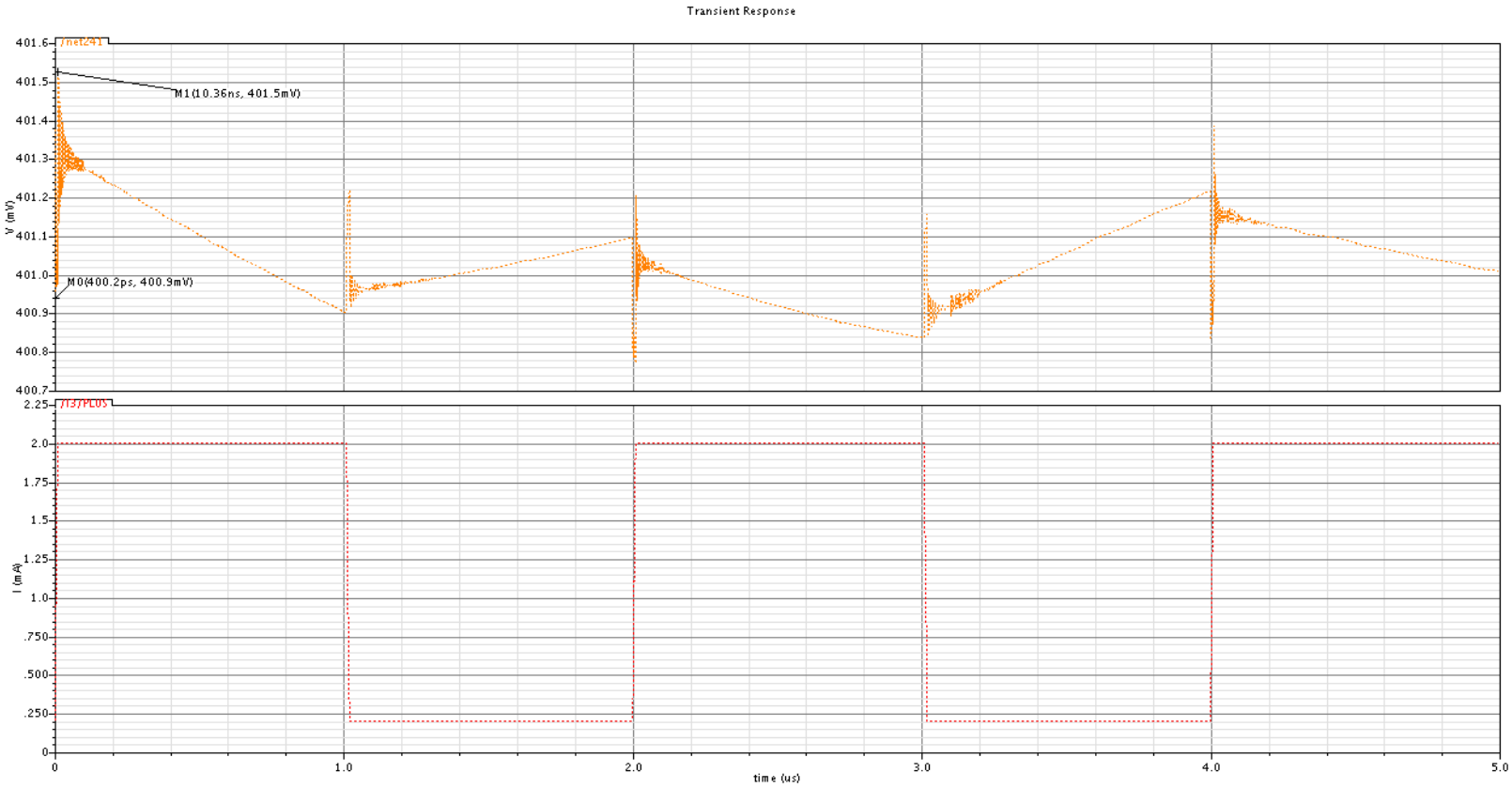
External Cap LDO continue

- Circuit PSRR
- Worst case PSRR=-13.33dB



External Cap LDO continue

- Transient simulation for I load=200u to I load_max=2m with 1u raise and fall time with Over shot =1.5mV

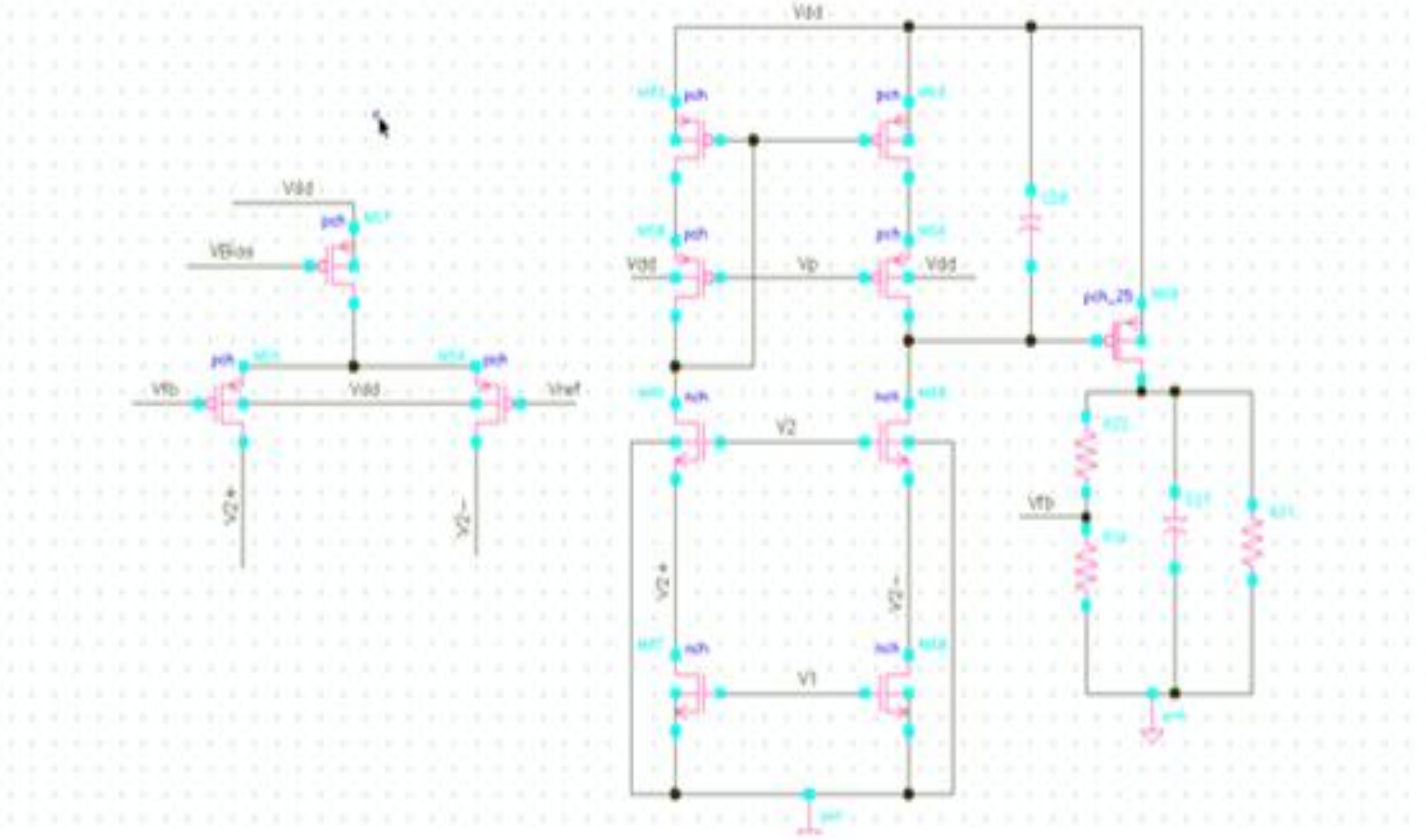


Cap Less LDO

- Circuit Schematic
- Total gnd current = 85u
- Loop Gain =60dB

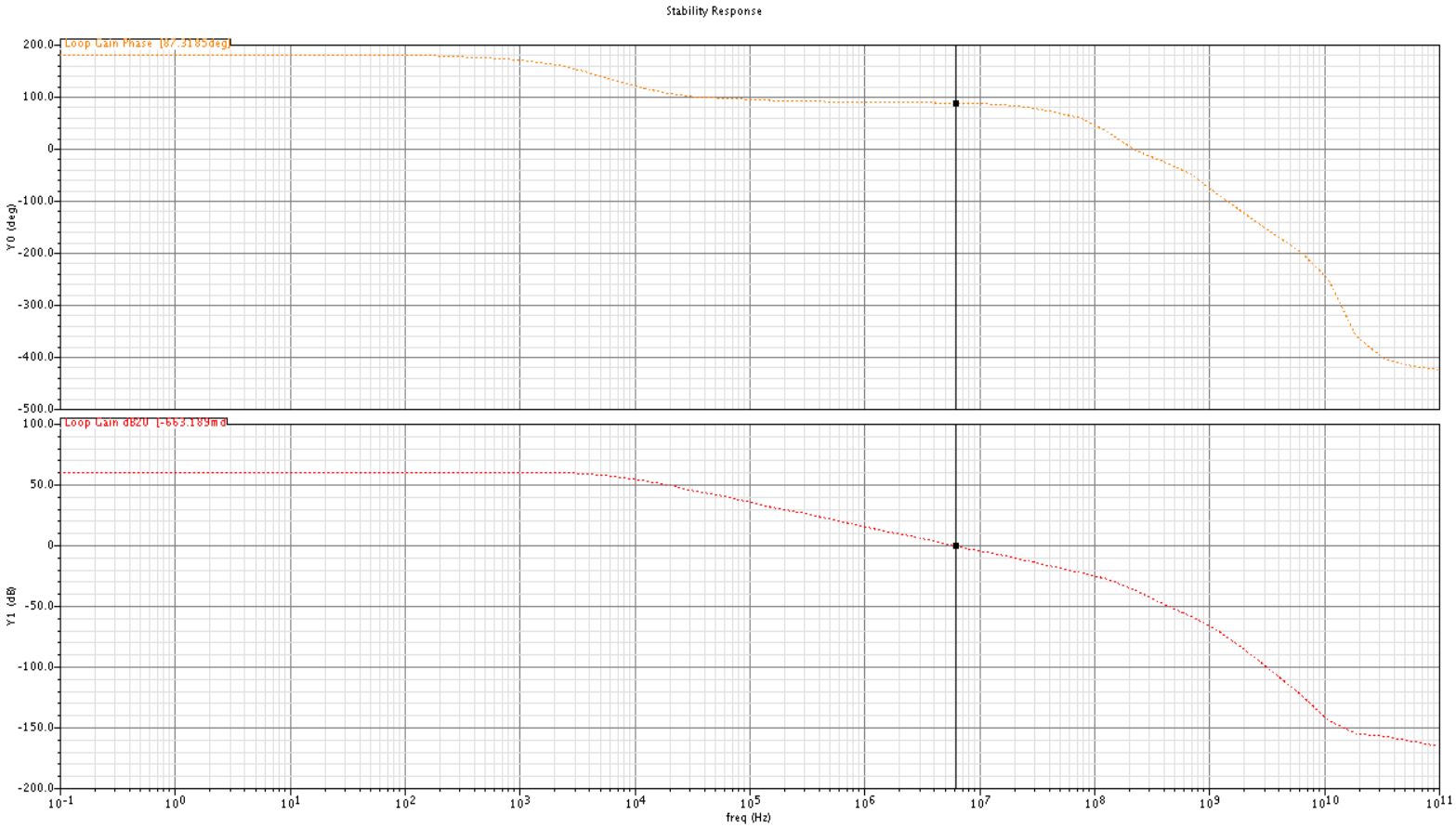
Integrated Cap = 8 pF

Efficiency=38.3%



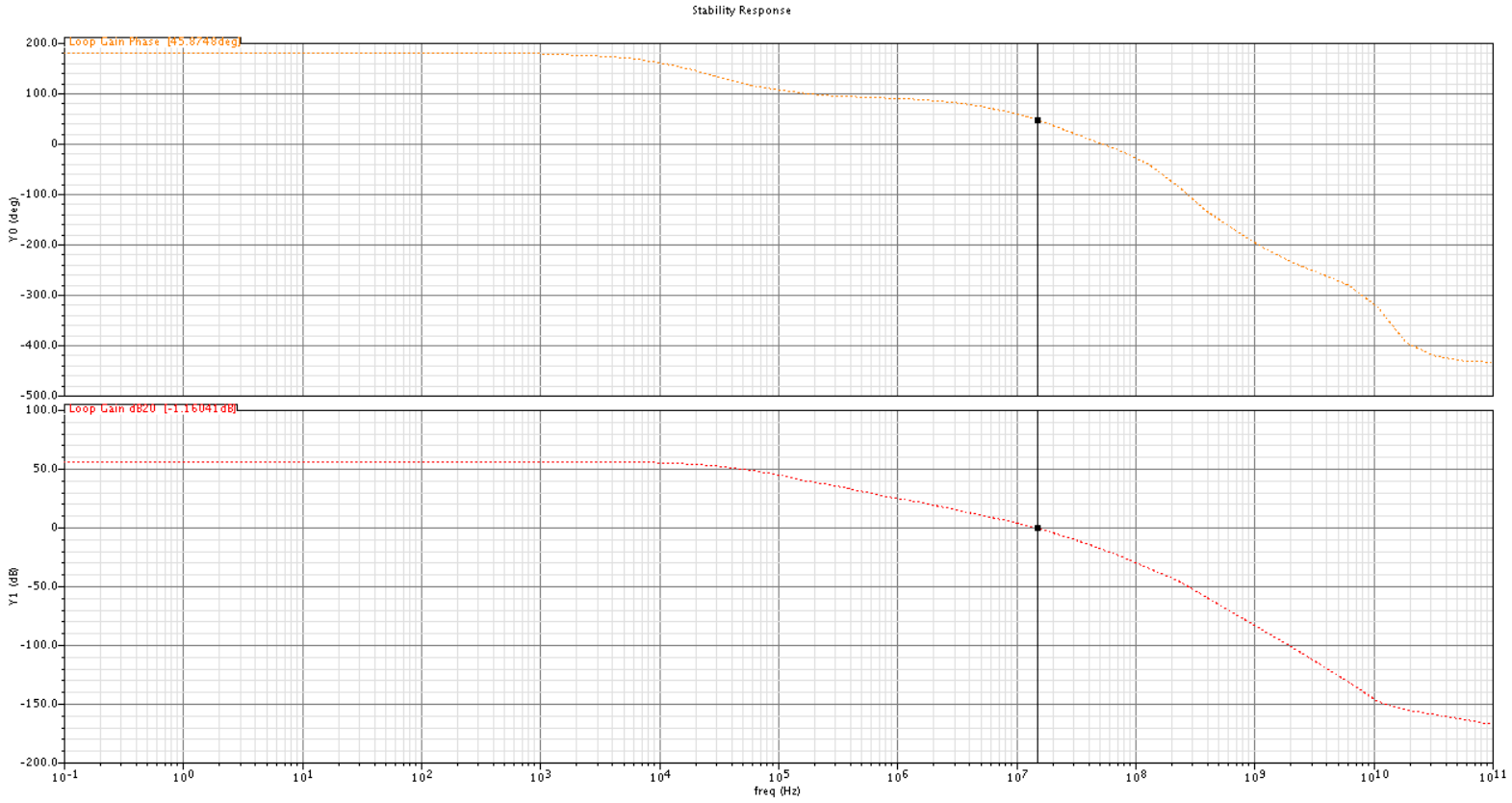
Cap Less LDO continue

- Circuit Stability analyses under load condition 2mA
- PM=87 degree



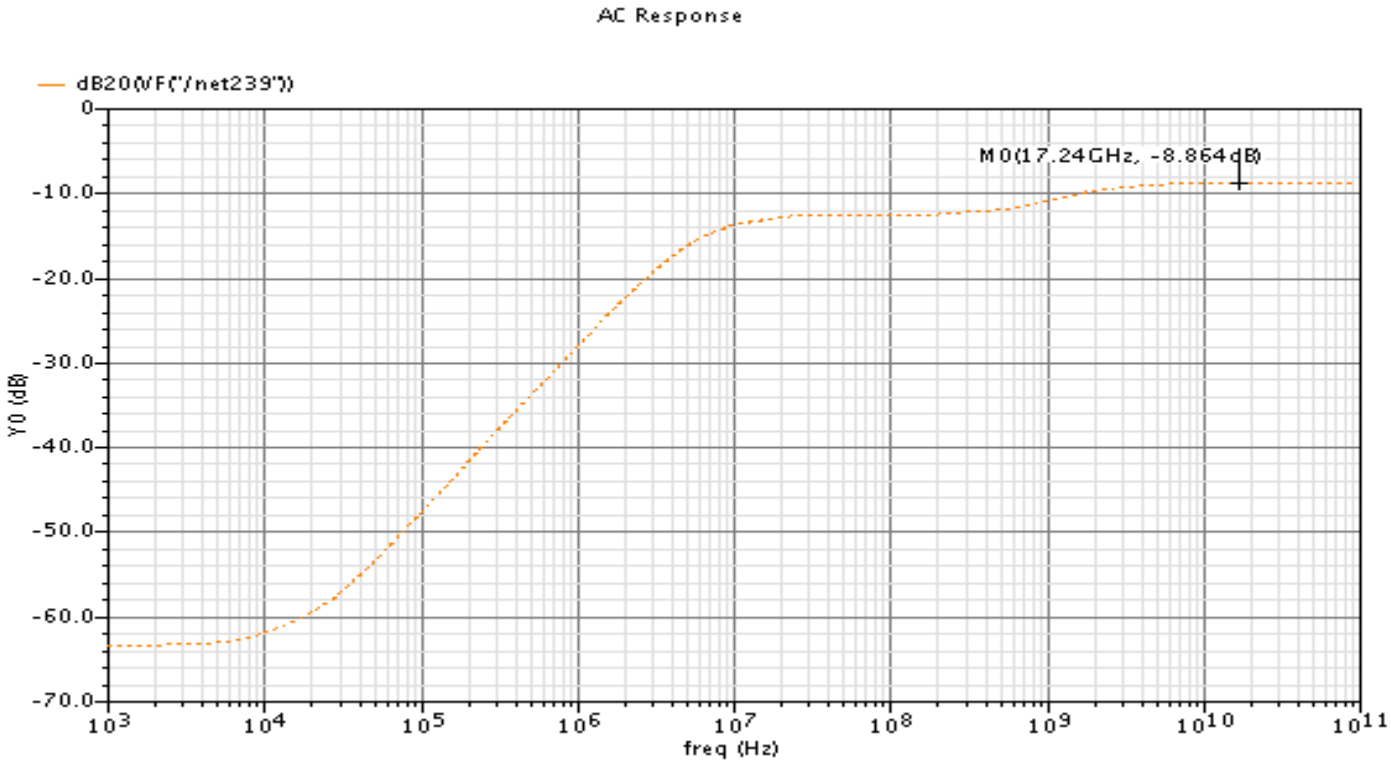
Cap Less LDO continue

- Circuit Stability analyses under no load condition
- PM=45 degree



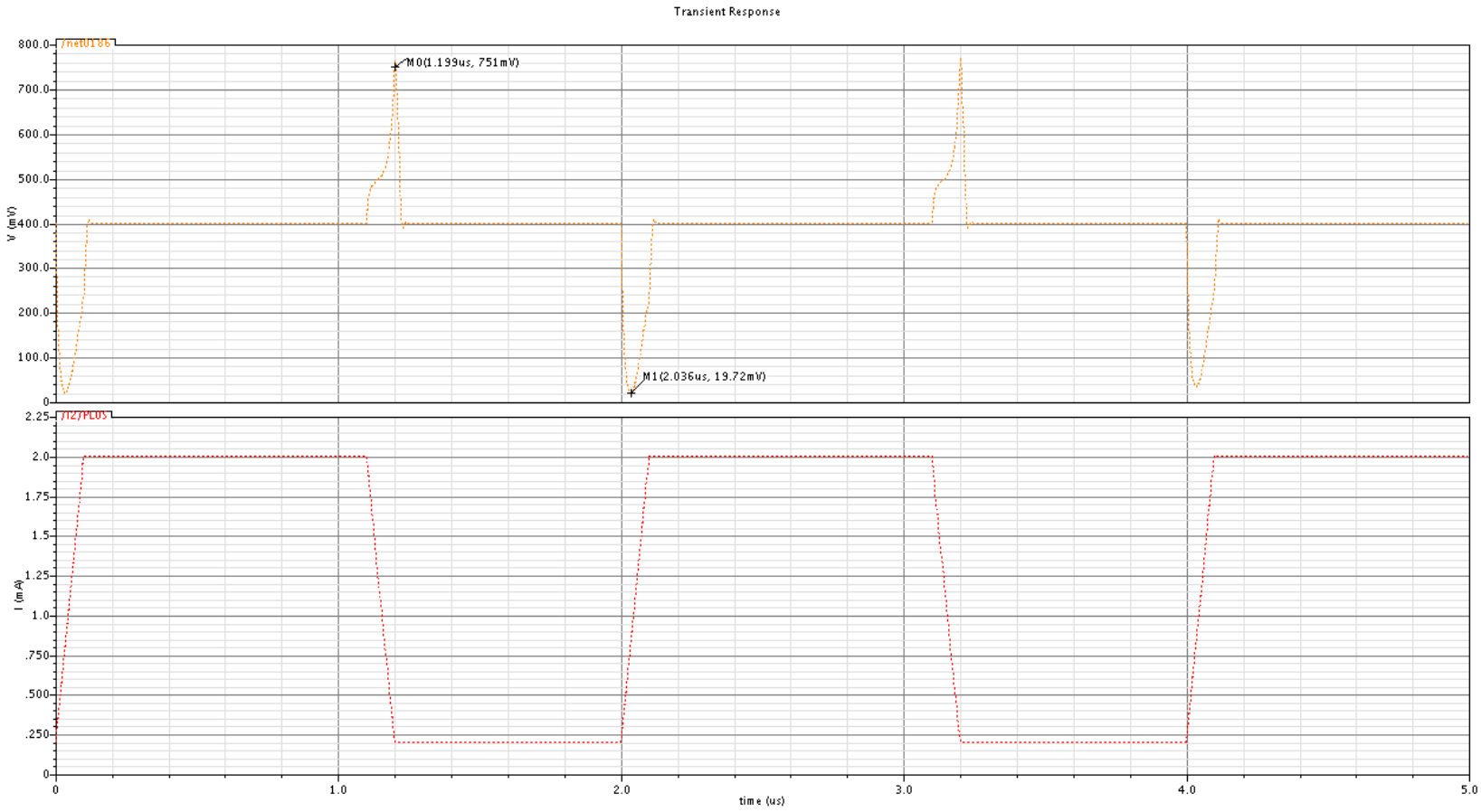
Cap Less LDO continue

- Circuit PSRR
- Worst case PSRR= -8.86dB



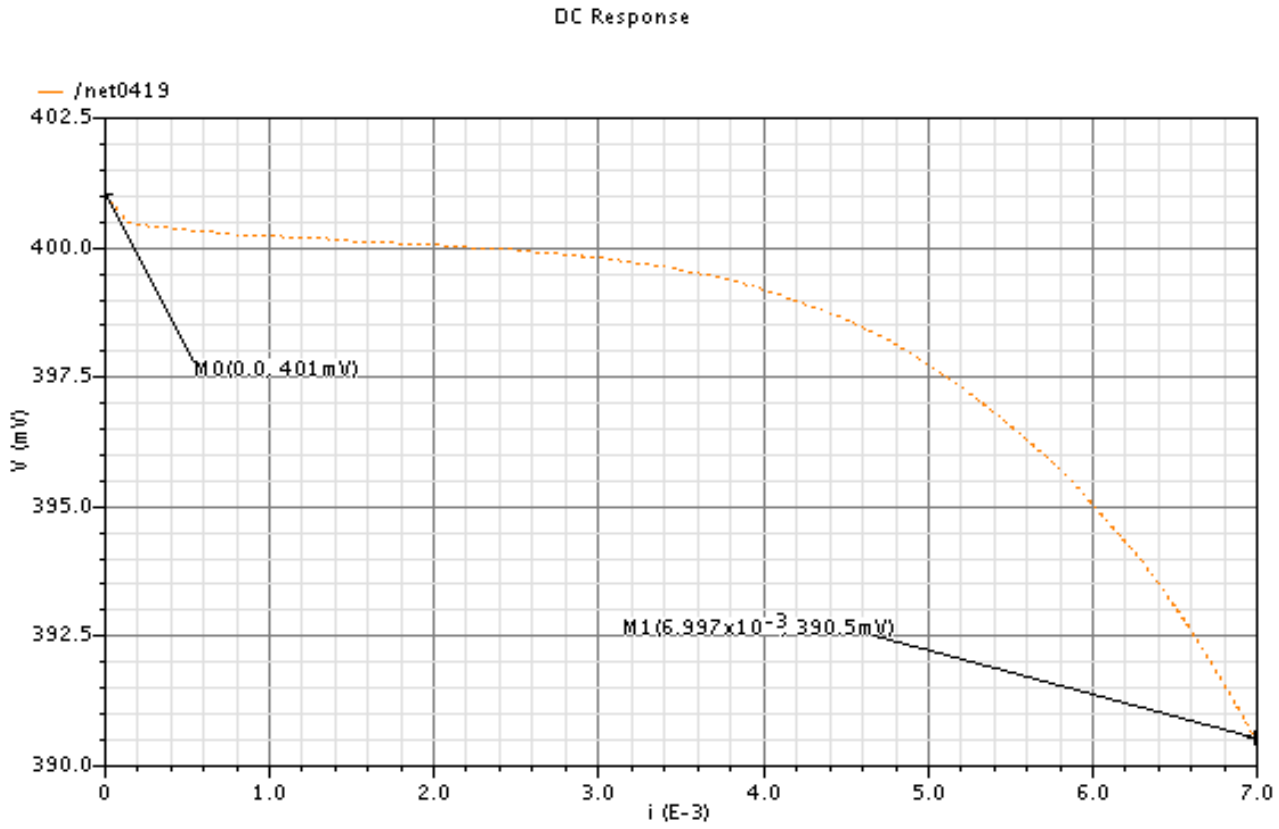
Cap Less LDO continue

- Transient simulation for I load=200u to I load_max=2m with 1u raise and fall time with Over and Under shot=350m



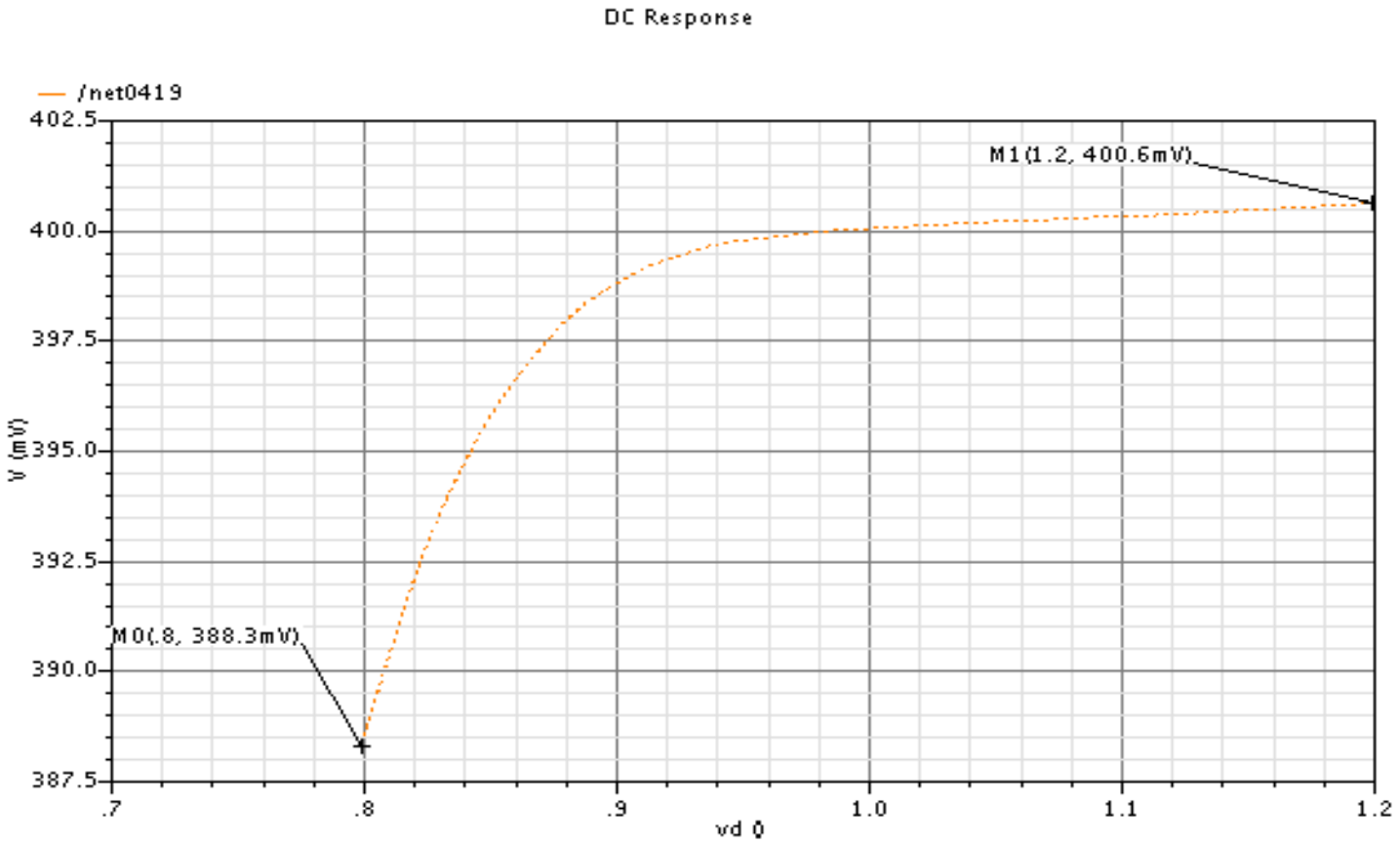
Cap Less LDO continue

- Load Regulation



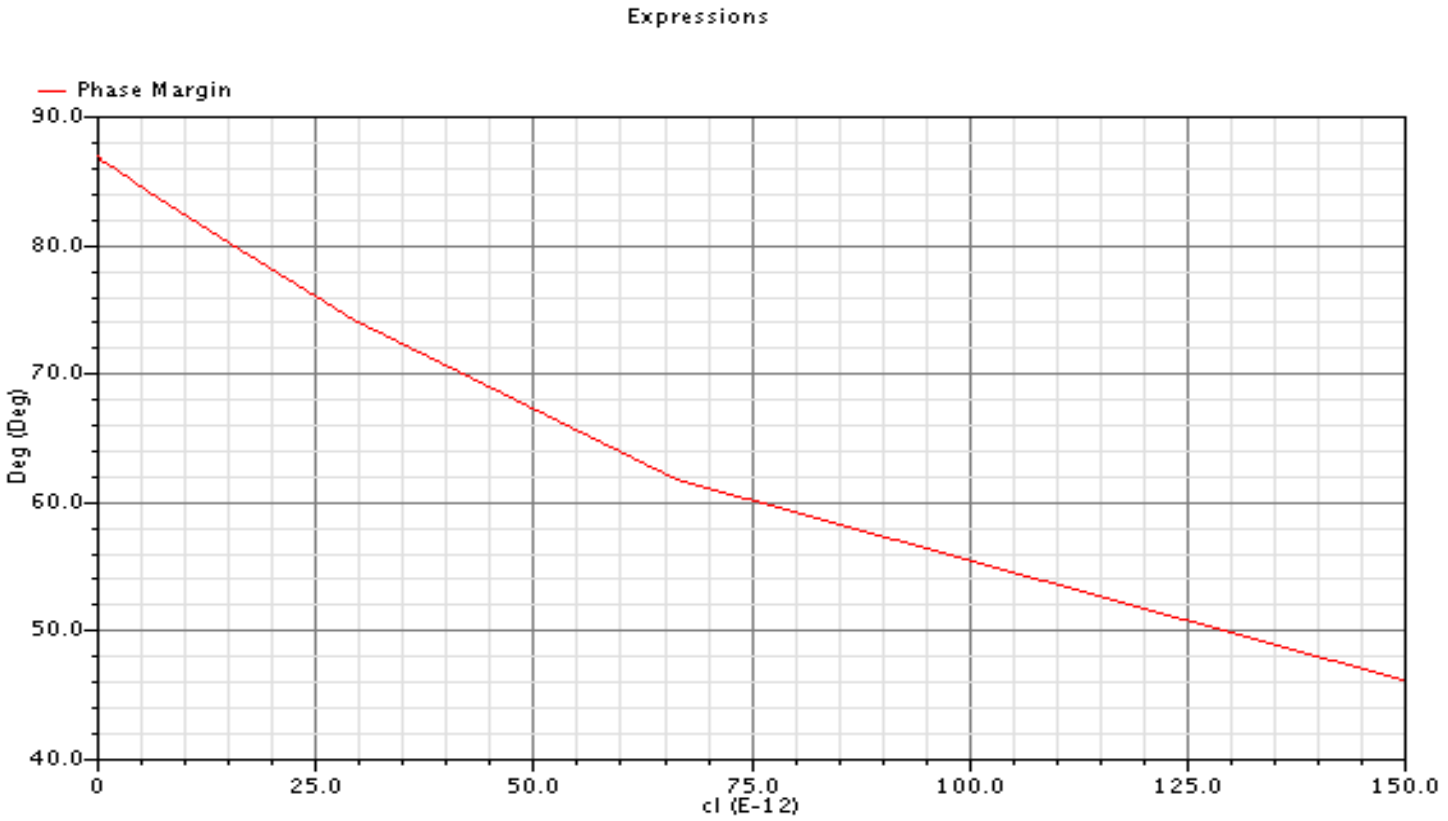
Cap Less LDO continue

- Line Regulation



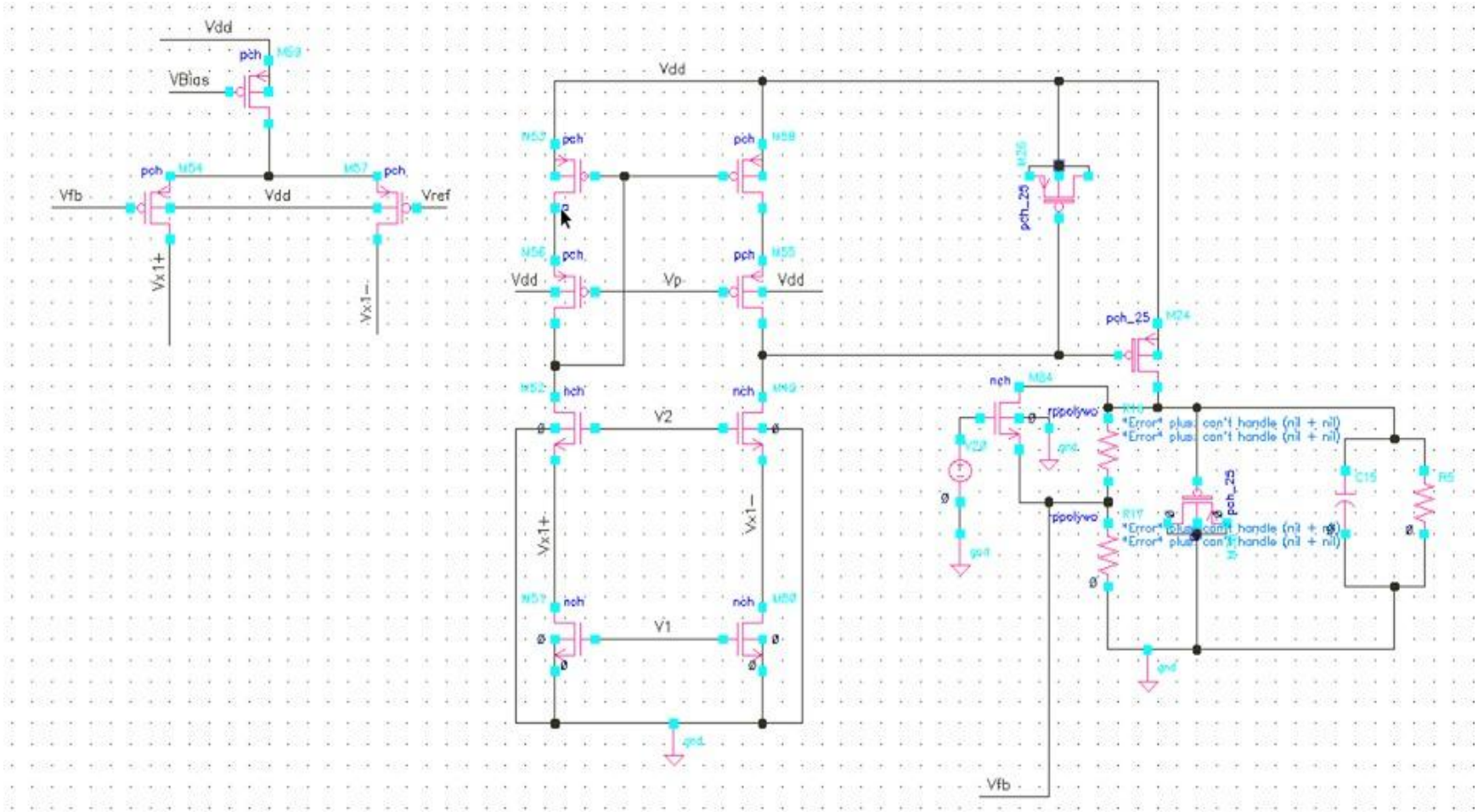
Cap Less LDO continue

- PM vs CLoad



Final Circuit

- Cap less LDO with programmable Output

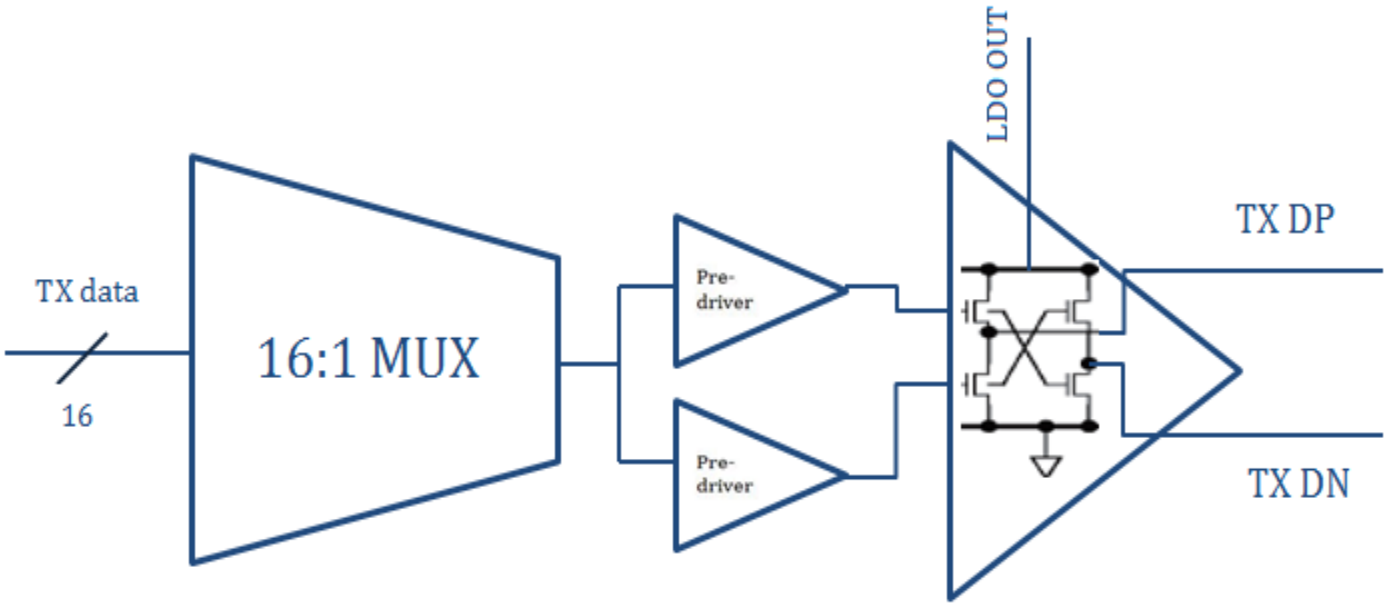


Conclusion

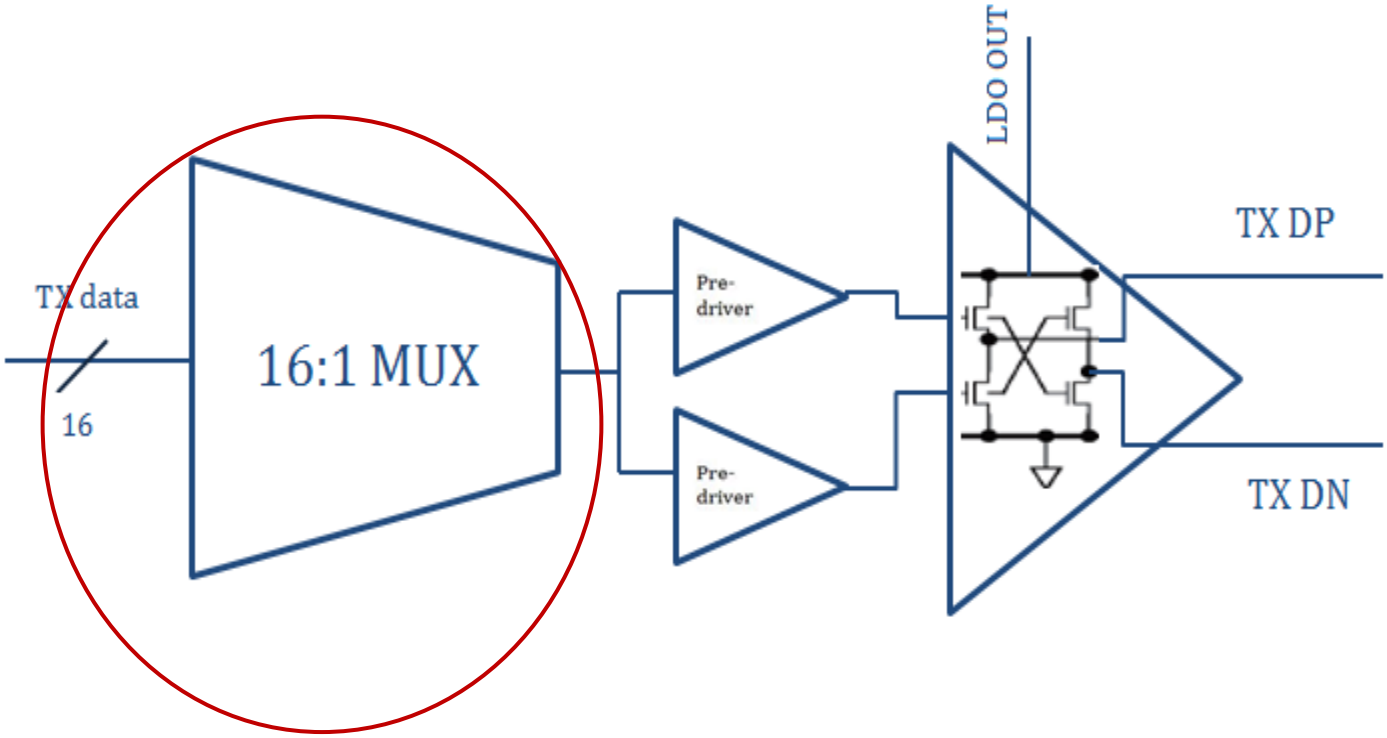
- External Cap gives Better results in all the parameters.

- Cap Less LDO would be sufficient for stable loads and give fair PSRR.

Transmitter



16:1 Serialializer

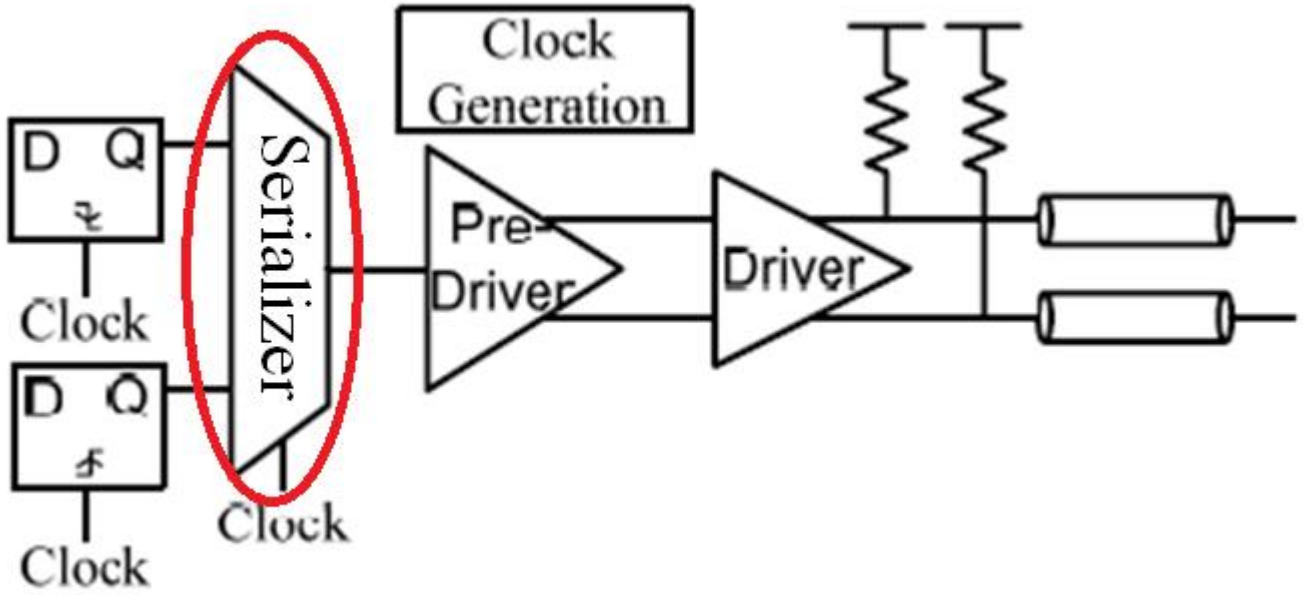


Presented by : Mohamed M.Shafey

Outlines

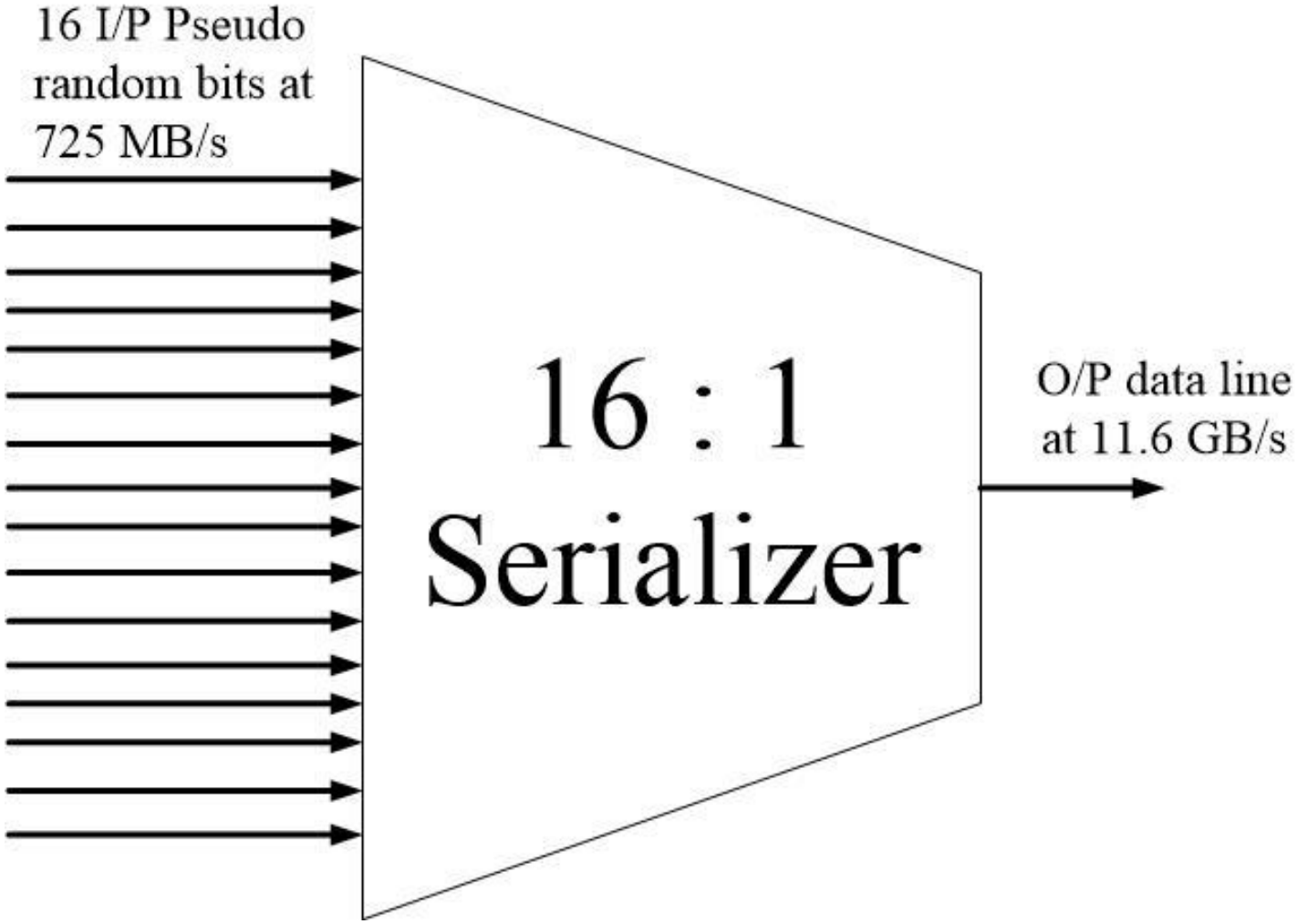
- Introduction
- Architecture
- Topology
- Design and Schematic
- Simulation Results
- Layout

Introduction



Serializer is serializing parallel input data to a serial output data line.

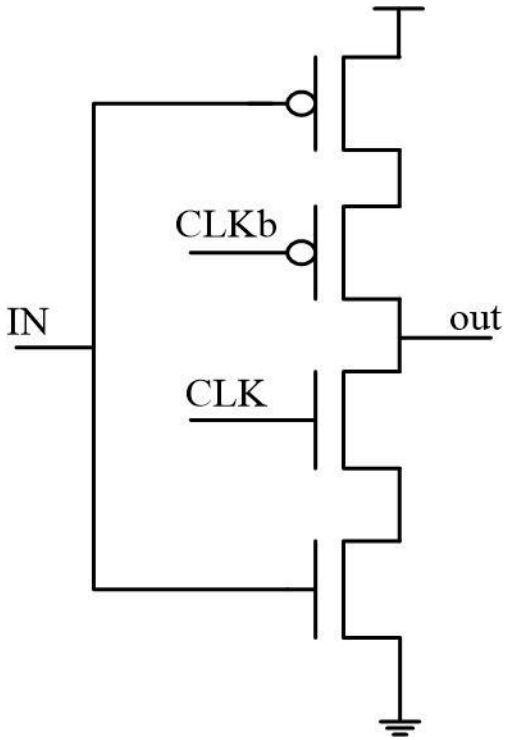
Architecture



Topology

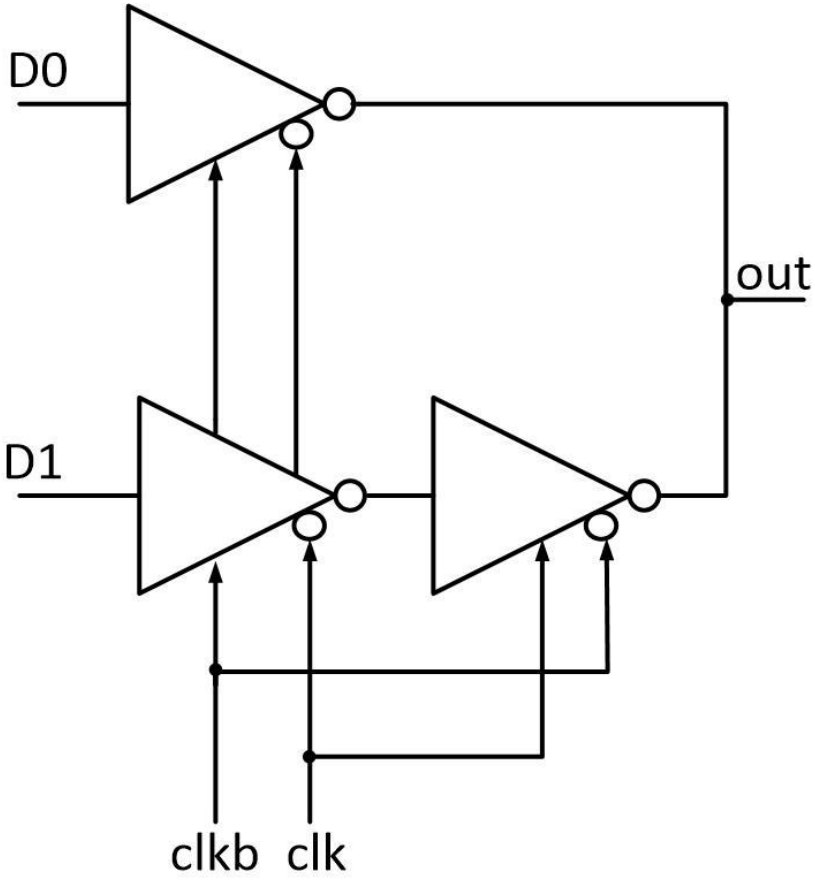
Clocked Inverter ($C^2\ MOS$) :

- Inverter that control it's output by a clock
- If CLK = 1 , Inverter pass the input to output
- If CLK = 0 , It holds the data as a latch (high impedance)
- **Clocked inverter is a latch**



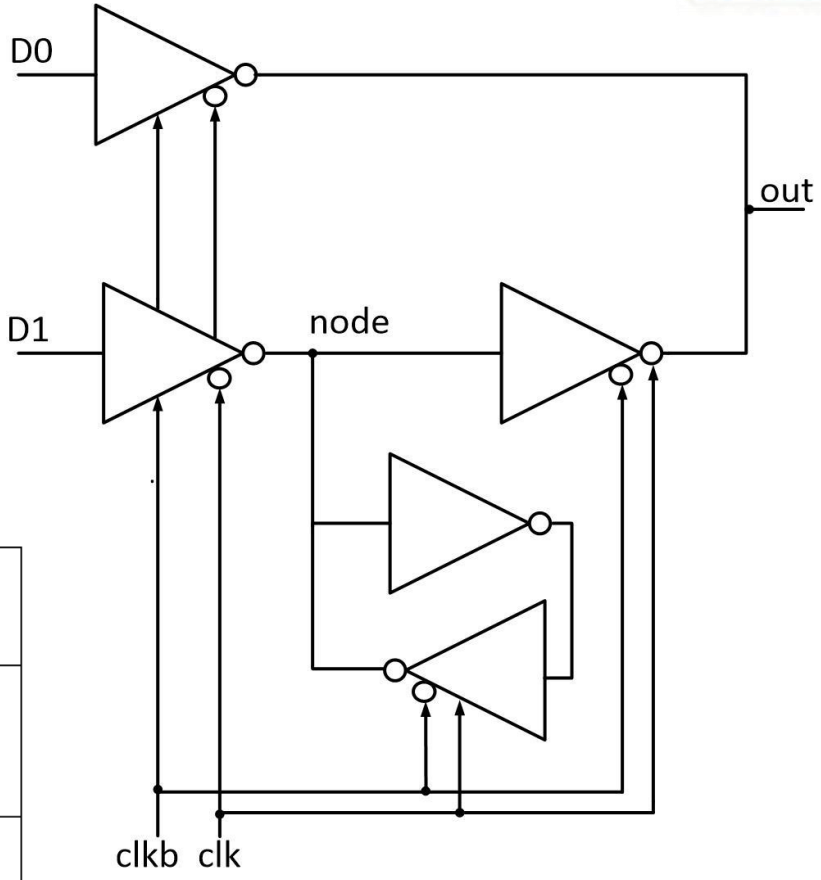
Design and Schematic

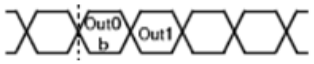
- 2:1 multiplexer
- Using 3 clocked inverters we can perform the operation of retiming and selection at the same time
- less power consumption ☺
- Decrease Switching components ☺
- Node Floating ☹



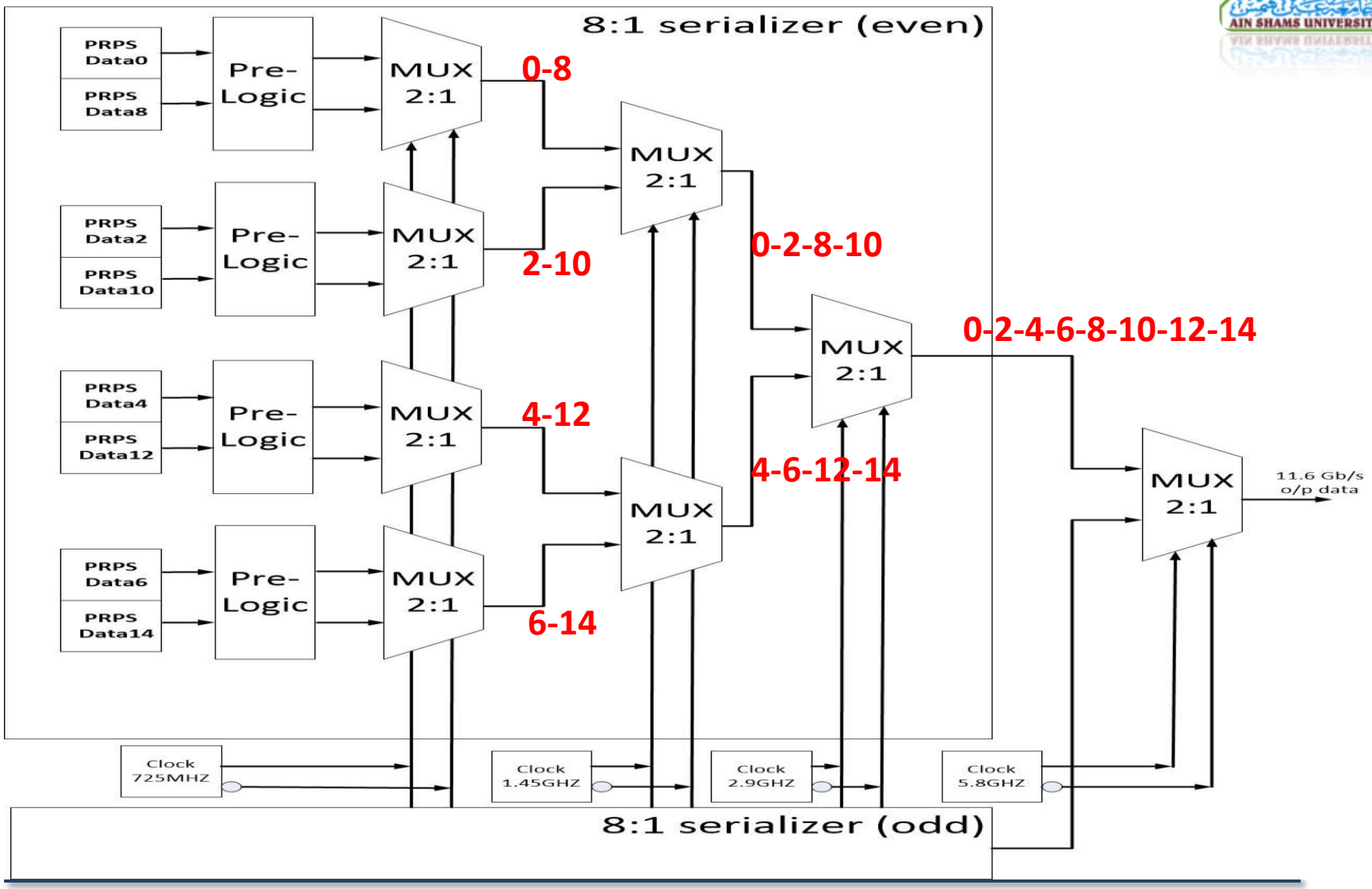
Design and Schematic (Cont.)

- Solving high impedance node (floating)
- Inter state latch
- To hold input level of 2nd inverter

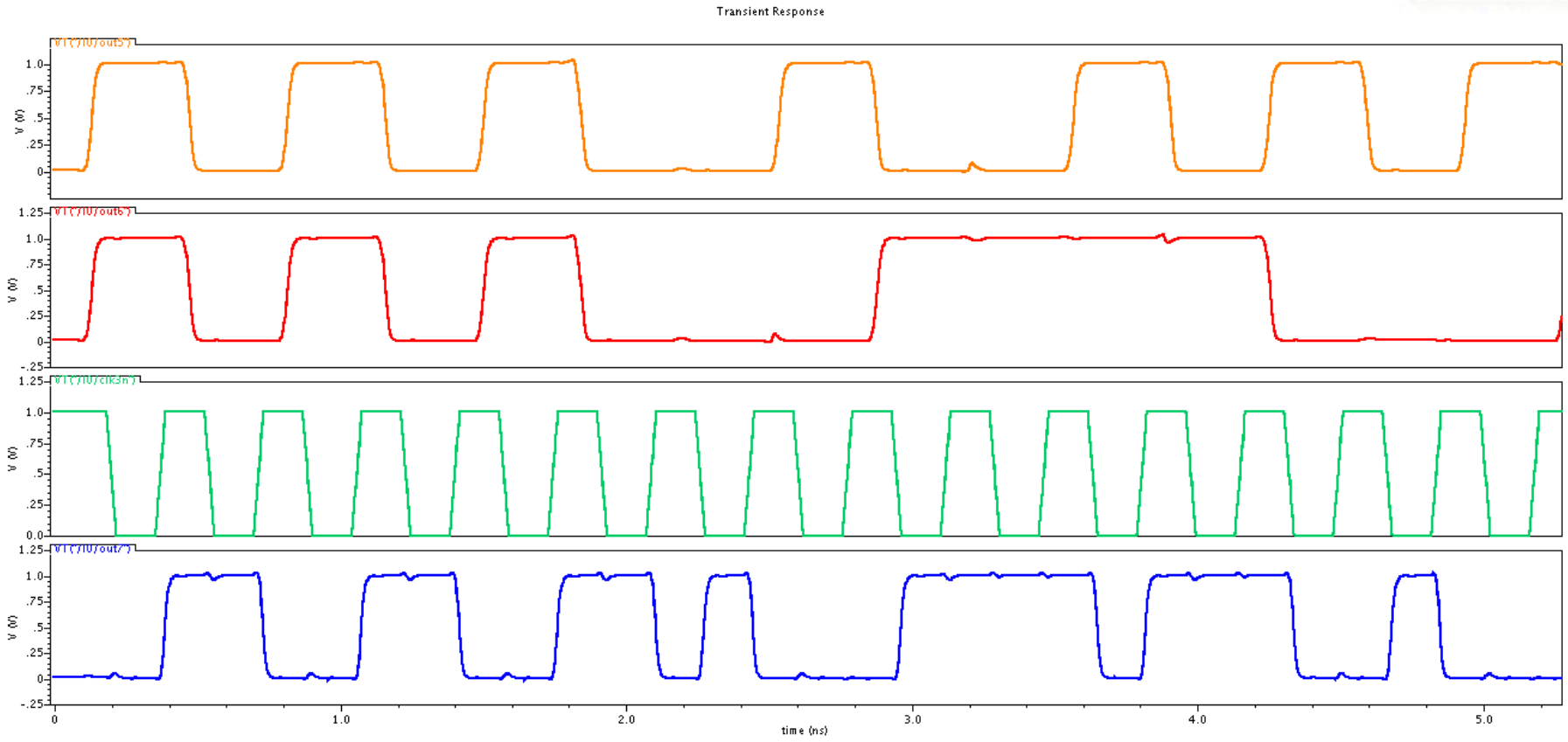


Input data	
clkb	
output	

Design and Schematic (Cont.)

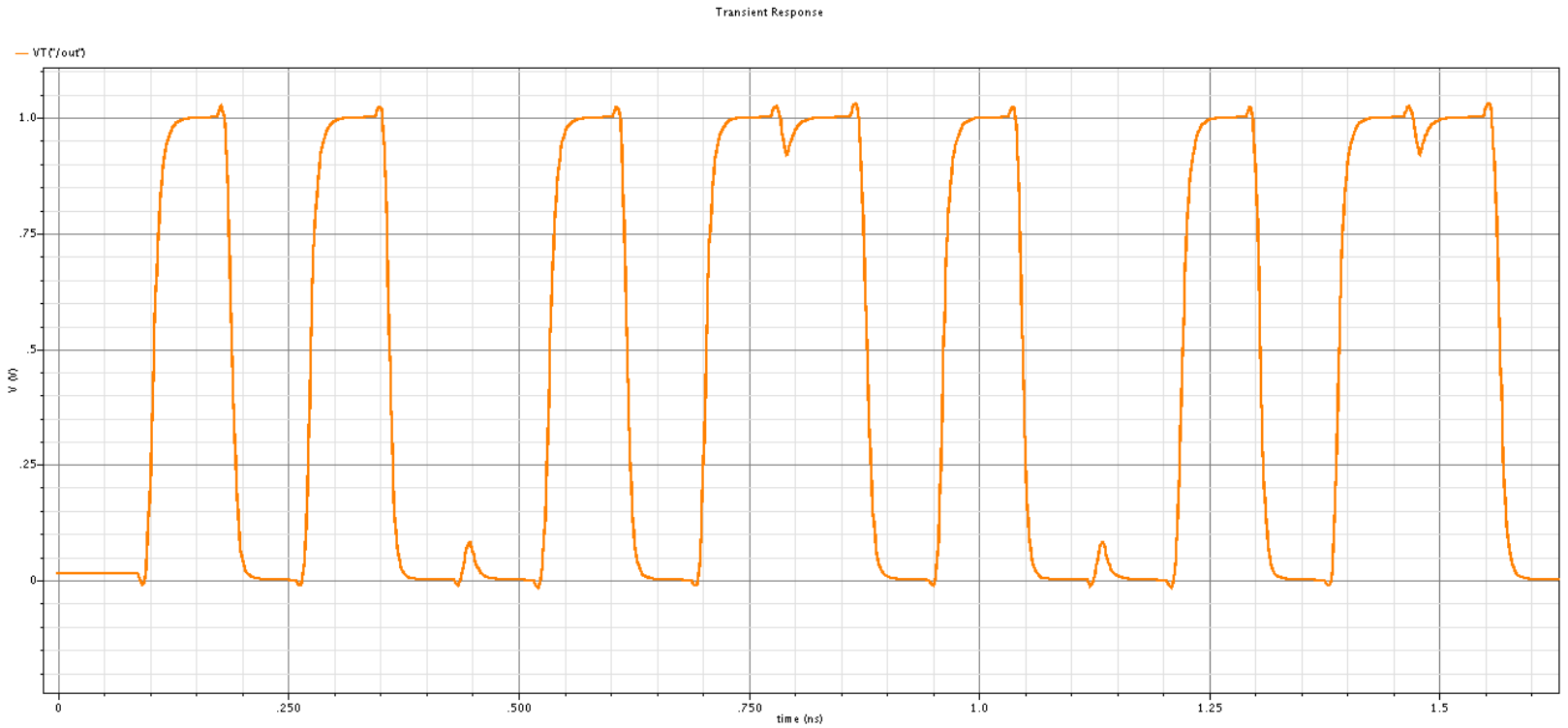


Simulation Results



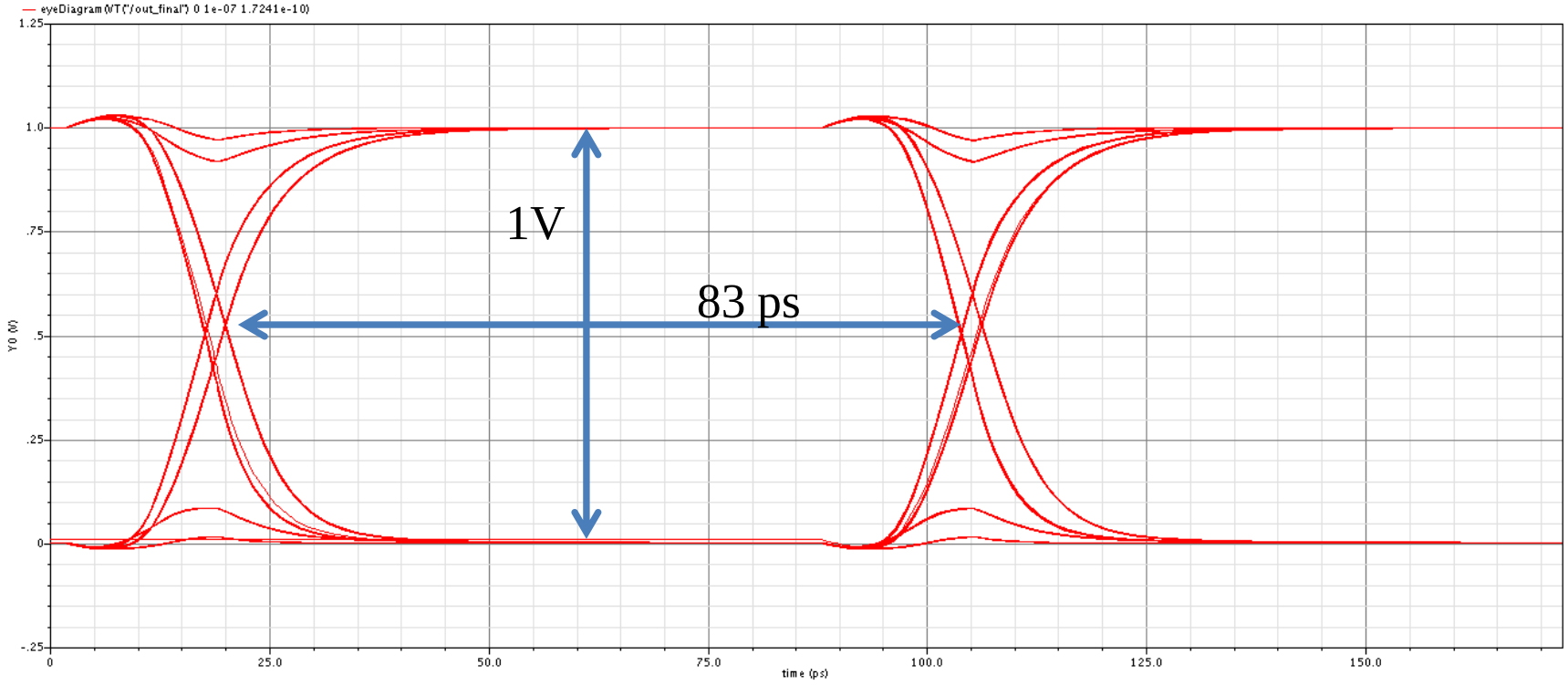
2 I/P data , CLKb , multiplexed O/P

Simulation Results (cont.)



Final Output waveform 11.6 GB/s

Simulation Results (cont.)

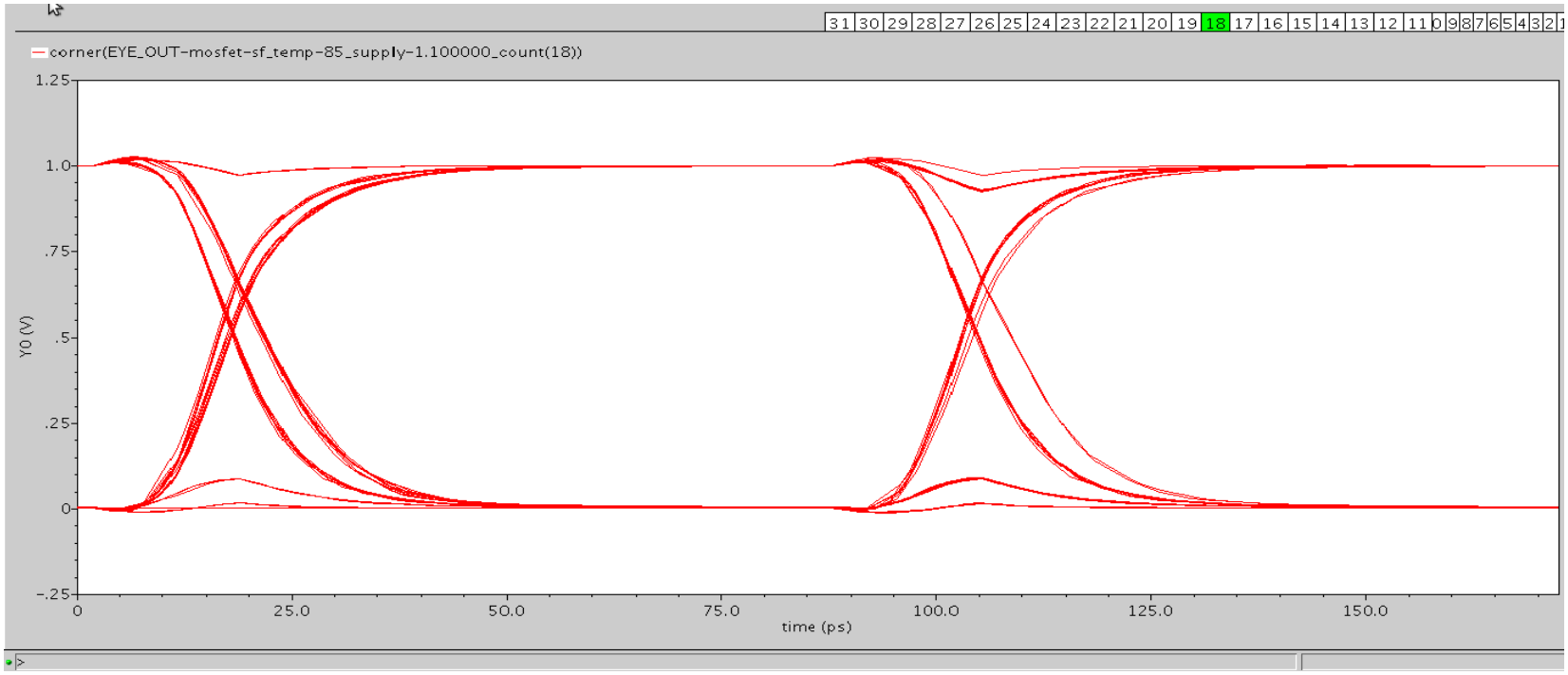


Final Eyediagram

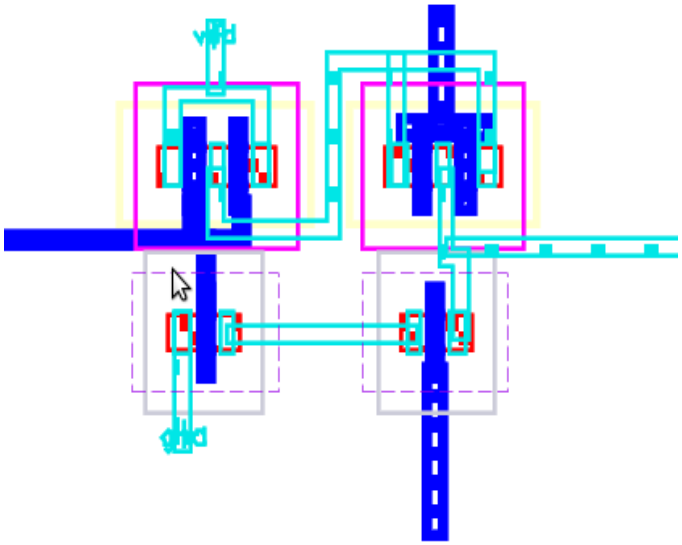
Simulation Results (cont.)

Corners Results :

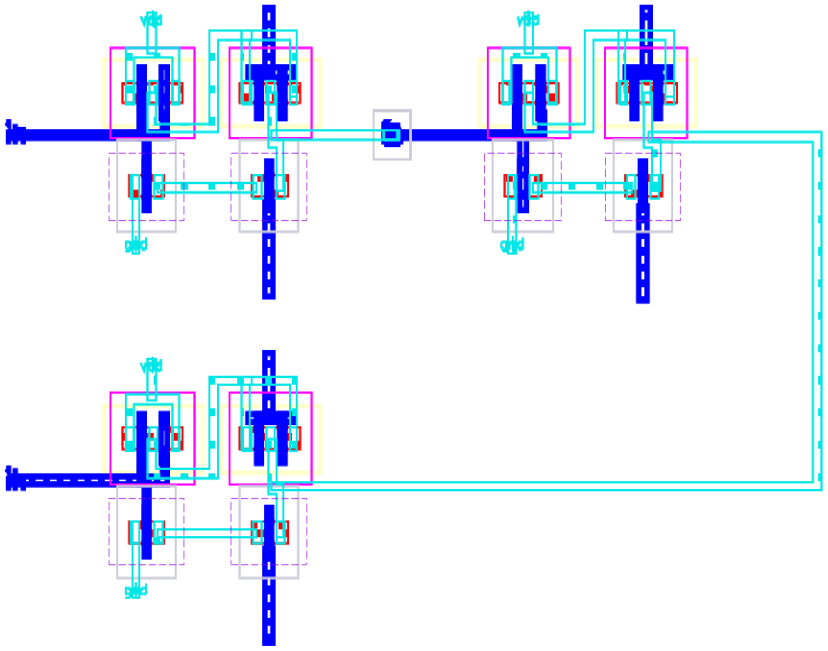
Worst case corner was at SF where eye opening is 82ps



Layout



- Clocked inverter



- 2:1 MUX

Pre-driver

Presented by : Samar Hussein

Outlines

- Why do we use a pre-driver?
- Power and delay problems in a pre-driver.
- Topologies of pre-driver buffers.
- Hand Analysis.
- Final design circuit and simulation outputs and Specs.

Why do we use a pre-driver?

- A pre-driver is used between the driver and the multiplexer in the transmitter to drive the large capacitance of the driver without loading on the small capacitance of the multiplexer.

- a pre-driver acts as a buffering stage so it is implemented using a buffer series.

Power problem in a pre-driver.

- A pre-driver face a problem with its large power consumption.

- Since a pre-driver is built up from a series of buffers ”inverters” then it sinks a large current and is called “ power hungry”.

- This large current is a short circuit current occurring when both transistors of an inverter are on at same instant.

- this problem can be solved by limiting the number of buffers used.

Delay problem in a pre-driver.

- Buffers used in a pre-driver may introduce a delay which can cause its following stages not to work functionally.

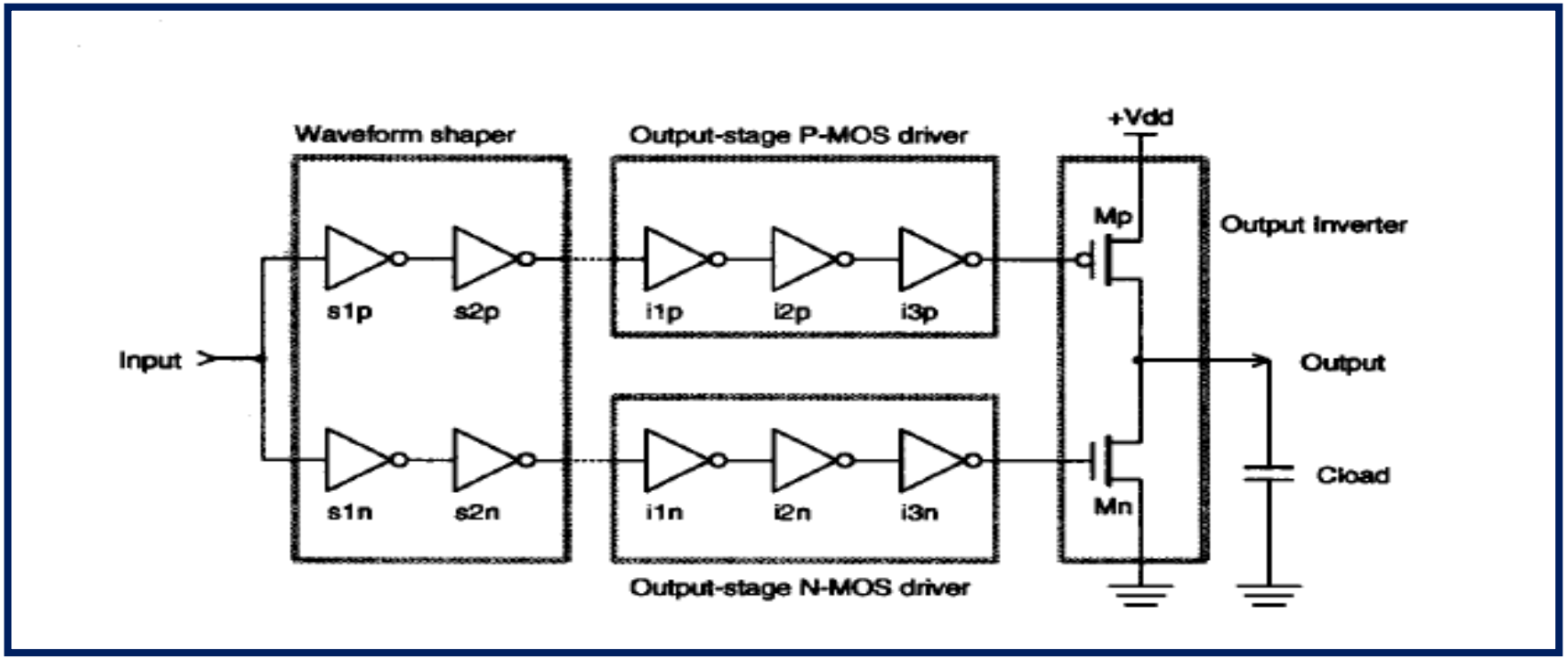
- This delay can be minimized to an optimum value through a proper sizing of the inverters used in the buffering stages.

- F04 “fan out of 4” can be used to solve the delay problem in an optimum way.

Topologies of a pre-driver.

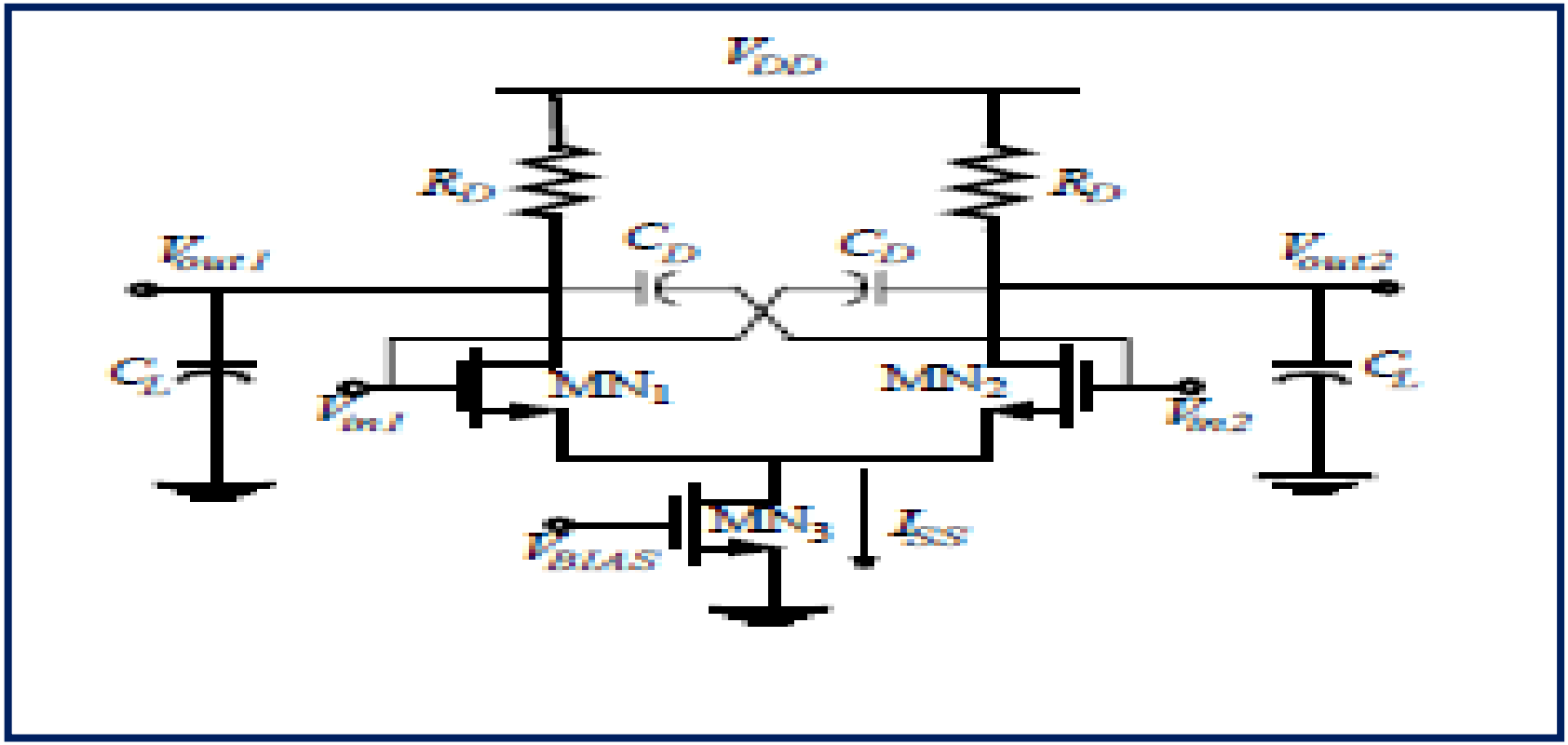
- Low power CMOS buffers
- CML buffers
- Tapered CMOS buffers

Low power CMOS buffers.



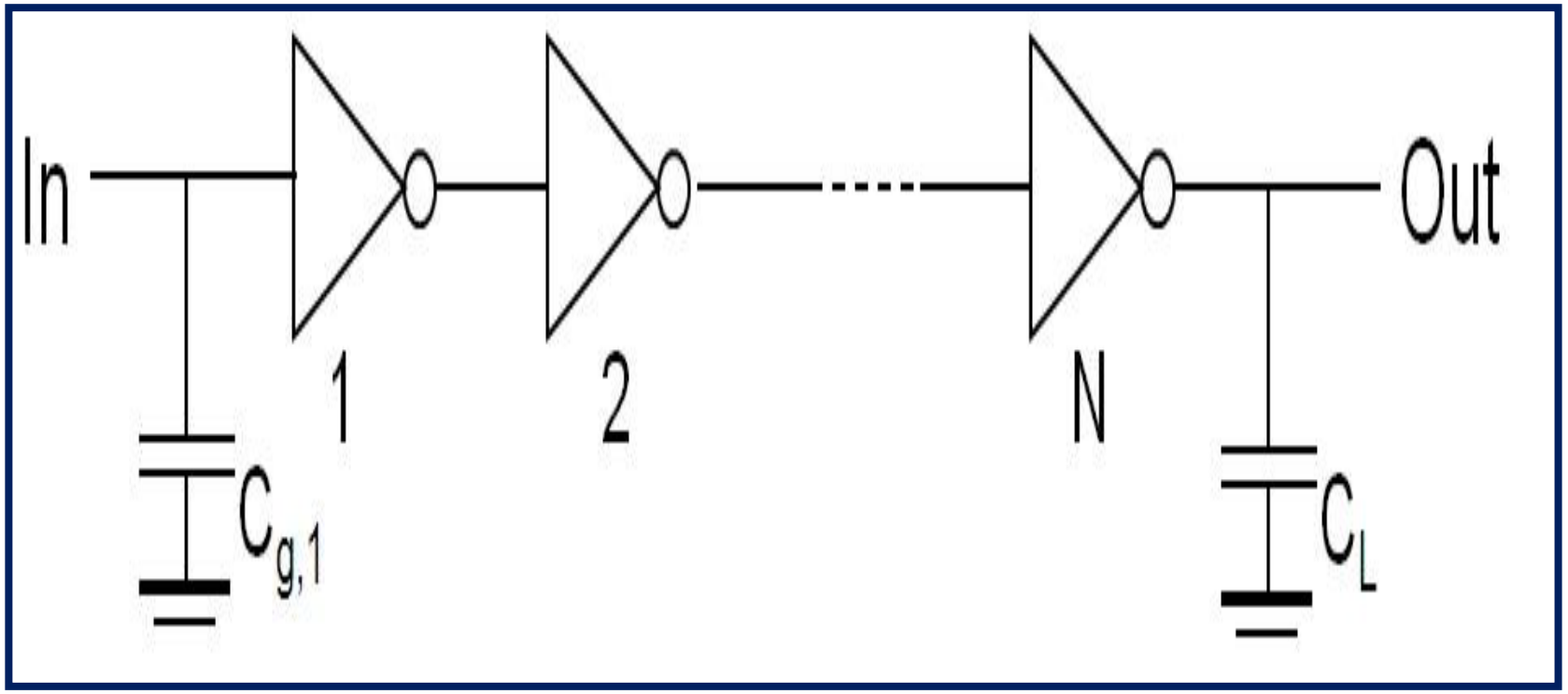
[Kei-Yong Khoo ; Integrated Circuits & Syst. Lab., California Univ., Los Angeles, CA, USA ; Wilson, A.N., Jr.]

CML buffers.



Payam Heydari, Ravi Mohavavelu ,
Department of Electrical and Computer Engineering ,University of California ,Irvine, CA 92697-2625

Tapered CMOS buffers.

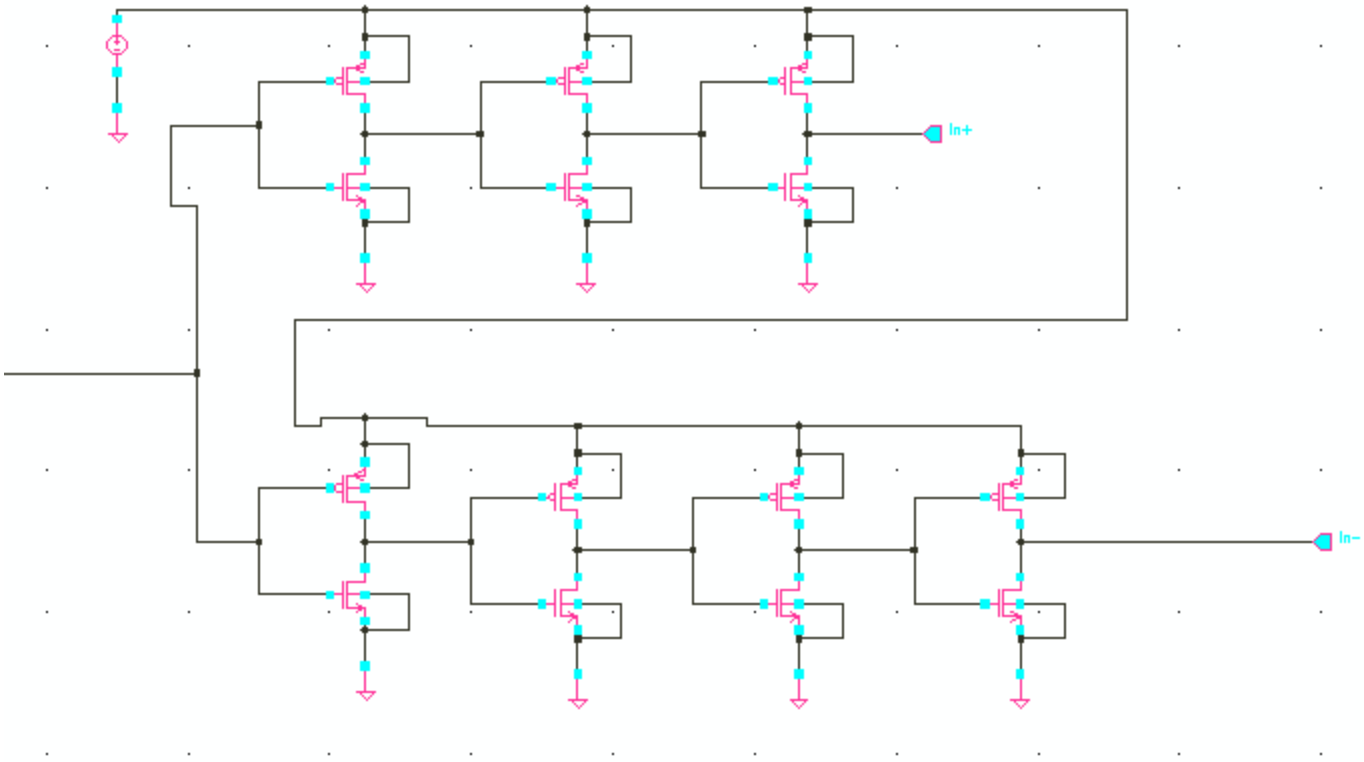


[Integrated Circuits ECE481 Lecture 6 Inverter Chain Delay ,Mohamed Dessouky ,*Integrated Circuits Laboratory ,Ain Shams University ,Cairo, Egypt]*

Hand Analysis.

- F = Cl/Cin
- Cl = 17fF, Cin = 0.5047fF.
- Fopt = $\sqrt[N]{F}$
- N = $\frac{log(F)}{log(fopt)}$
- Where F = 33.683 , fopt = 4.
- Then we get Nopt = 3stages

Final design circuit.

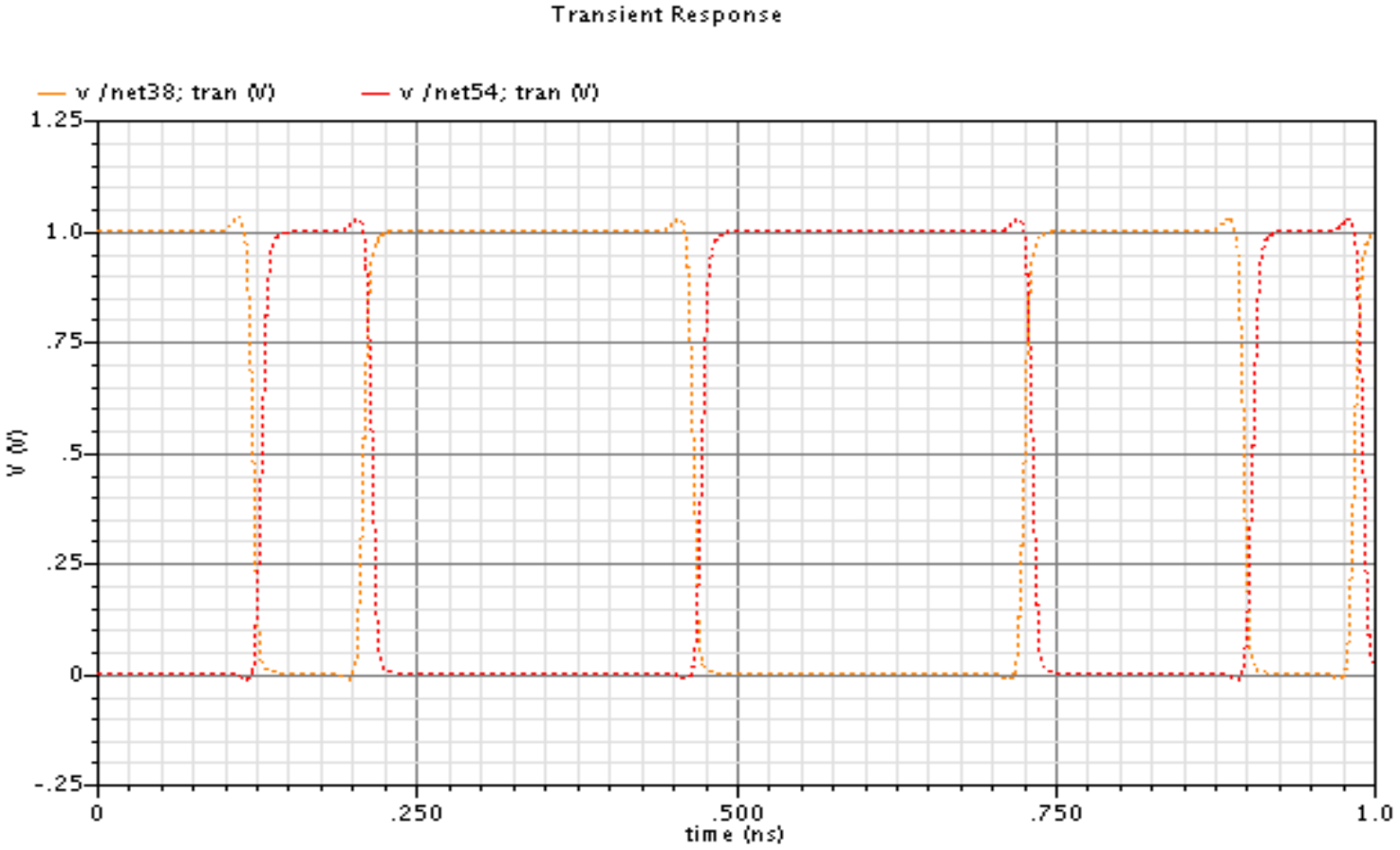


Simulation Outputs.

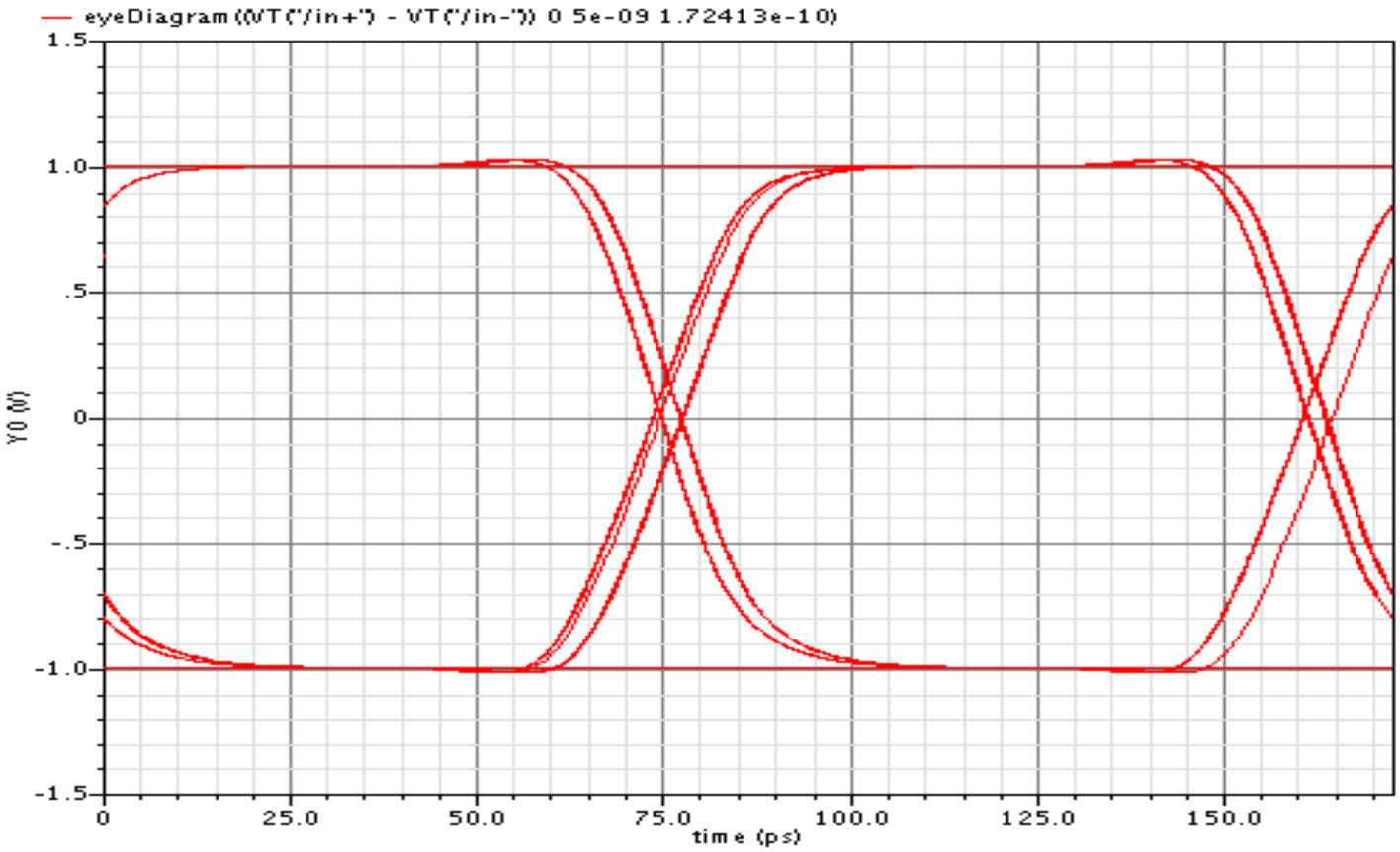
- Input Waveform
- Output Waveform
- Eye Diagram

Input waveform.

Output waveform.



Eye Diagram.


eyeDiagram((VT("/in+") - VT("/in-")) 0 5e-09 1.72413e-10)
1.5
1.0
.5
0
-.5
-1.0
-1.5
Y0 (V)
0
25.0
50.0
75.0
100.0
125.0
150.0
time (ps)

Pre-driver Specifications.

Supply Voltage	1 V
Supply Current	0.4 mA
Power	0.4 mW

CML to CMOS Stage

Presented by : Samar Hussein

Outlines

- Why do we need a CML to CMOS converter?
- Stages used in a CML to CMOS converter.
- Simulation results.

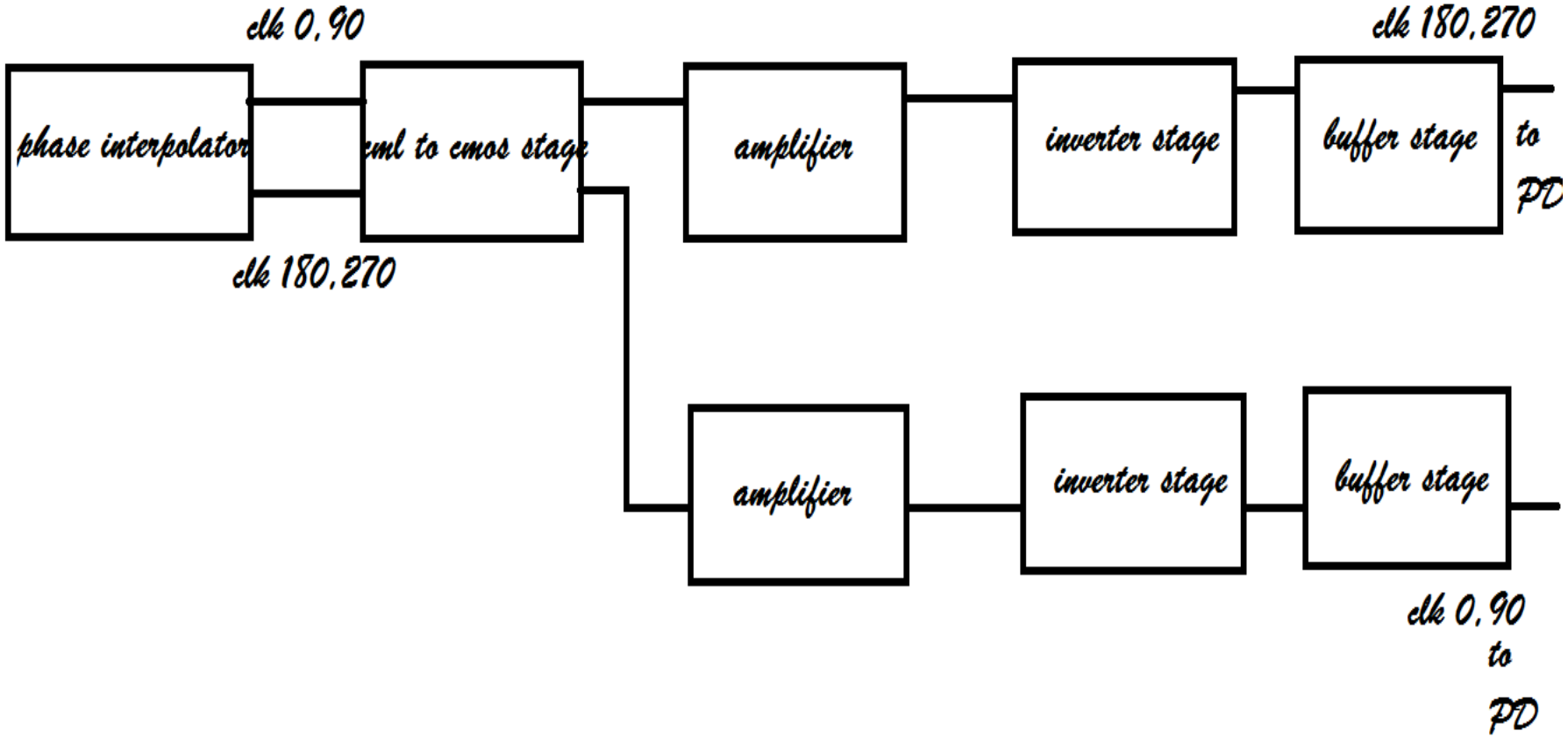
Why do we need a CML to CMOS converter

•A CML to CMOS converter is an intermediate block in the CDR loop between the phase interpolator and the PD.

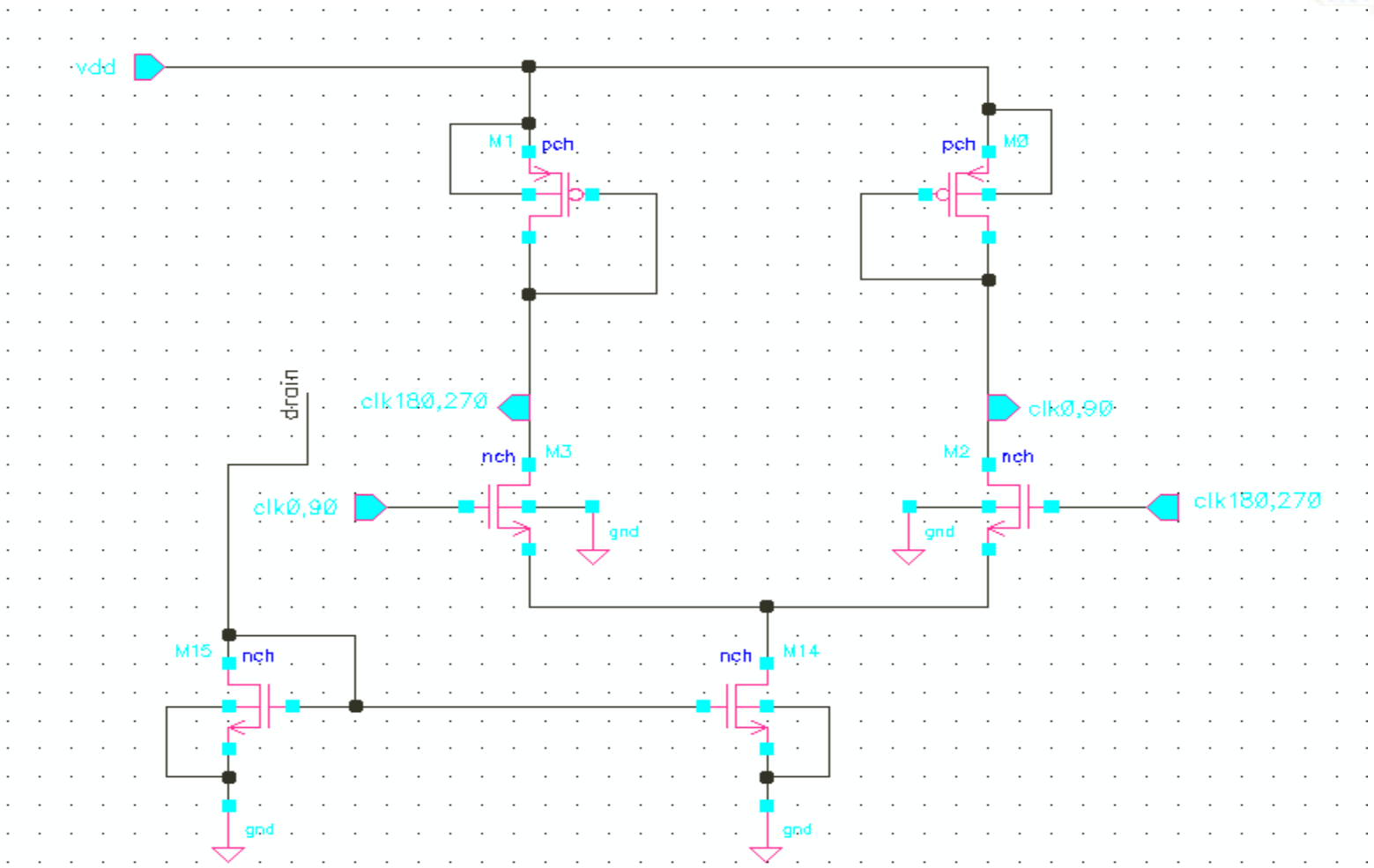
• it converts the small swing output from the phase interpolator that uses CML circuits into a large swing that can drive the PDN and PUN CMOS circuits in the PD functionally.

•This avoids large power consumption and degradation in noise margins.

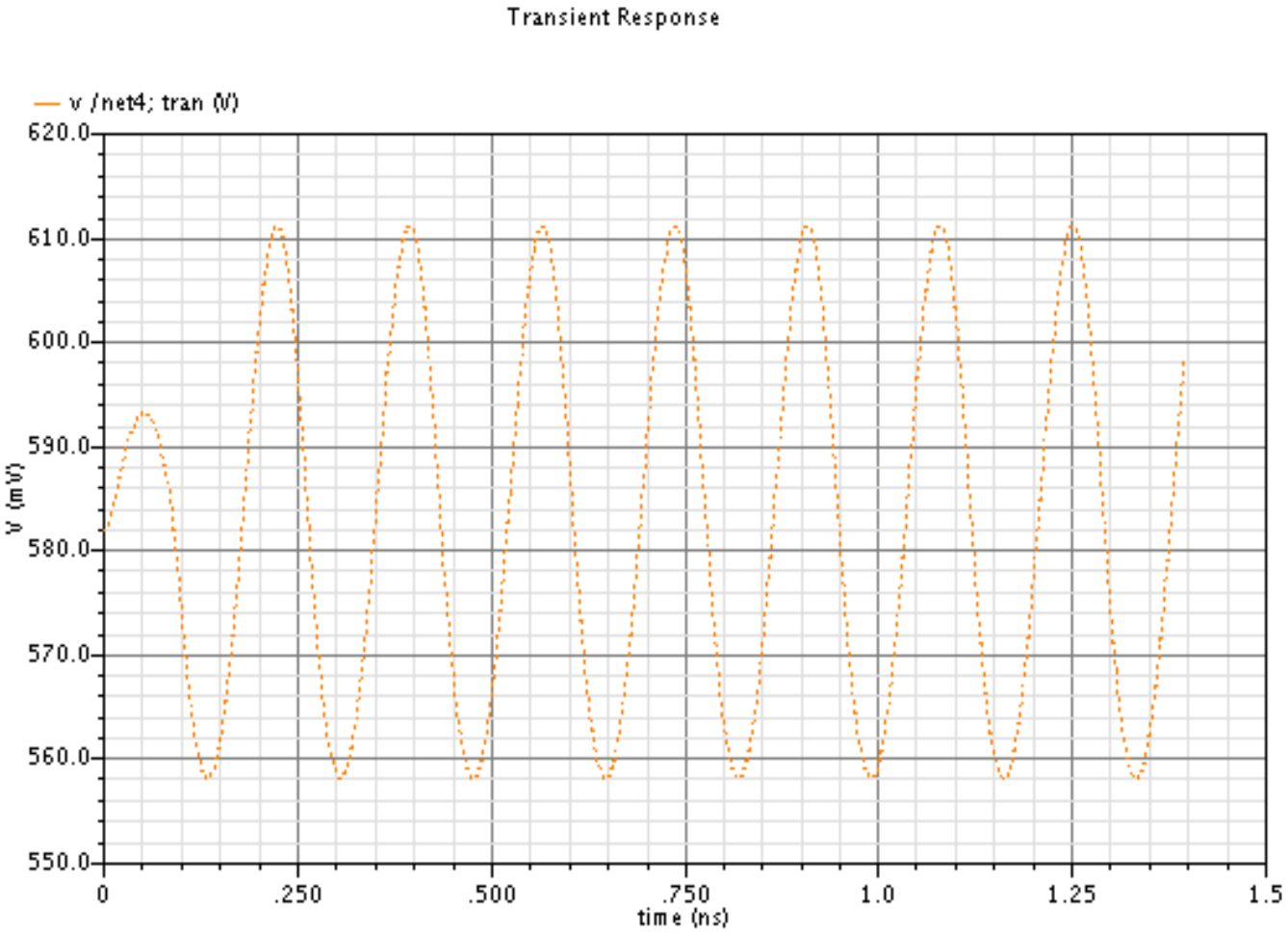
Stages used in a CML to CMOS converter



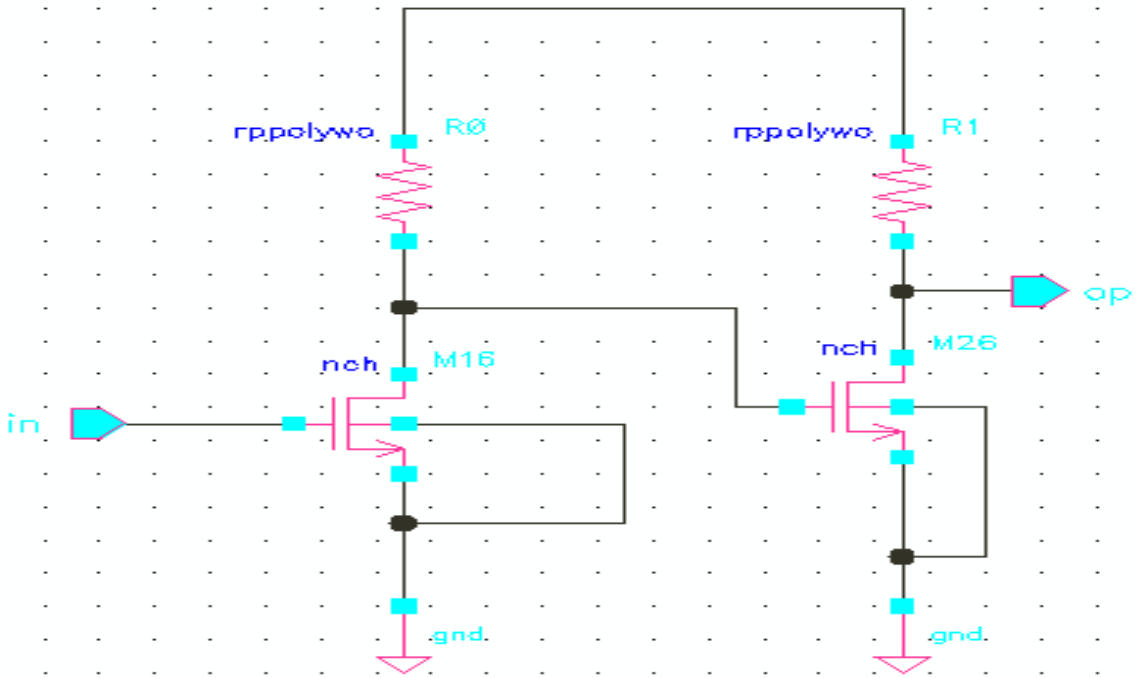
CML to CMOS stage



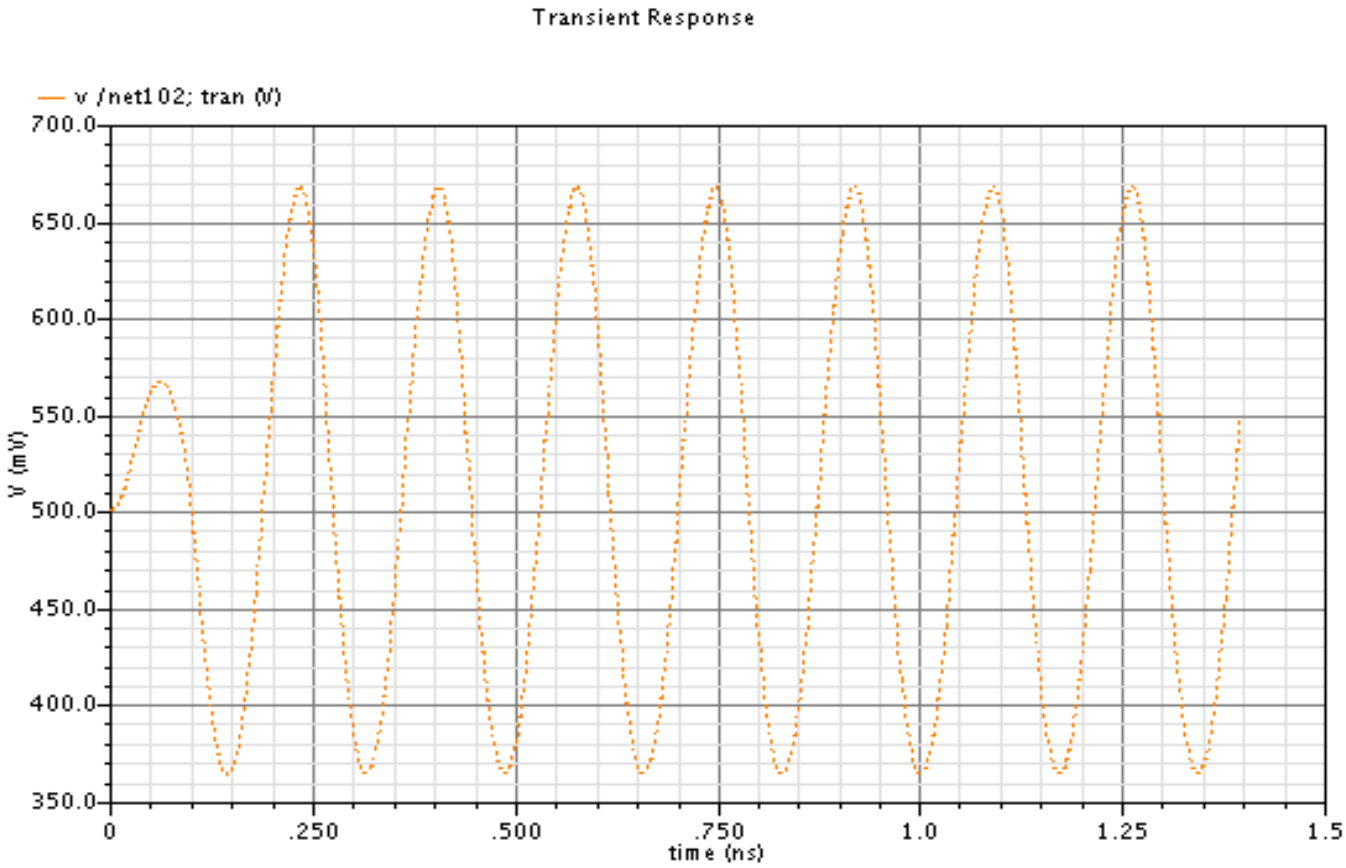
CML to CMOS stage output.



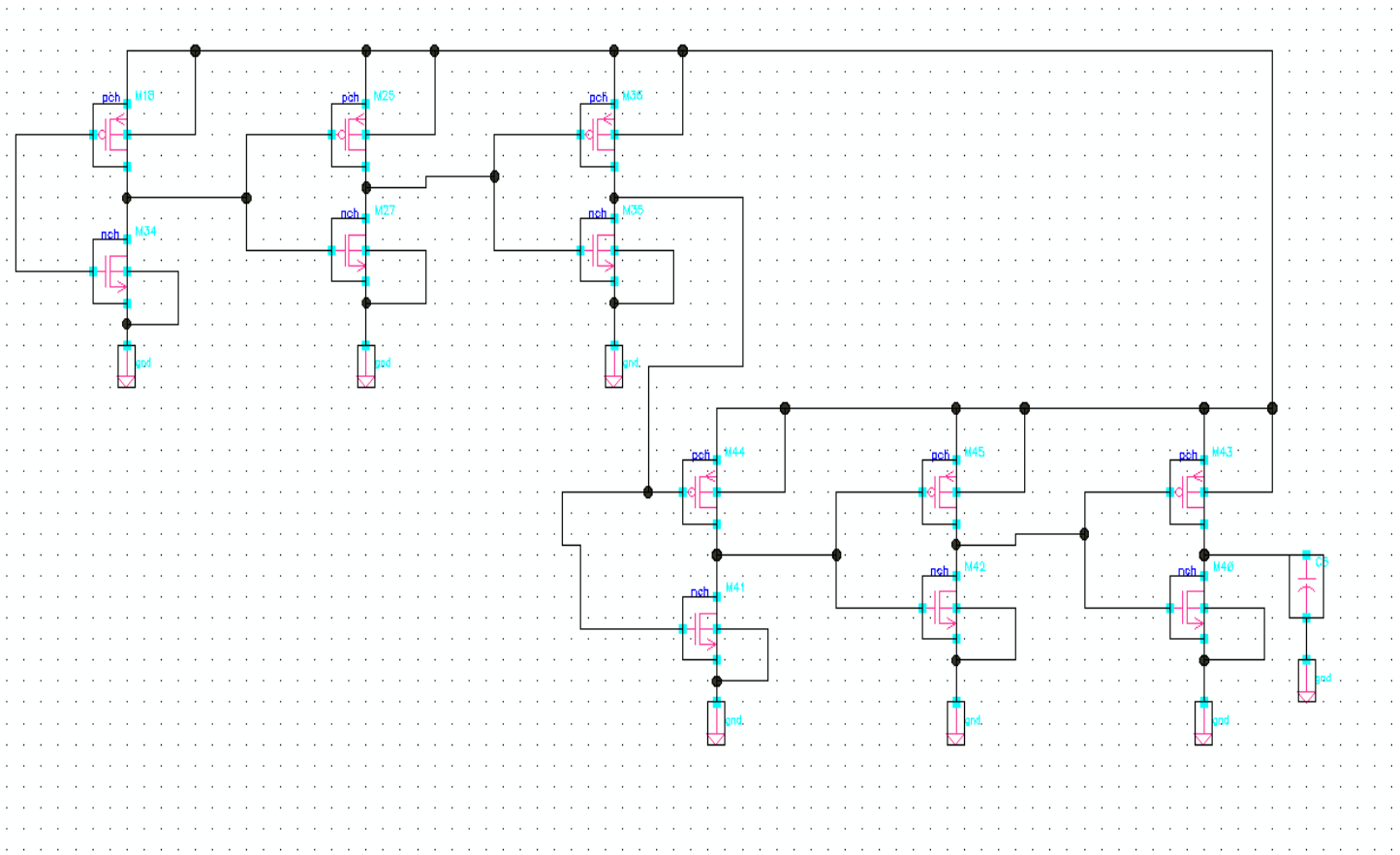
Amplifier stage.



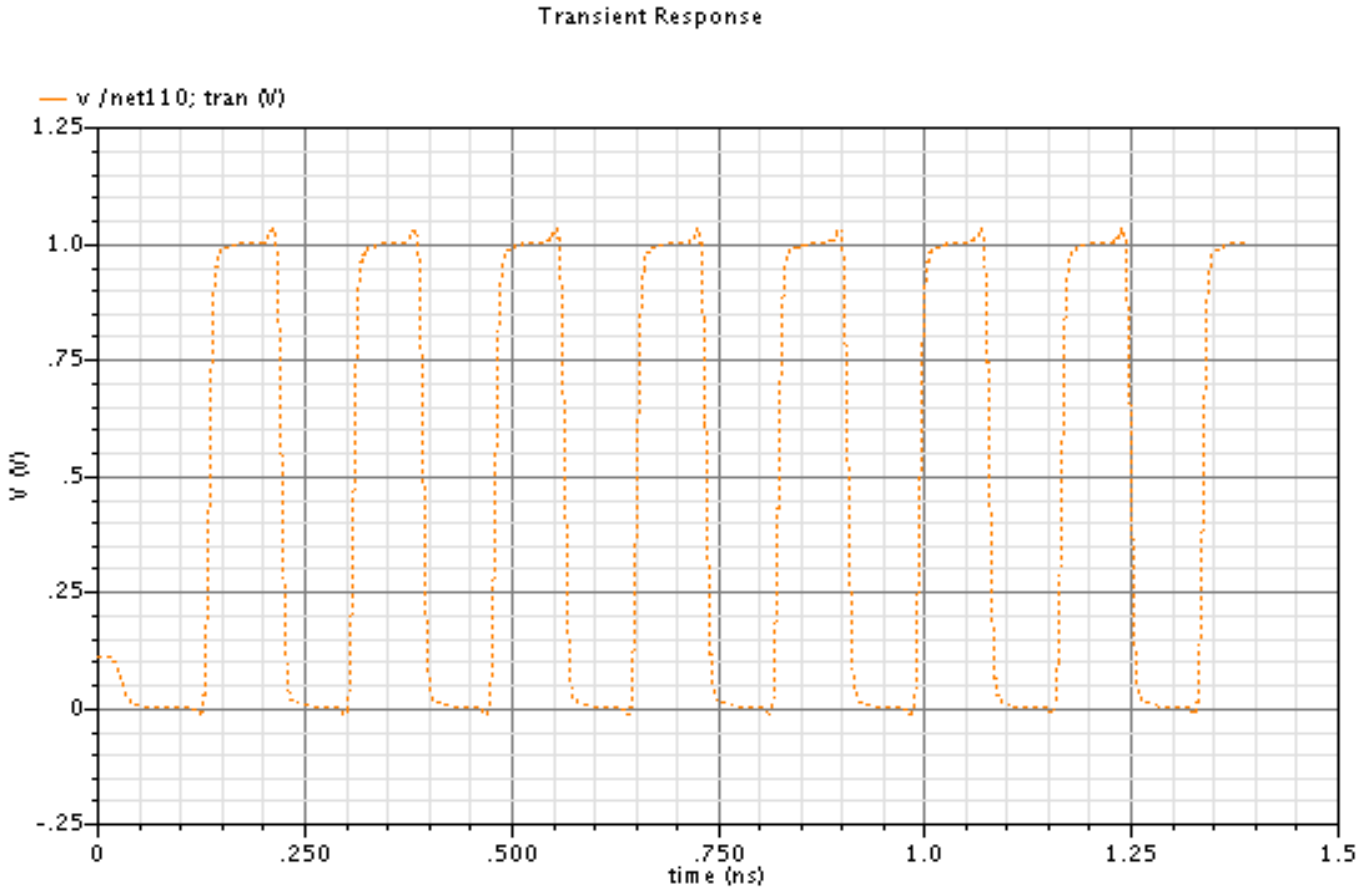
Amplifier stage output.



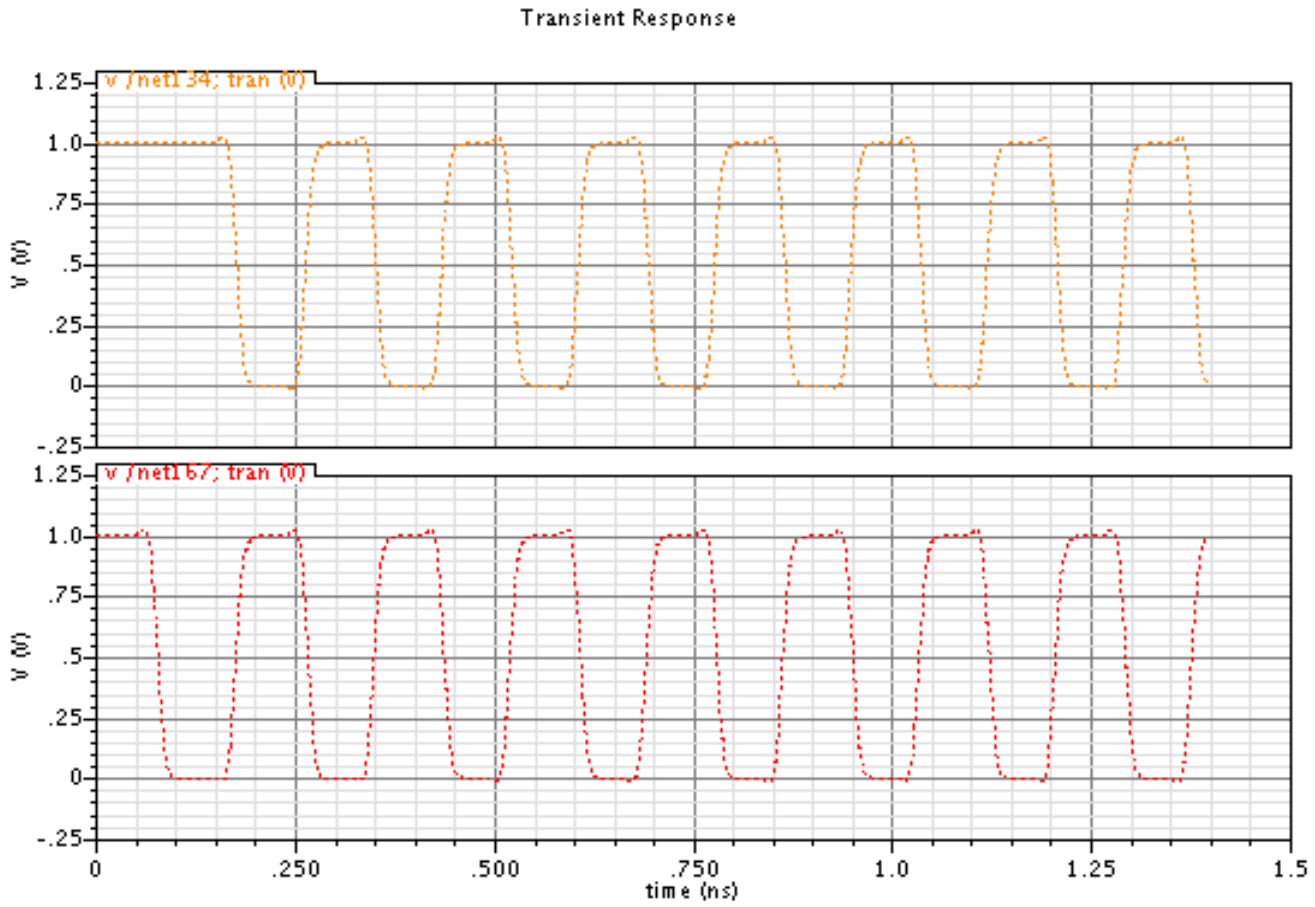
Inverters and Buffer stages.



Inverters output.



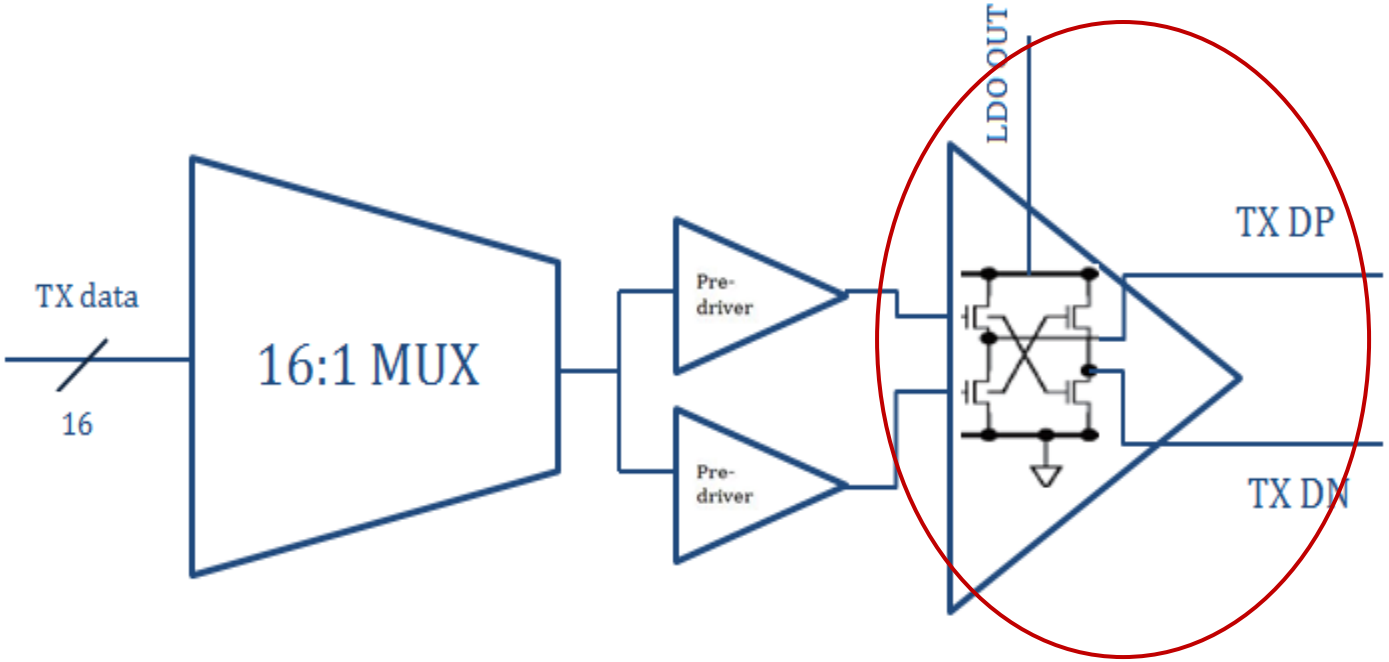
Buffers output.



Specifications:

Supply Voltage	1 V
Supply Current	7.75 mA
Power	7.75 mW

Driver

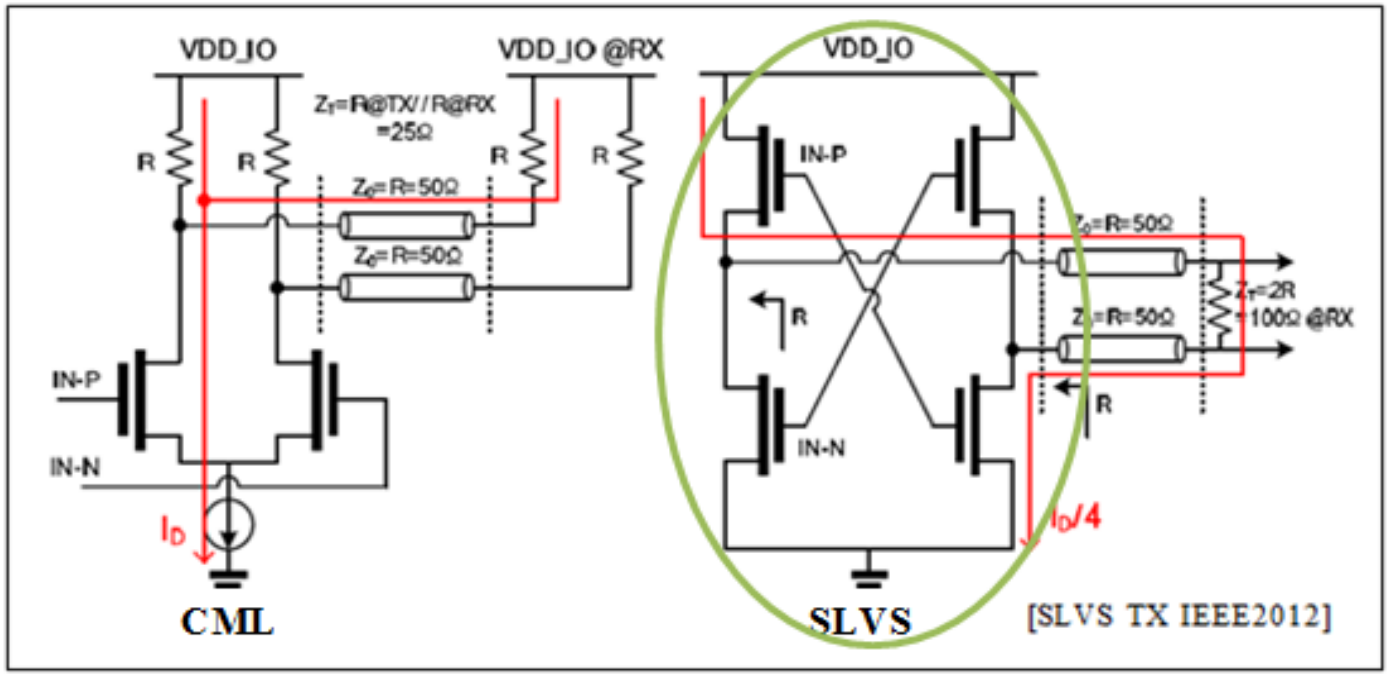


Presented by : Mirna Mokhtar and
Marina Labib

Outlines

- Topologies of Driver
- LA & SA Driver
- Termination Control
- Final design circuit
- Simulation Outputs and Specs.

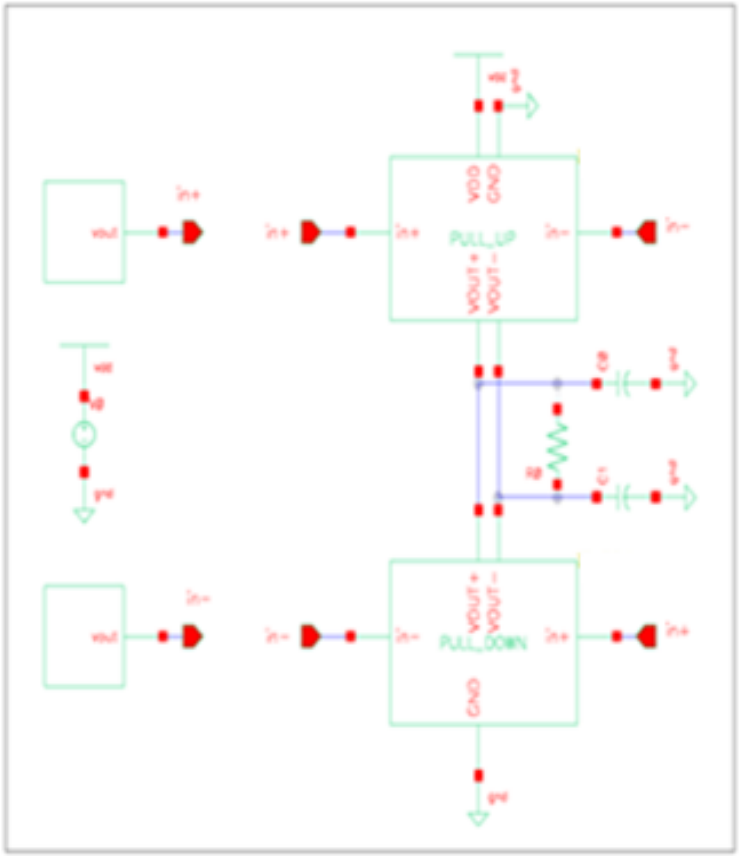
Topologies of Driver



SLVS consumes only 25% of the static output power of the CML

LA & SA Driver

- Large amplitude →Vdd=0.4V
- Small amplitude →Vdd =0.2V
- For low-swing (<400-500mVpp), an all NMOS driver is suitable
- For high-swing, CMOS driver is used.



LA & SA Driver (cont.)

Advantages of low swing driver:

- Higher speed →Devices switch faster.
- Smaller device →Lower capacitance.
- Better linearity →Driver transistor stays in a single region of operation when ON.

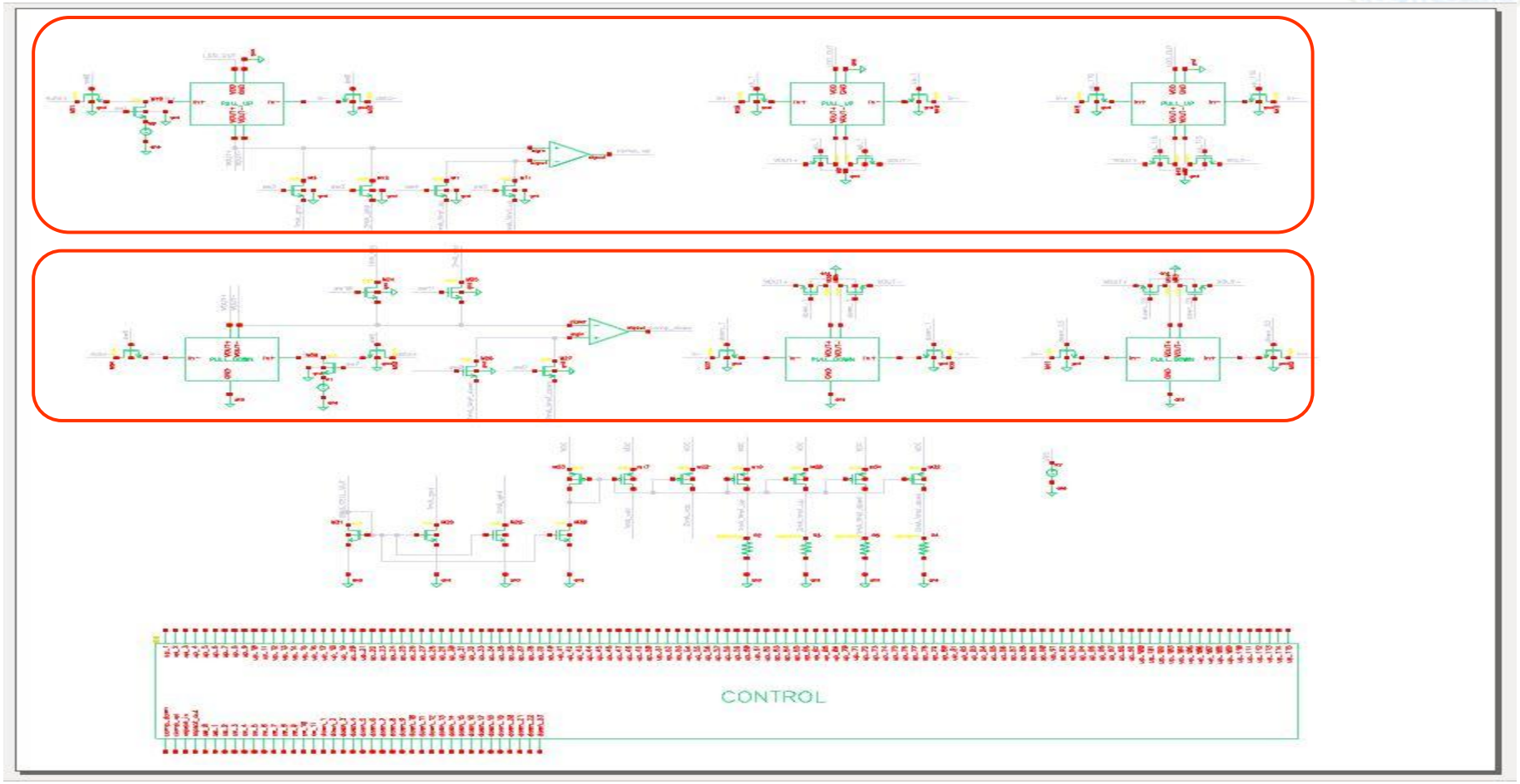
Termination Control

- Segmented Driver → implementation depends on output swing requirements but as supply voltage changes, the implementation does not change; only the number of segments differs to achieve matching.

- The resistance provided by the mosfets vary across the process corners so we need to calibrate the termination in order to reduce signal reflections.

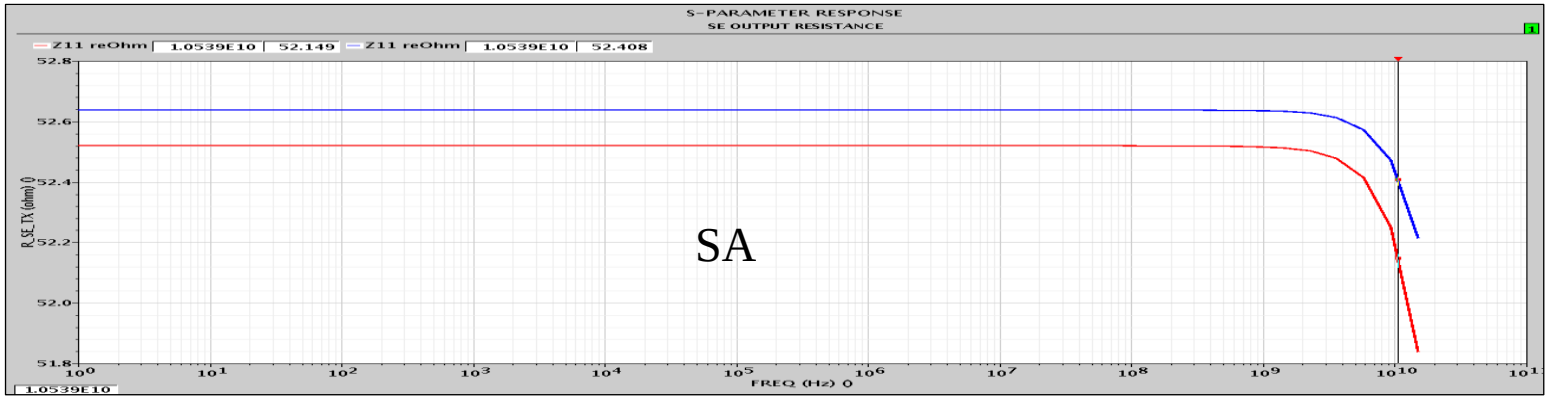
- The termination circuit consist of 22 fixed segments and 78 controllable unit segments tied together for pull up network and 23 controllable unit segments tied together for pull down network. The fixed segments are always turned on, and other unit segments will be set by calibration.

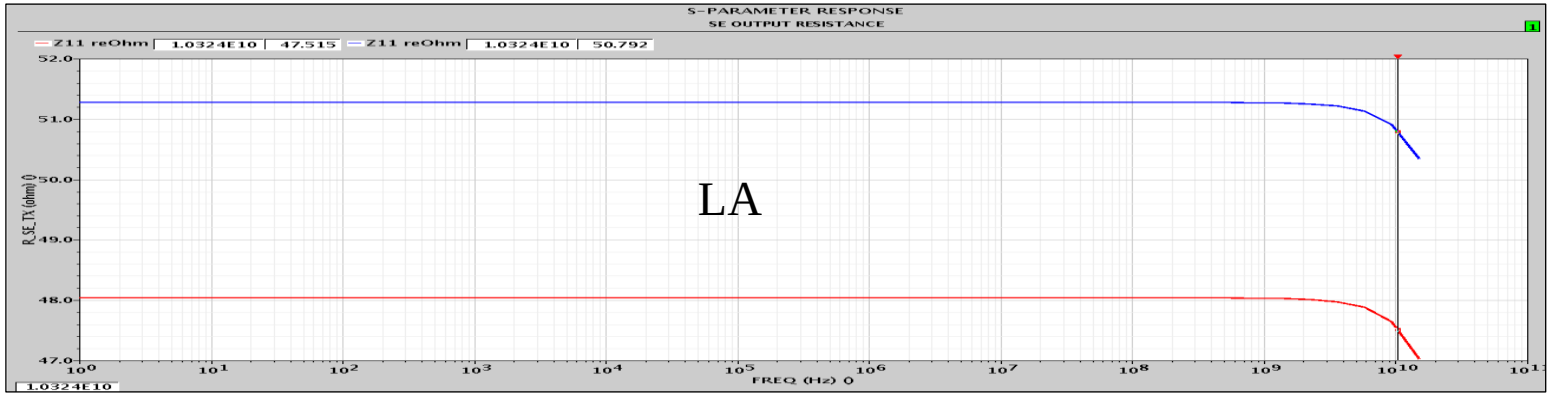
Final design circuit



Simulation Outputs and Specs

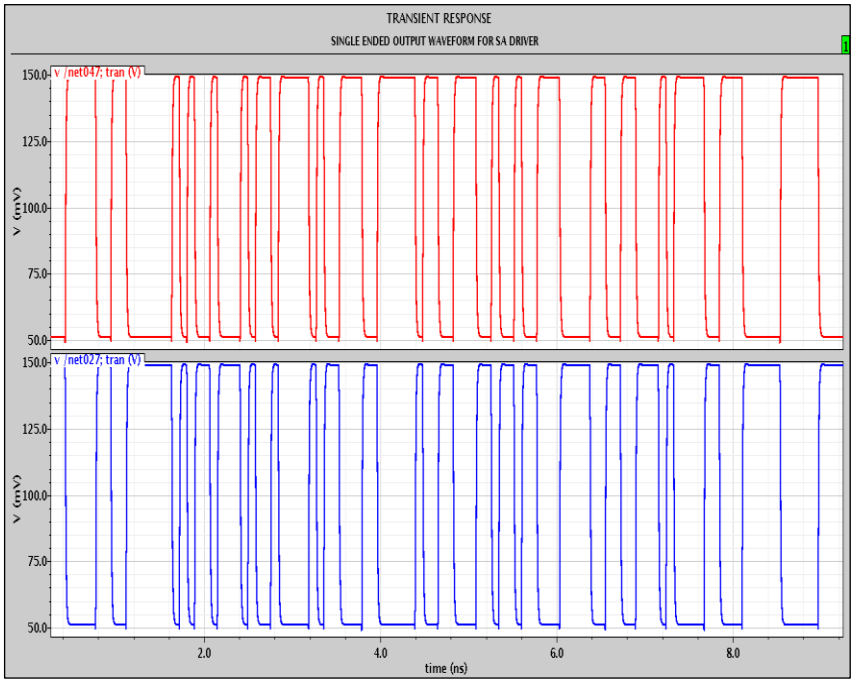
- RSE_TX (Single ended output resistance) in the range from 40 Ω up to 60 Ω.
- Δ RSE_TX (Output resistance mismatch) is 6 Ω.



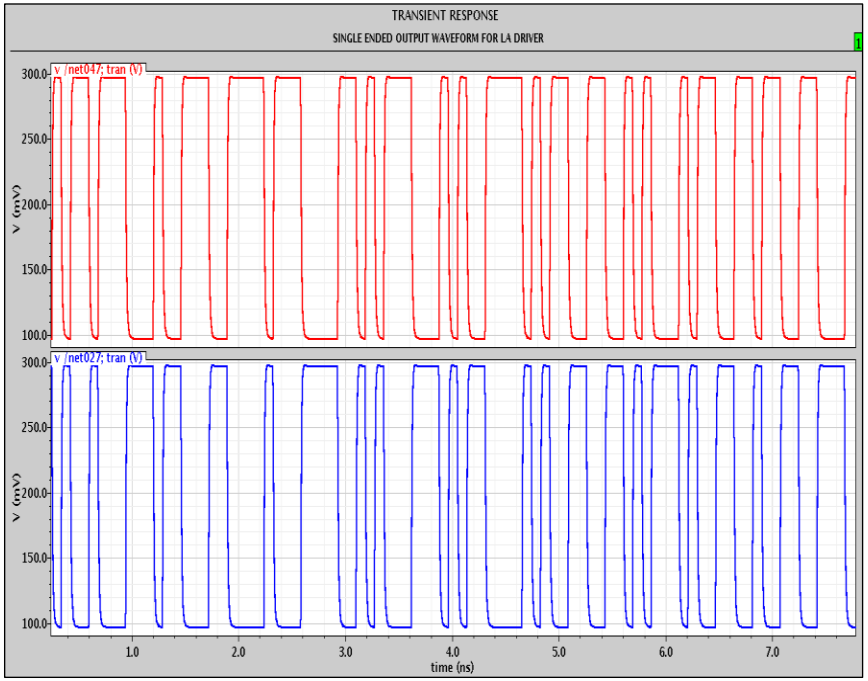


Simulation Outputs and Specs(cont.)

Symbol	MIN	MAX
$V_{DIF\_DC\_LA\_Rt\_TX}$	160mV	240 mV
$V_{DIF\_DC\_SA\_Rt\_TX}$	100 mV	130 mV
$V_{CM\_LA\_TX}$	160 mV	260 mV
$V_{CM\_SA\_TX}$	80 mV	190 mV

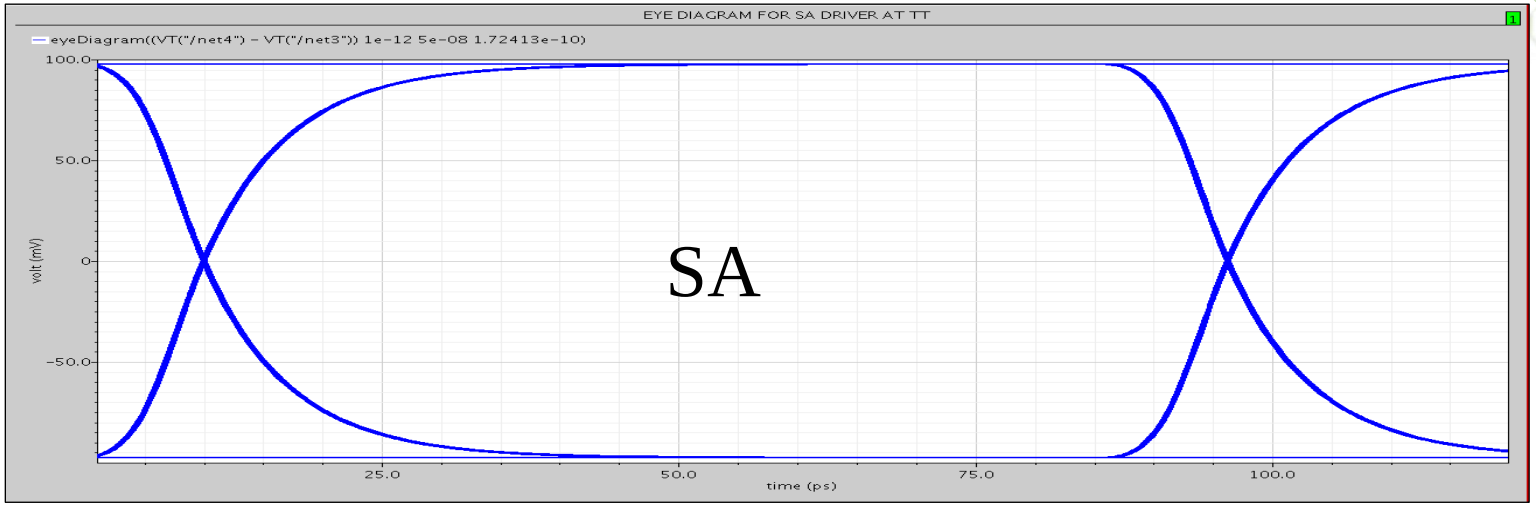


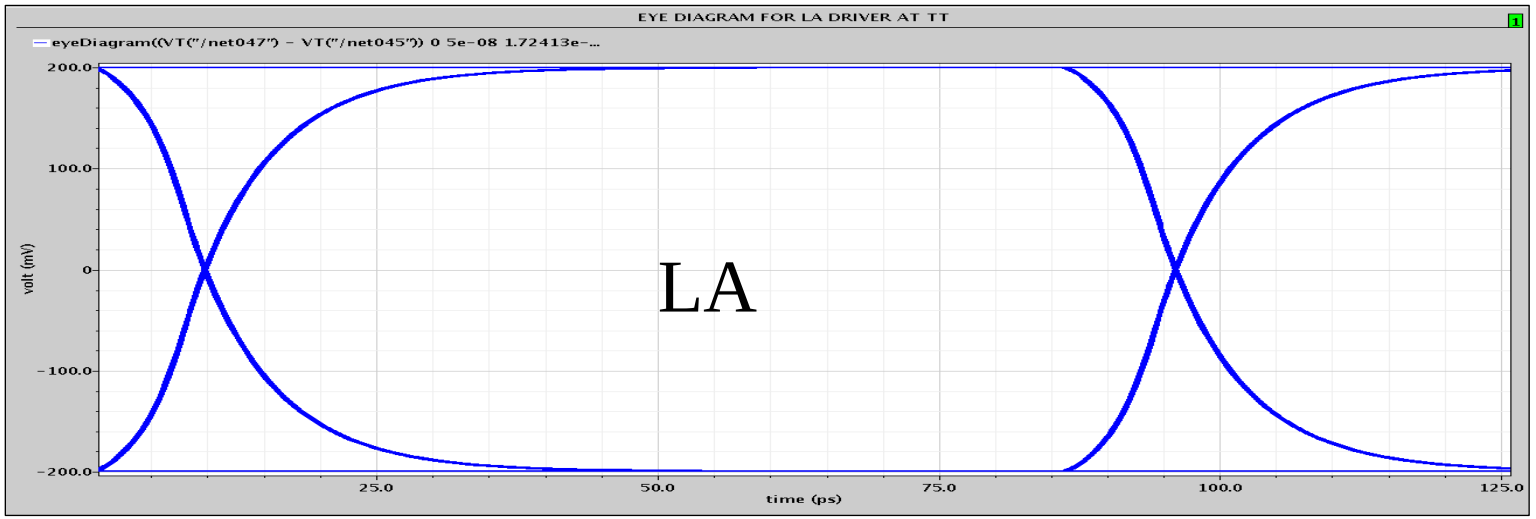
SA



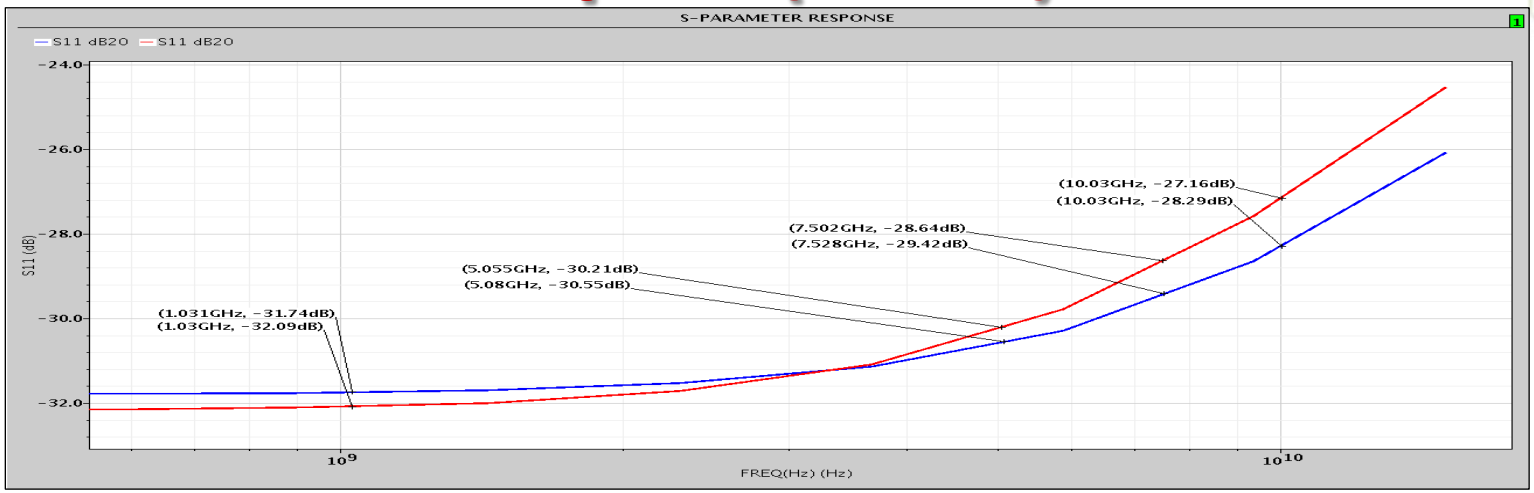
LA

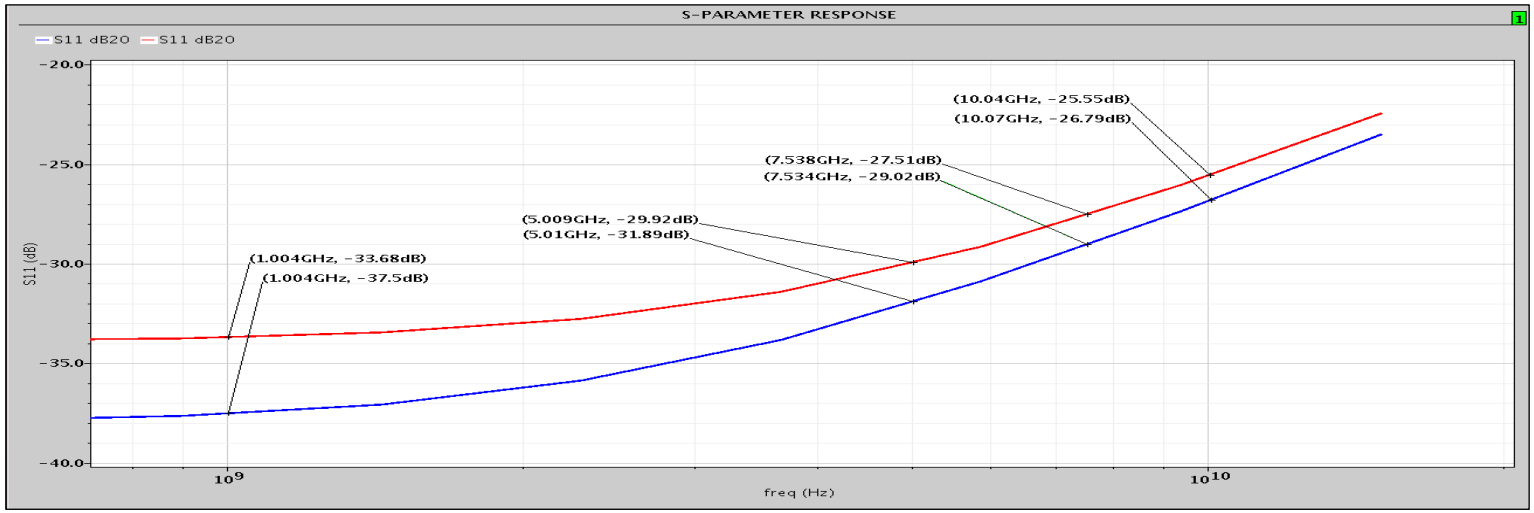
Simulation Outputs and Specs(cont.)





Simulation Outputs and Specs(cont.)

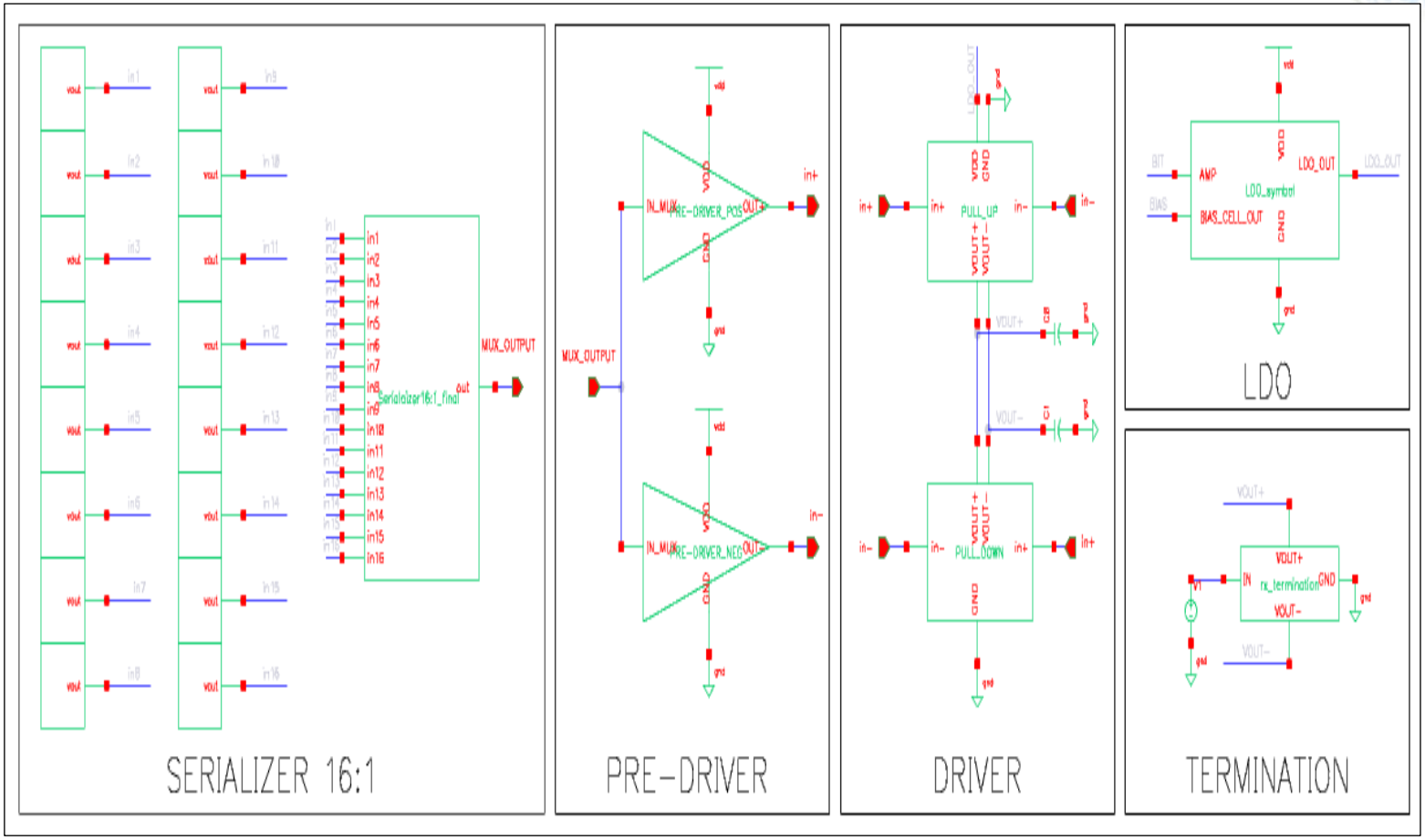




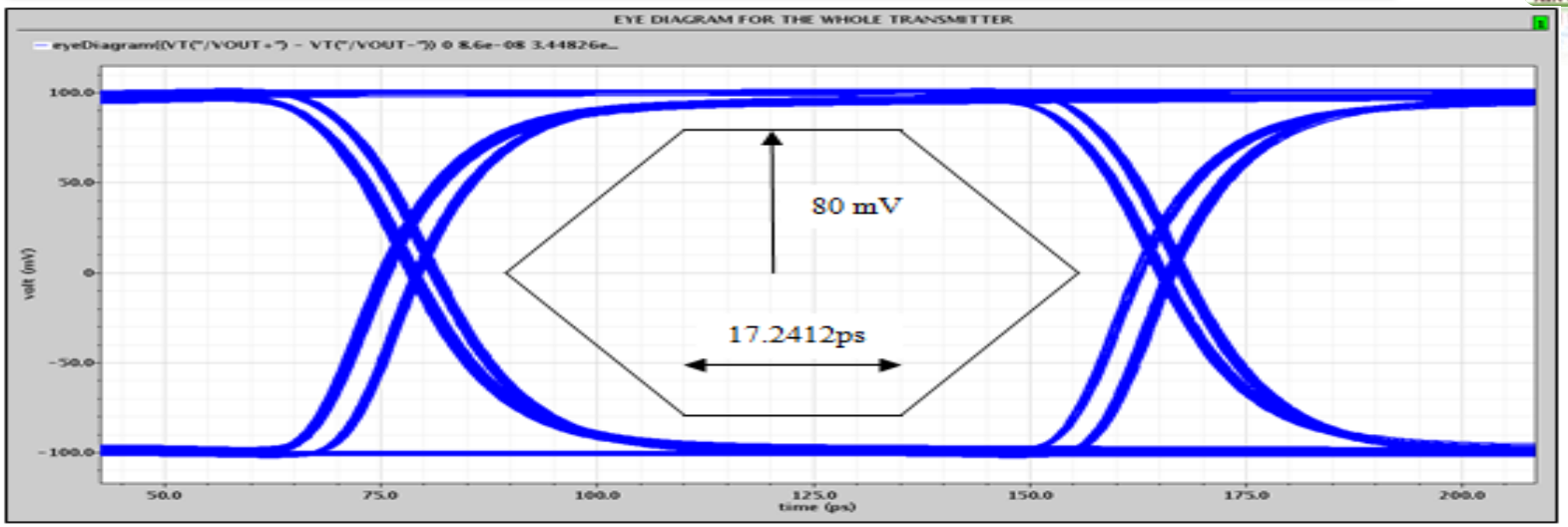
Simulations Outputs and Specs(cont.)

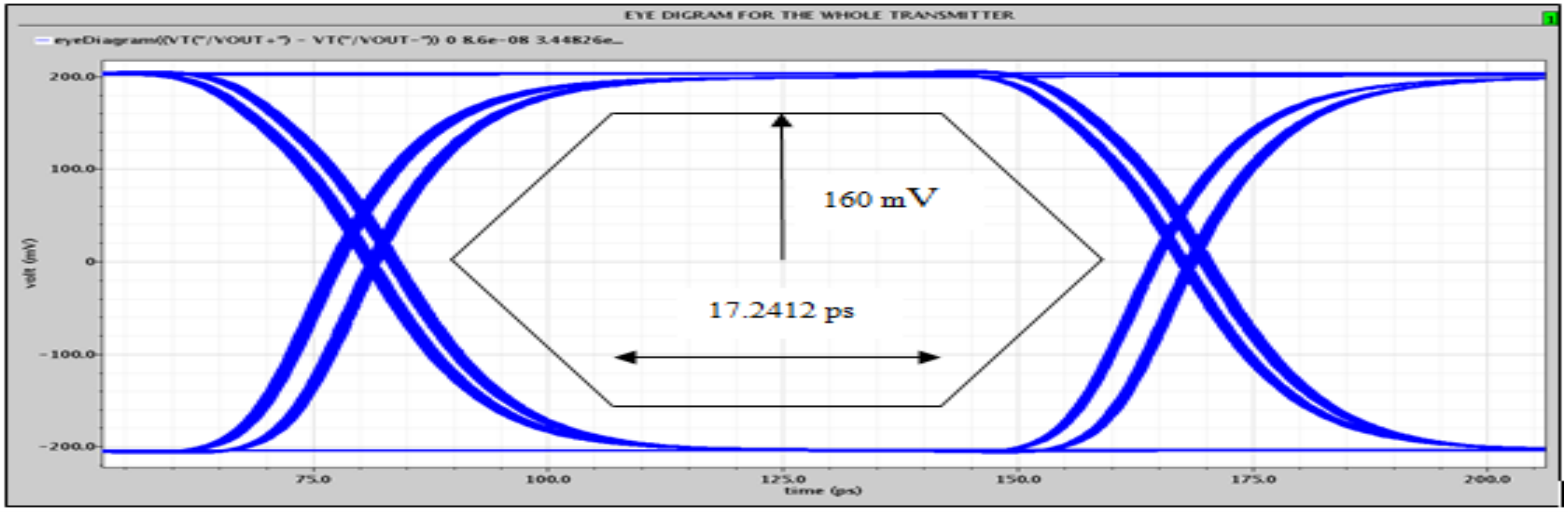
	SA	LA
VDD	0.2V	0.4V
Current	1mA	2mA
Power	200µW	800µW

Whole Transmitter



Whole Transmitter (cont.)





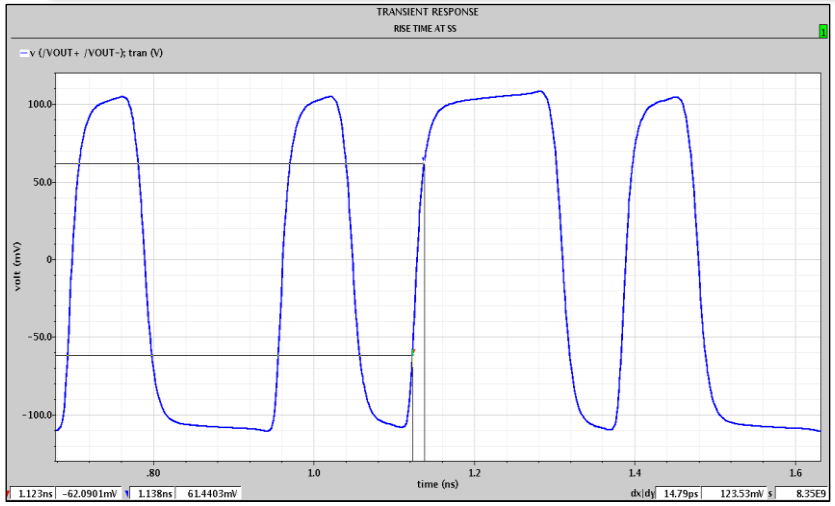
Whole Transmitter (cont.)

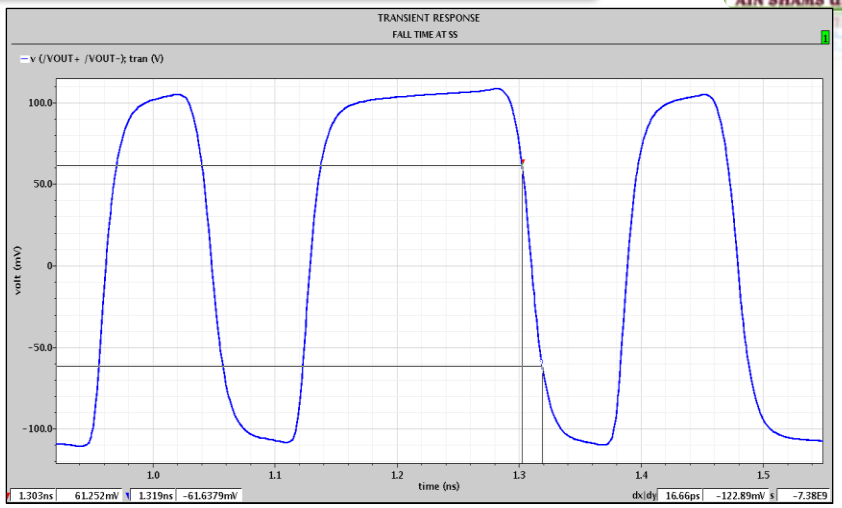
- Rise and Fall times are defined as transition times between the 20% and 80% signal levels of the differential output

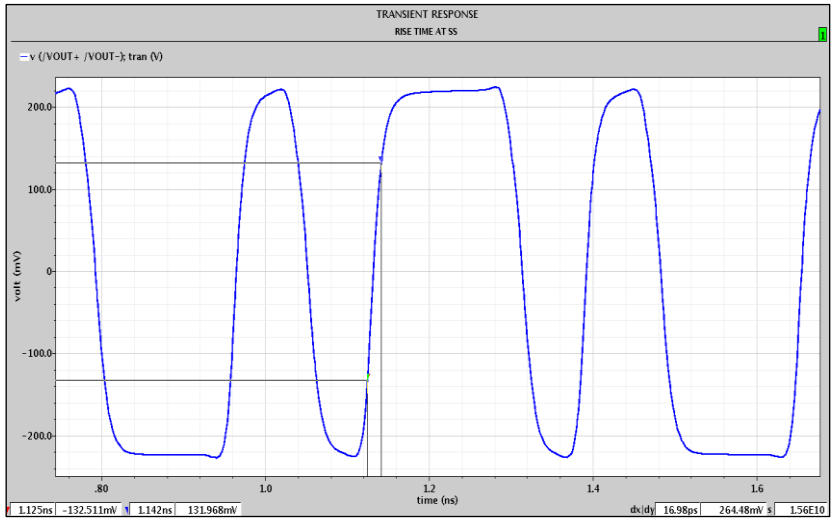
- Rise and Fall time = 0.2 UI

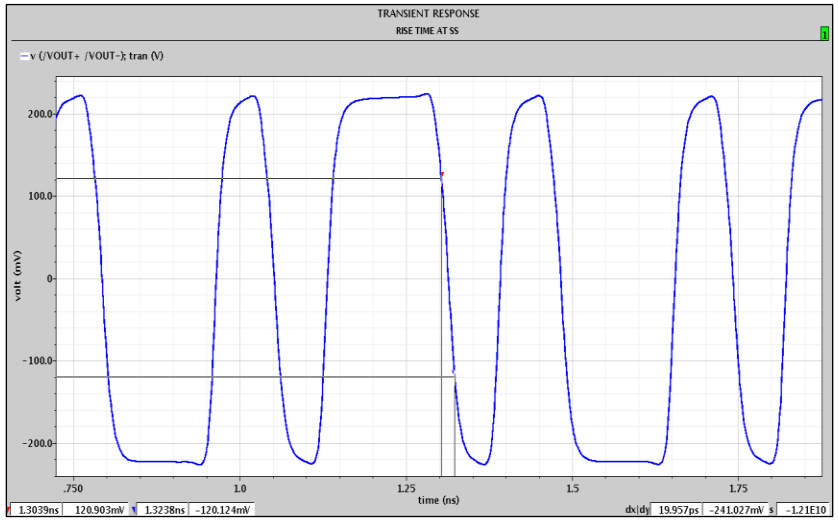
Corner	Amplitude	Rise Time (ps)	Fall Time (ps)
TT	SA	13.172	14.242
SS	SA	14.79	16.66
TT	LA	12.9291	17.218
SS	LA	16.98	19.957

Whole Transmitter (cont.)

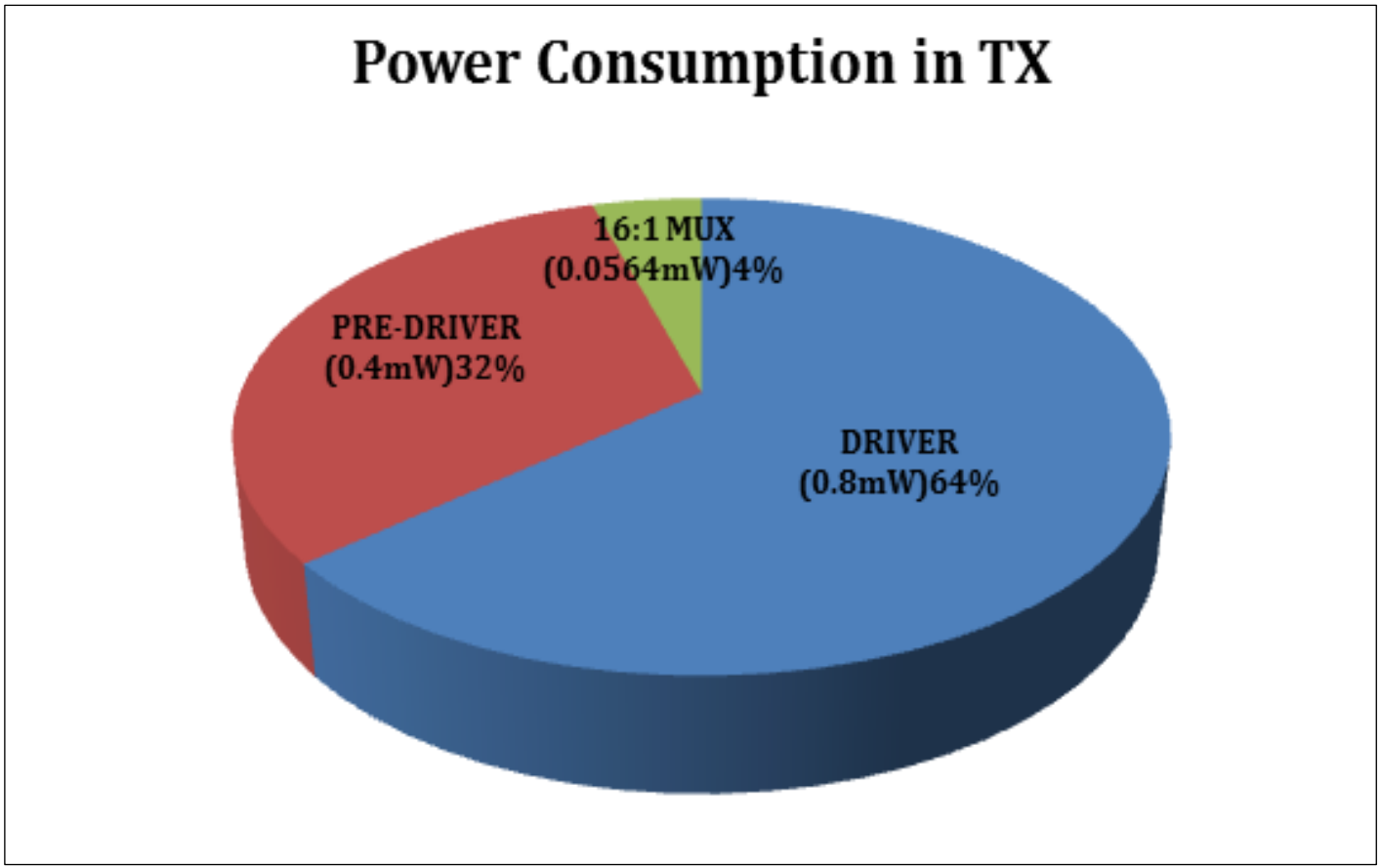








Whole Transmitter (cont.)



Receiver

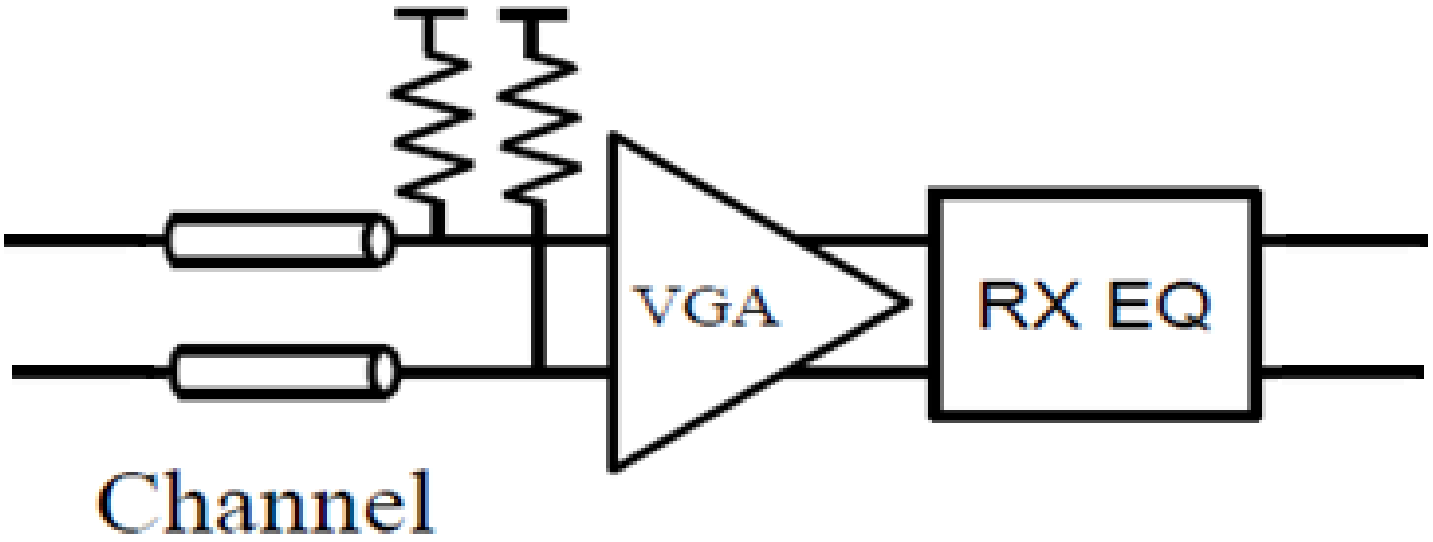
Outlines

- Introduction.
- Termination.
- Variable gain amplifier.
- Continues time linear equalizer.
- CDR.
  - Phase Detector and Charge Pump (PD and CP).
  - Analog Phase Interpolator (PI).
- De-Serializer.

Receiver Termination

Presented by : Mohamed Mohie

introduction

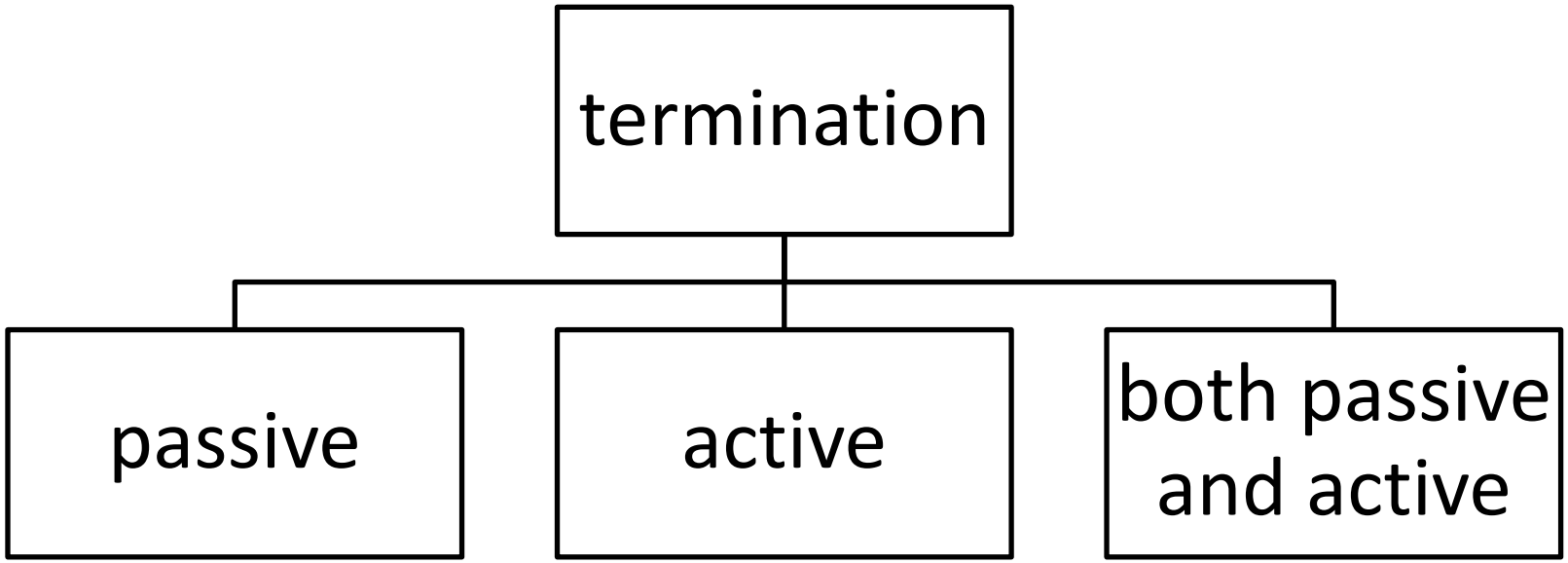


This is the reception of the receiver consist of termination , VGA , CTLE.

Outlines

- Introduction
- topologies
- Circuit and schematic
- Simulations and results

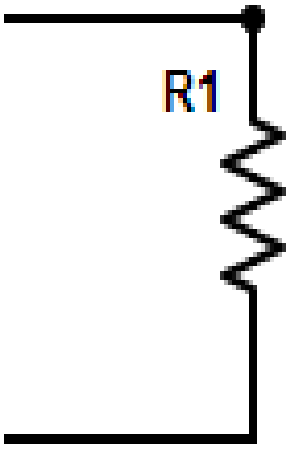
Introduction



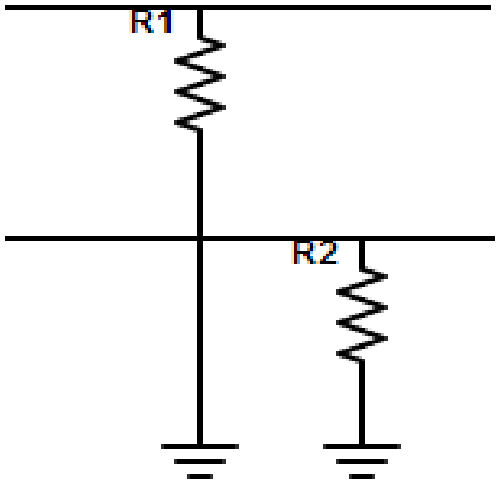
Passive: consist of resistance

Active : consist of transistors

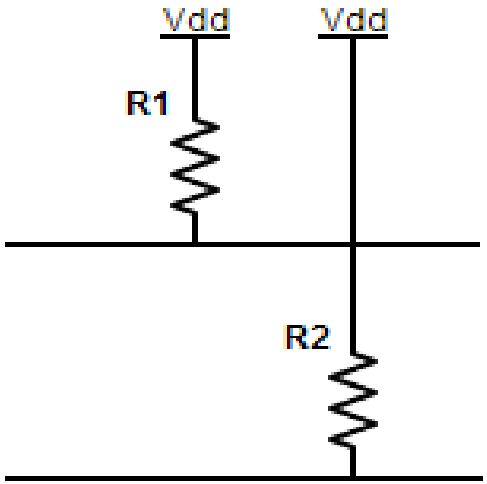
Topologies



Differential resistance

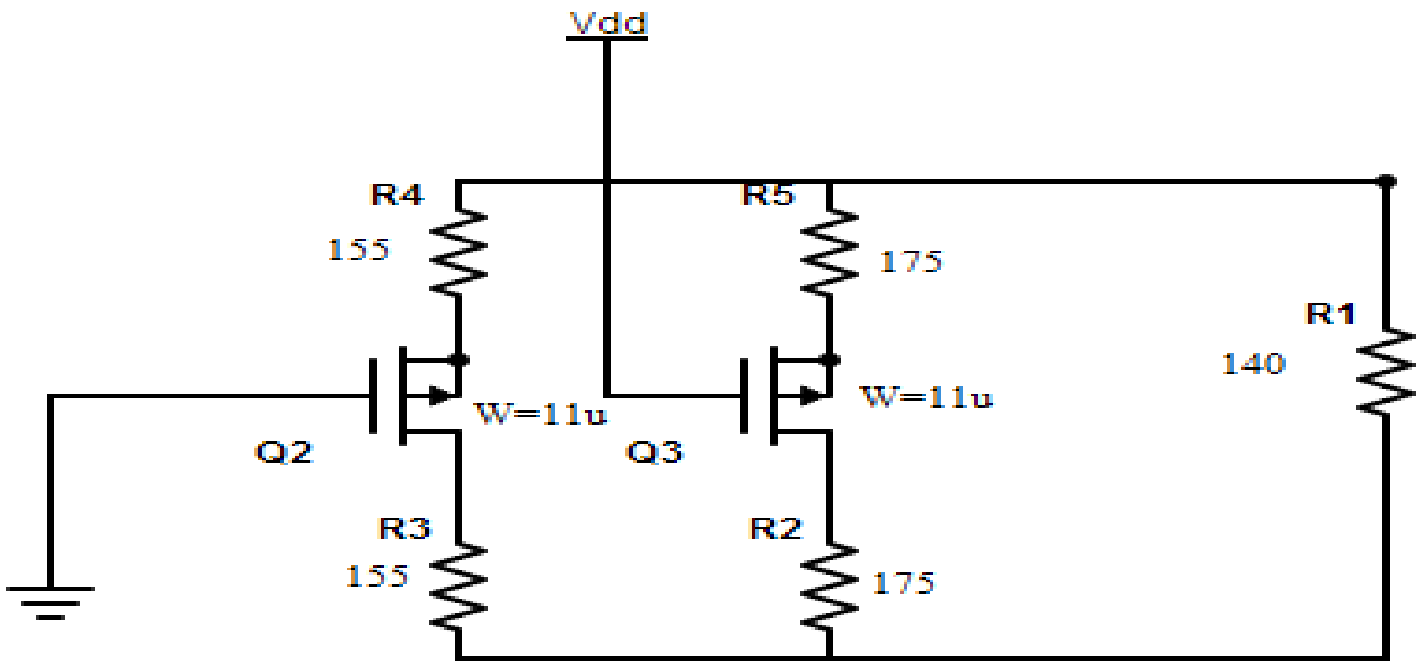


resistance to Gnd



resistance to Vdd

Circuit and schematic

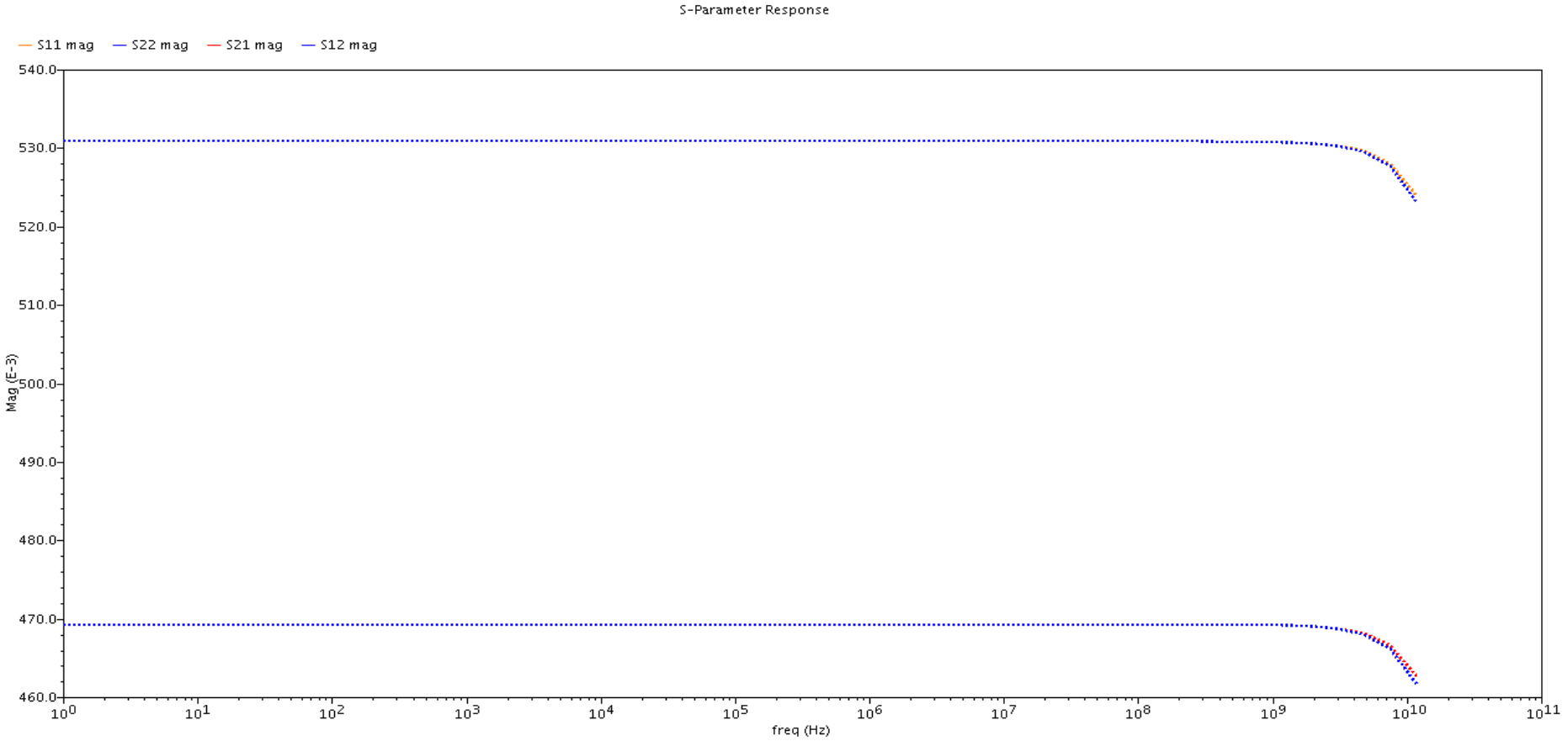


it's a differential termination consist of resistance and transistors where the transistors are used as on/off switch

Simulation and results

- Since we use differential termination we calculate Sdd11 instead of S11
- Sdd11=1/2(s11-s12-s21-s22)

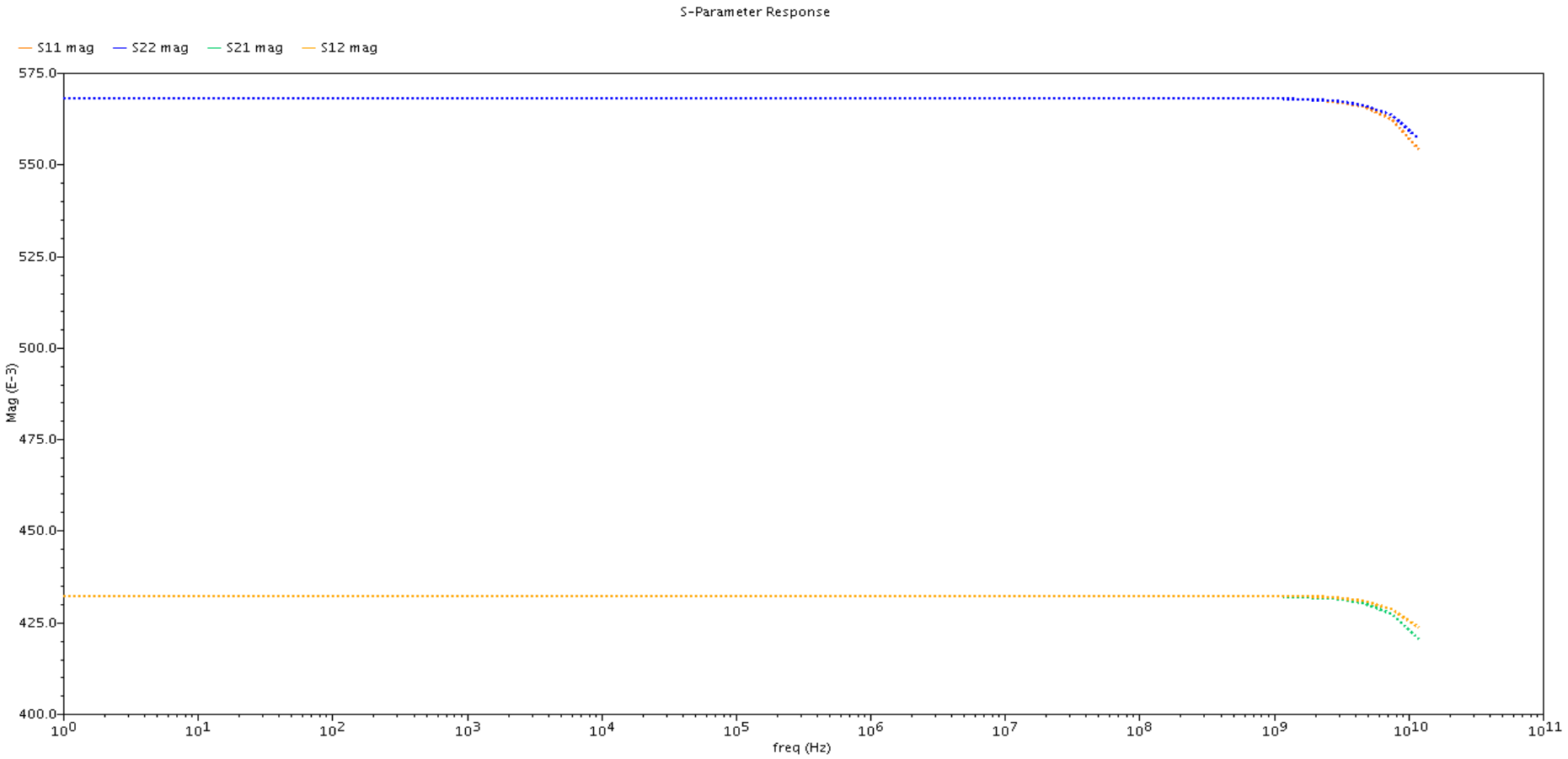
Simulation and results



For TT: S11=S22=0.53 , S12=S21=0.469

Sdd11=-24dB

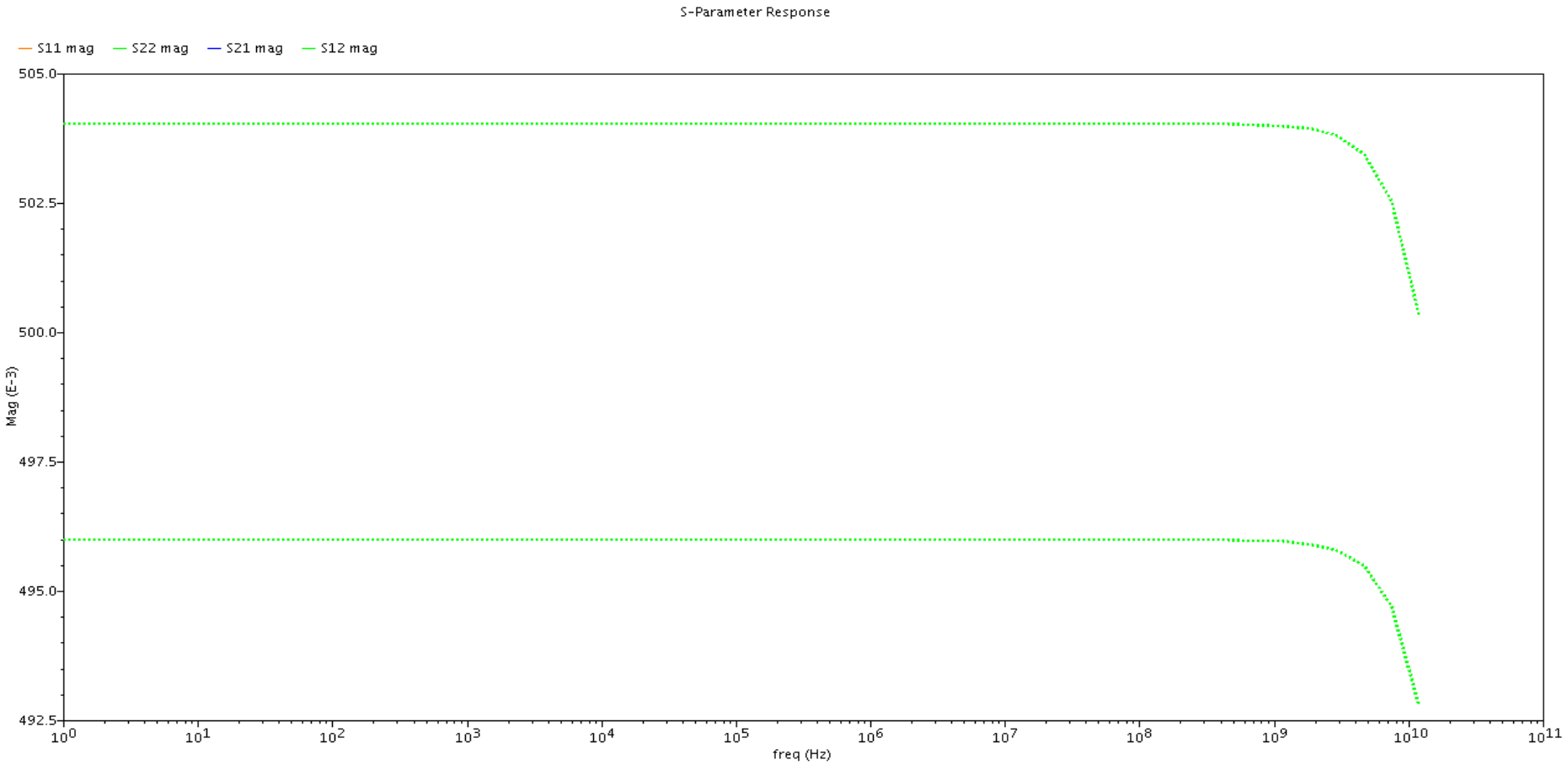
Simulation and results



For SS: S11=S22=0.567 , S12=S21=0.432

Sdd11=-23.4dB

Simulation and results



For FF: S11=S22=0.496, S12=S21=0.504

Sdd11=- infinity

Variable Gain Amplifier (VGA)

Presented by : Mohamed Mohie

Outlines

- Introduction
- Circuit and schematic
- Simulations and results

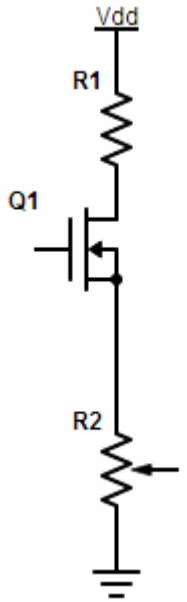
Introduction

•The variable gain amplifier gives different values of gain and it also can make attenuation

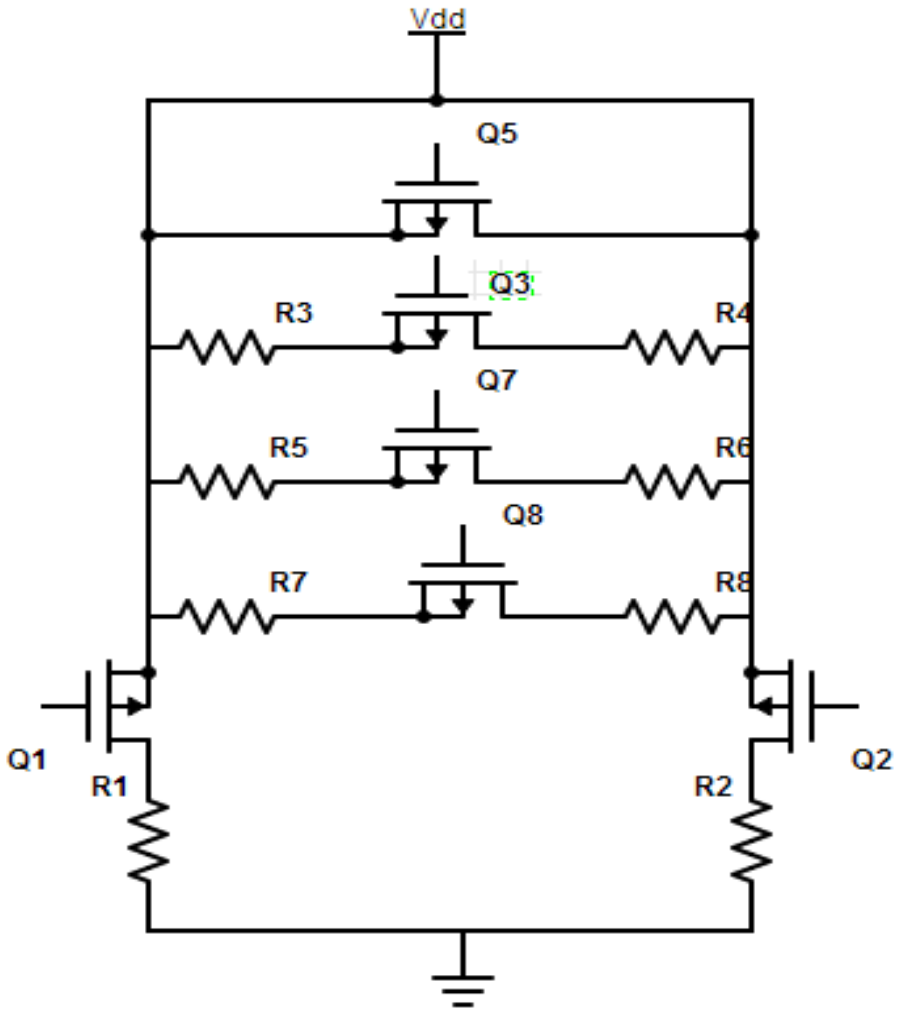
•We use a source degeneration common source amplifier

• it's $gain = \frac{-\text{gm Rout}}{1 + \text{gm RS}}$

•By changing RS we get different values of gain



Circuit and schematic



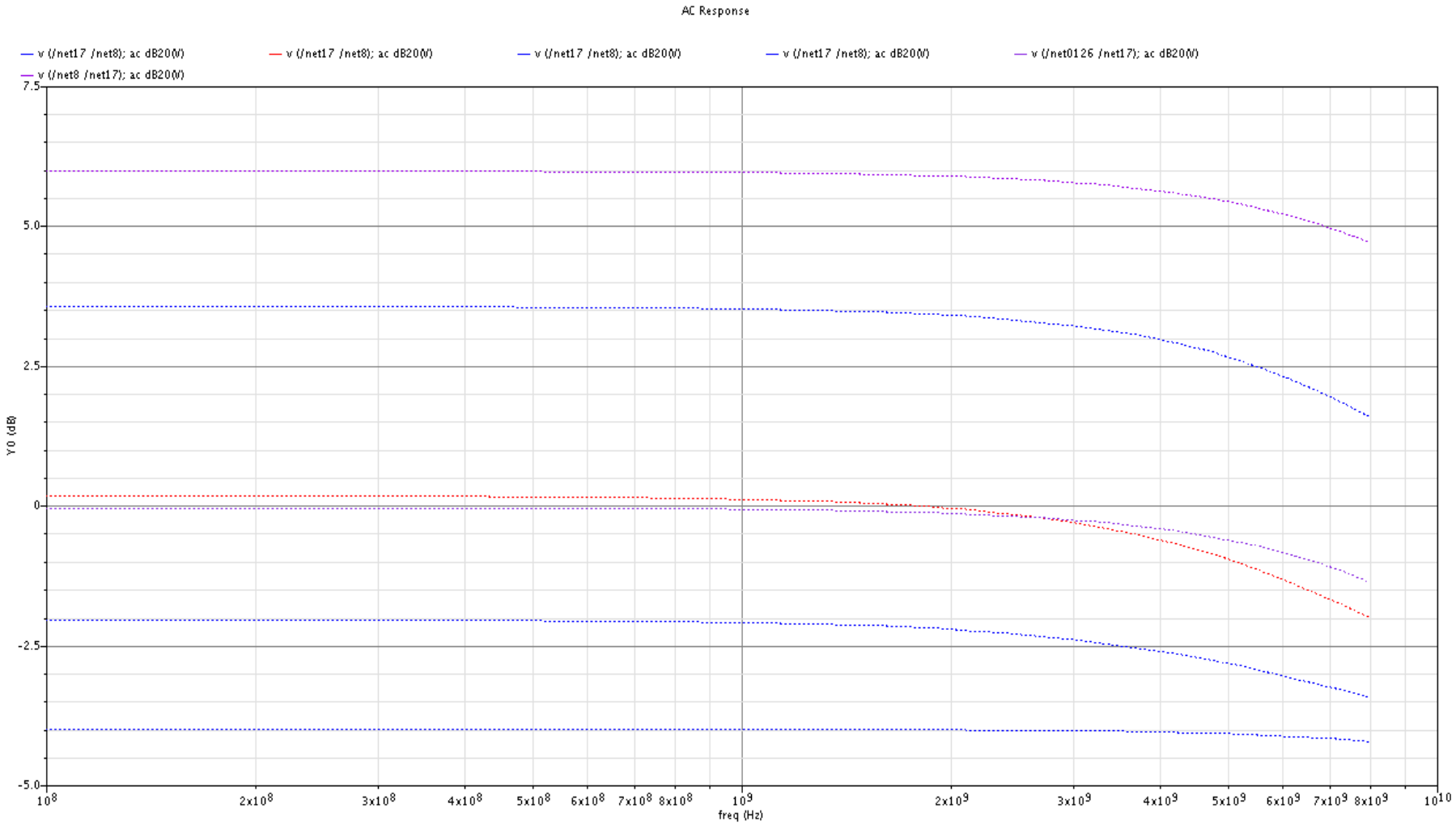
Circuit and schematic

- When Q5 or Q3 or Q7 or Q8 are switched on the circuit gives a certain gain or a certain attenuation , and we can open more than one switch at a time getting more values of gains and attenuations

- This VGA gives range from 5.75dB to -4dB

- The dc input ranges from 25mV to 330mV gives output 200mV

Simulation and results



CTLE
(Receiver Equalization)

Presented by : Reem Amr

Outlines

- Receiver Equalization
- CTLE
- CTLE output
- Composing Receiver circuits
- Verification for correct data from slicer

Receiver Equalization

- Received signal suffers frequency dependent losses .
- To cancel Inter symbol interference (ISI) due dispersion and skin effect.

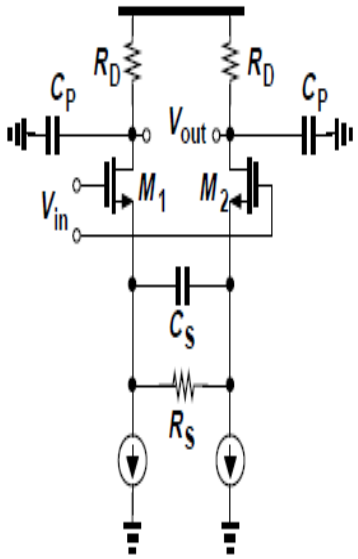
Continuous Time linear Equalizer [CTLE]

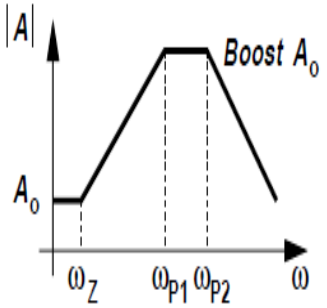
$$H(s)=\frac{g_m}{C_p}\frac{s+\frac{1}{R_S C_S}}{\left(s+\frac{1+g_m R_S/2}{R_S C_S}\right)\left(s+\frac{1}{R_D C_p}\right)}$$

$$\omega_z=\frac{1}{R_S C_S},\quad \omega_{p1}=\frac{1+g_m R_S/2}{R_S C_S},\quad \omega_{p2}=\frac{1}{R_D C_p}$$

$$\text{DC gain}=\frac{g_m R_D}{1+g_m R_S/2},\ \text{Ideal peak gain}=g_m R_D$$

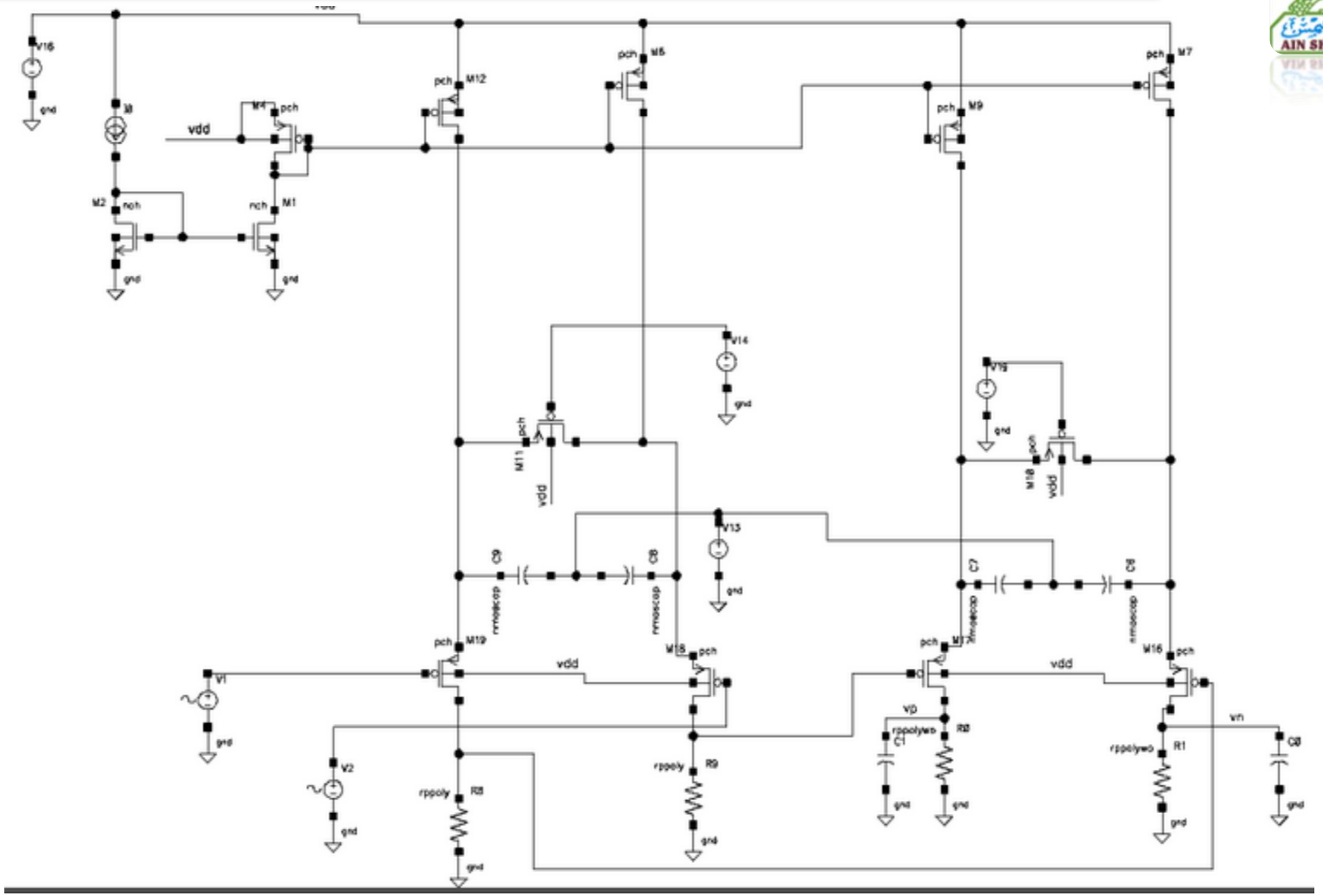
$$\text{Ideal Peaking}=\frac{\text{Ideal peak gain}}{\text{DC gain}}=\frac{\omega_{p1}}{\omega_z}=1+g_m R_S/2$$



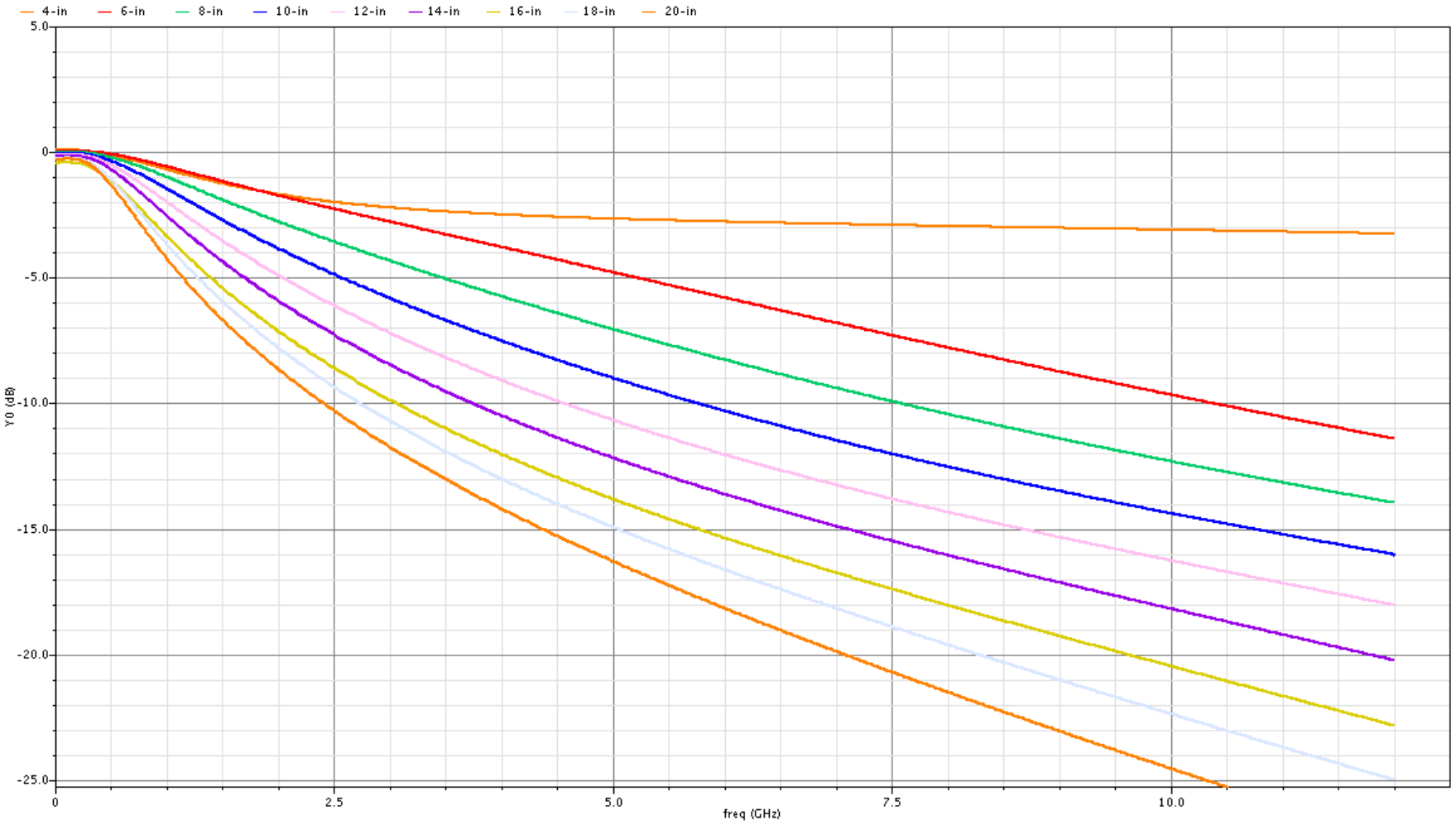


This is the reception of the receiver consist of termination , VGA , CTLE.

Schematic

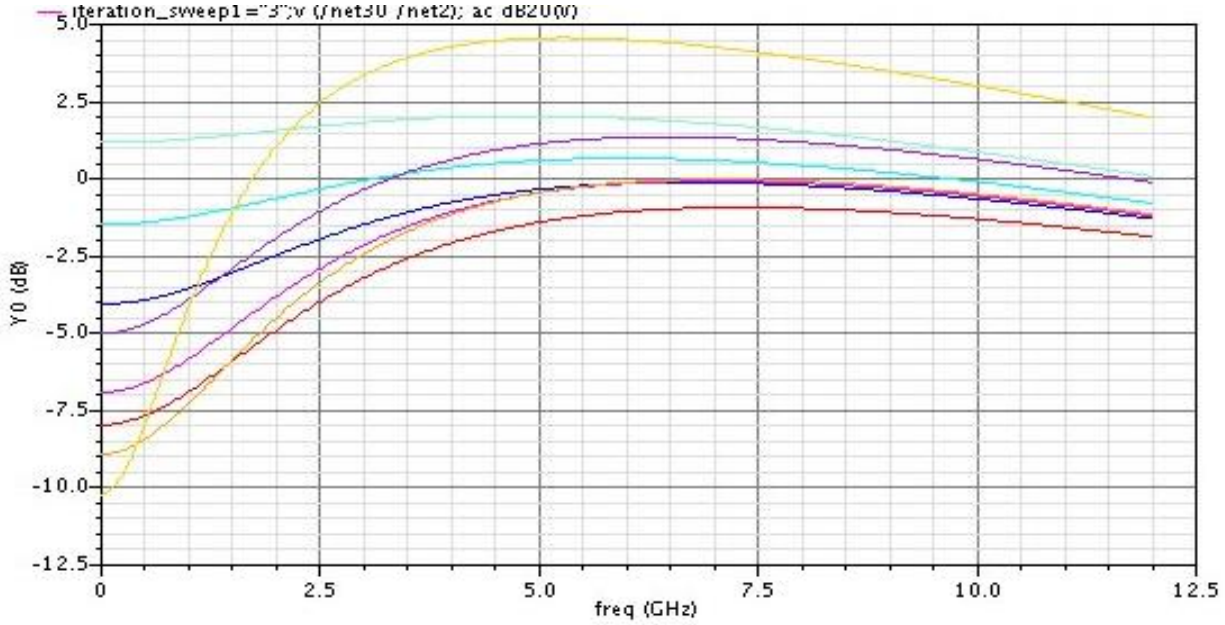

V16
gnd
I8
vdd
M4
pch
M12
pch
M6
pch
M9
pch
M7
pch
M2
nch
nch
M1
gnd
gnd
V14
M11
pch
pch
V15
gnd
M18
pch
vdd
V13
C9
C8
C7
C6
rmoscap
rmoscap
rmoscap
rmoscap
M19
pch
M17
pch
M16
pch
V1
vdd
vdd
vp
vn
V2
rppoly
R8
rppoly
R9
rppolywo
C1
R2
rppolywo
R1
C0
gnd

Channel losses

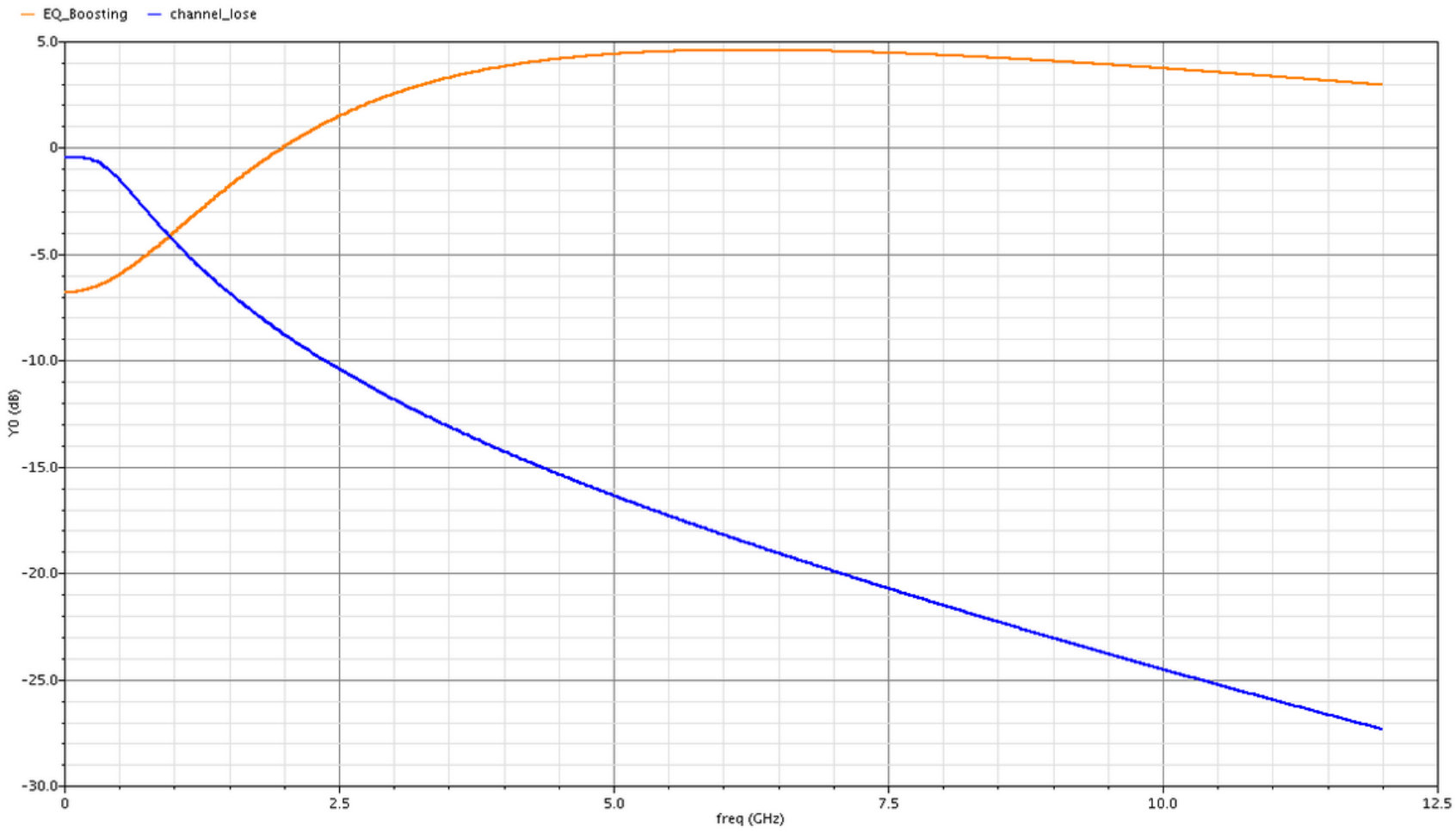


CTLE outputs

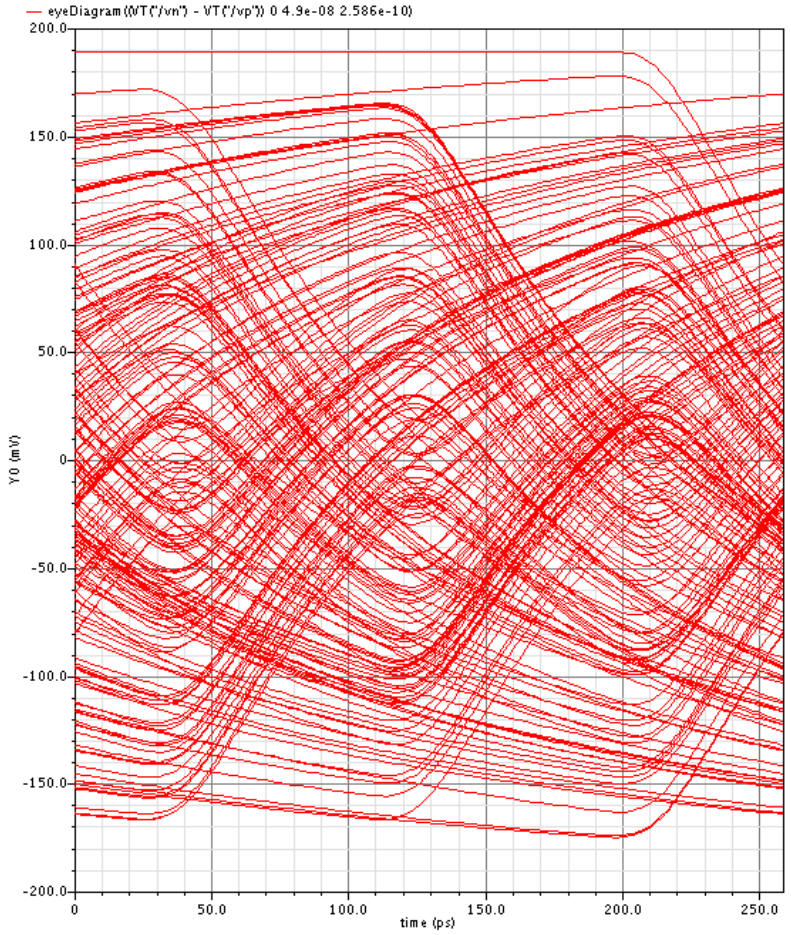
Channel (in)	Rs	Cs (fF)	Boost factor (dB)
4	430	125	3
6	645	104	4
8	950	94	5.5
10	1.1K	115	7
12	1.5K	94	8
14	1.8K	84	9.5
16	2.15K	94	11
20	2.8K	183	14

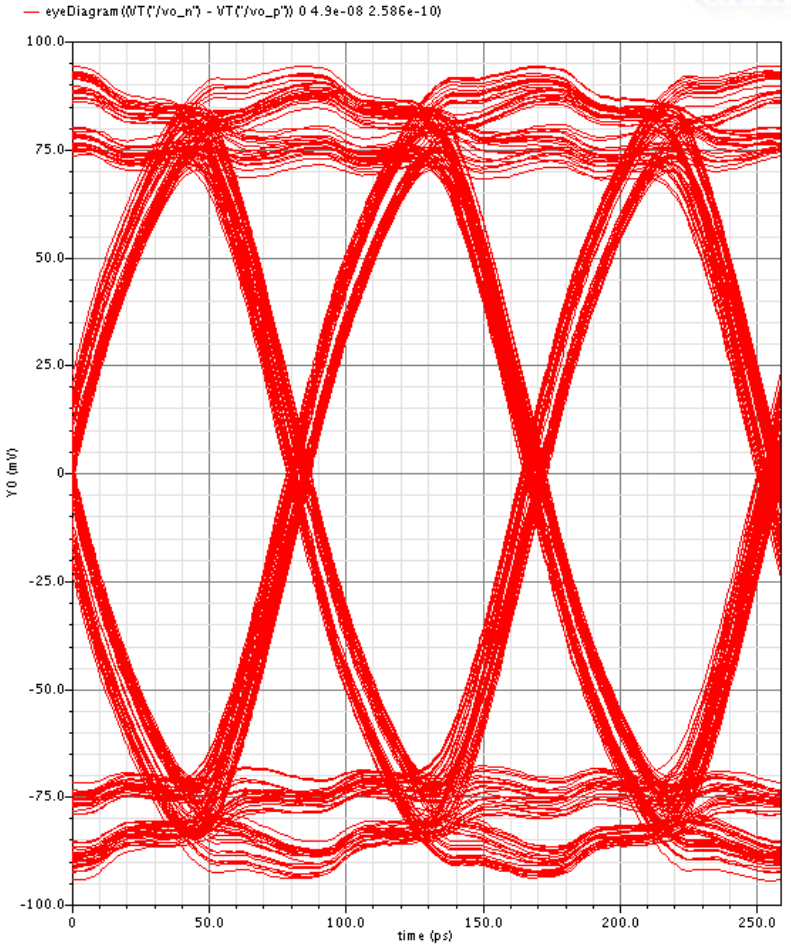


For 20-inch channel

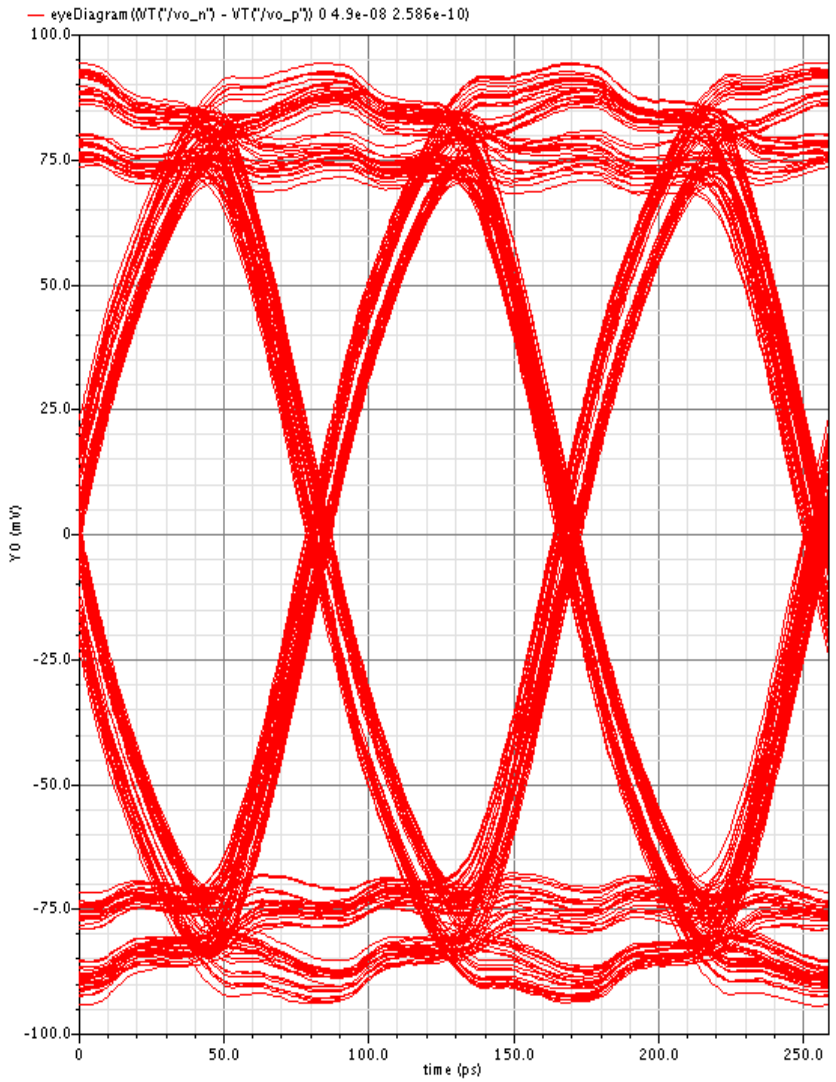


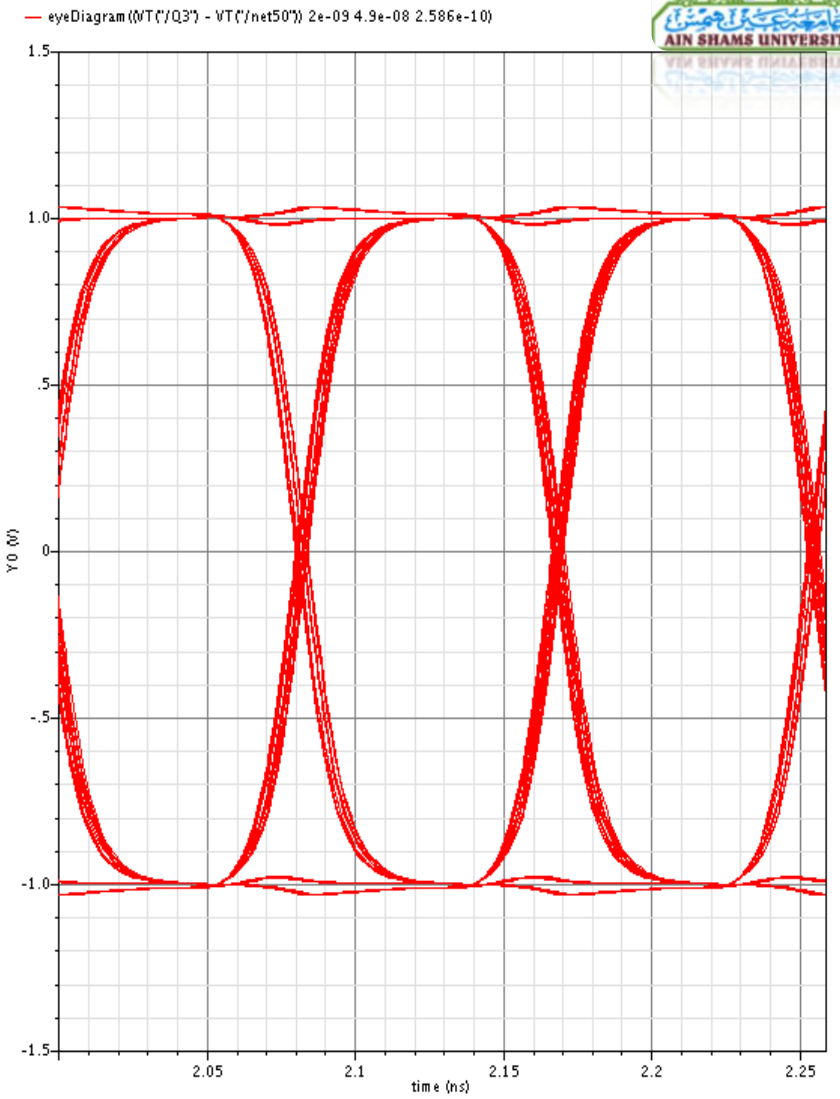
outputs


eyeDiagram (/VT("/vn") - VT("/vp")) 0 4.9e-08 2.586e-10
200.0
150.0
100.0
50.0
0
-50.0
-100.0
-150.0
-200.0
Y0 (mV)
0
50.0
100.0
150.0
200.0
250.0
time (ps)

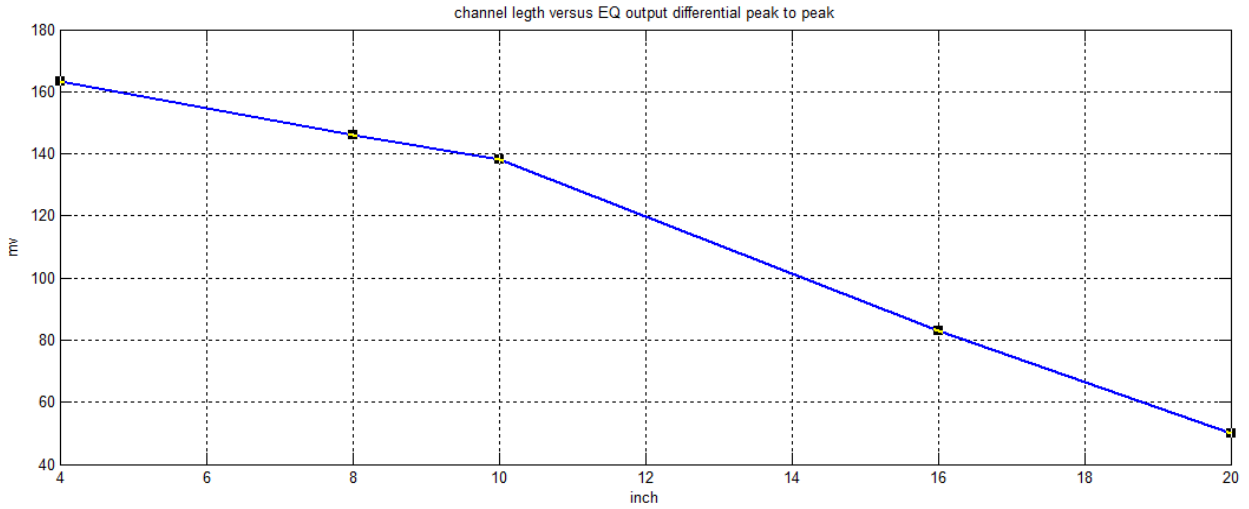

eyeDiagram (/VT("/vo_n") - VT("/vo_p")) 0 4.9e-08 2.586e-10
100.0
75.0
50.0
25.0
0
-25.0
-50.0
-75.0
-100.0
Y0 (mV)
0
50.0
100.0
150.0
200.0
250.0
time (ps)

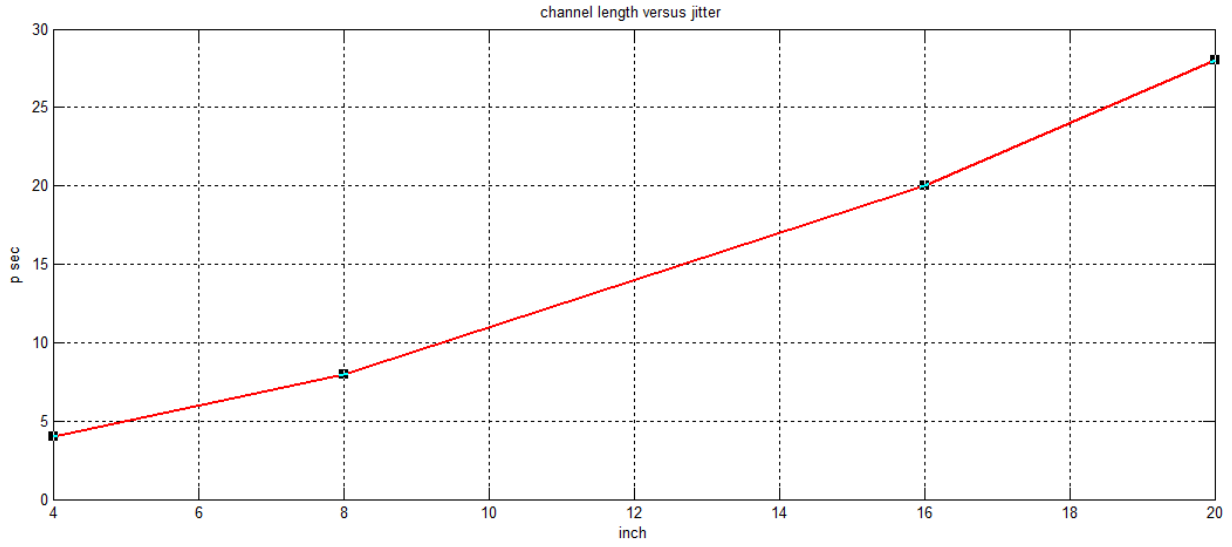
Outputs


eyeDiagram (VT("/vo_n") - VT("/vo_p")) 0 4.9e-08 2.586e-10)
100.0
75.0
50.0
25.0
0
-25.0
-50.0
-75.0
-100.0
Y0 (mV)
0
50.0
100.0
150.0
200.0
250.0
time (ps)


eyeDiagram (VT("/Q3") - VT("/net50")) 2e-09 4.9e-08 2.586e-10)
1.5
1.0
.5
0
-.5
-1.0
-1.5
Y0 (V)
2.05
2.1
2.15
2.2
2.25
time (ns)

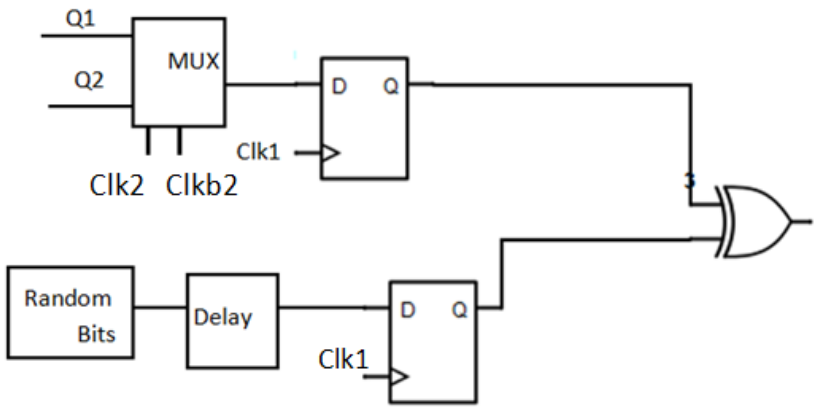
Outputs


channel legth versus EQ output differential peak to peak
mv
inch
180
160
140
120
100
80
60
40
4
6
8
10
12
14
16
18
20

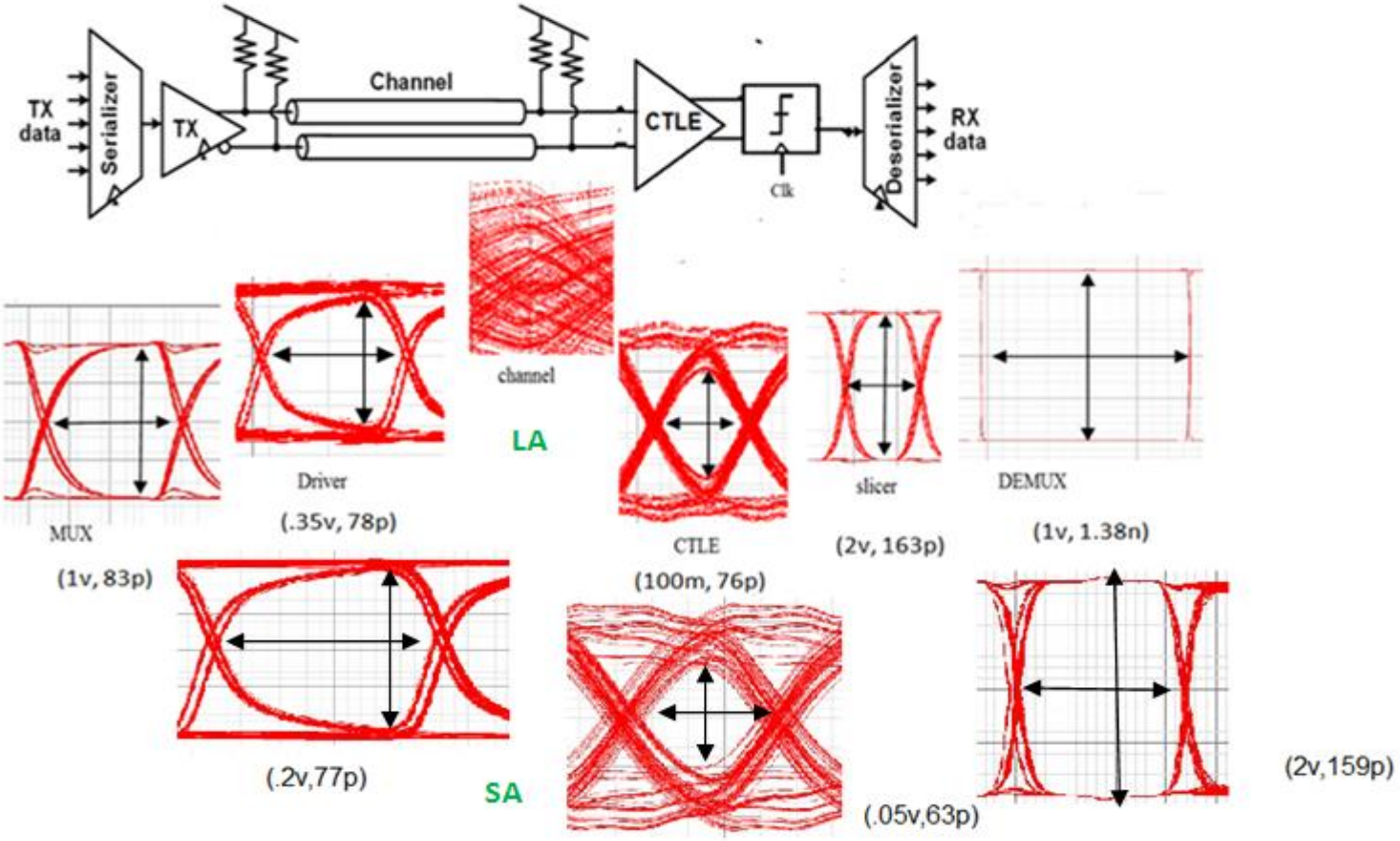

channel length versus jitter
p sec
inch
30
25
20
15
10
5
0
4
6
8
10
12
14
16
18
20

Verification for correct data from slice

- When composing EQ with slicer
- With 6psec clock jitter, We got 0.5UI margin for clock and data to be delayed .



When composing transmitter and recei circuits



Clock and Data Recovery (CDR)

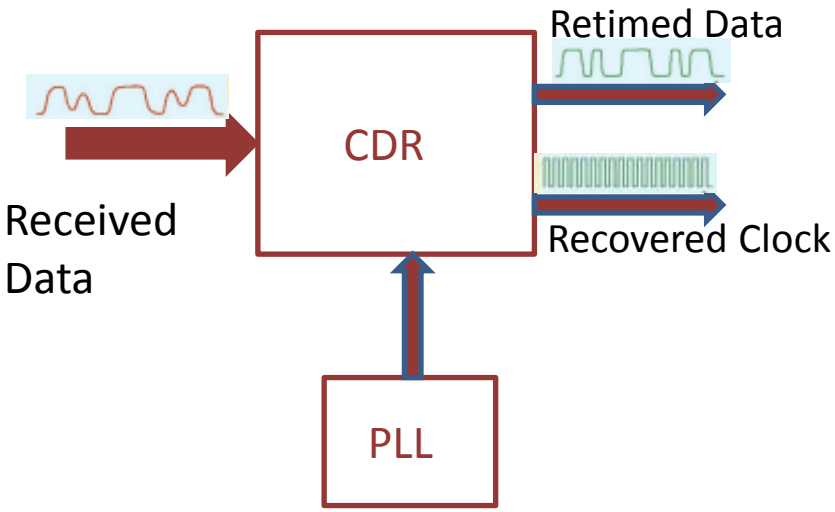
Presented by : Eman Omar

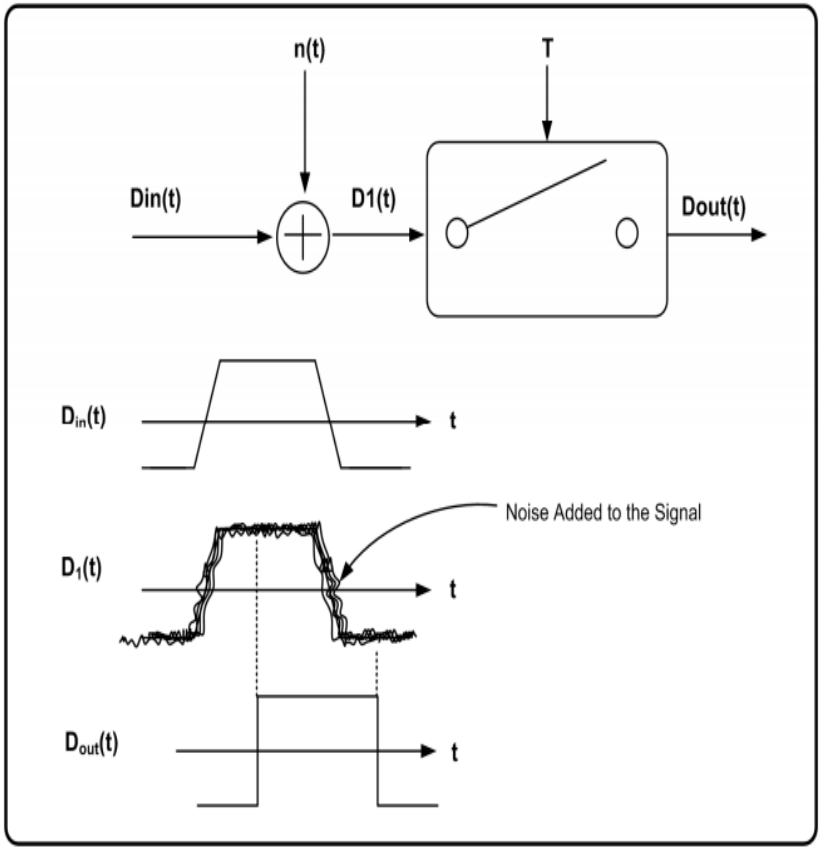
Outlines

- CDR
- CDR Topologies
- Selected Topology

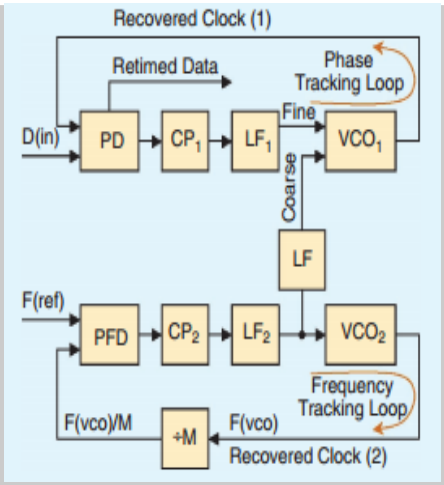
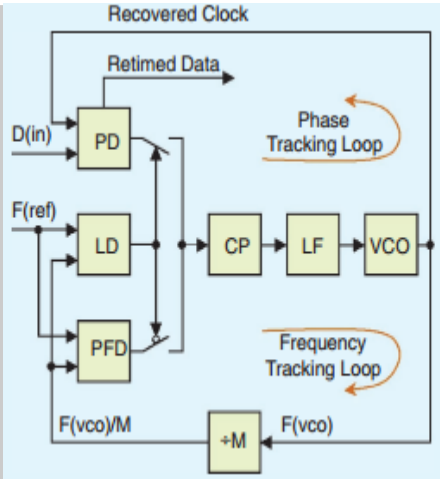
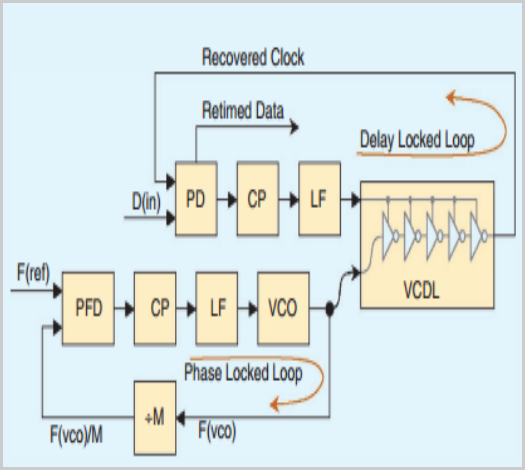
CDR

- Function of CDR
- Requirements of CDR



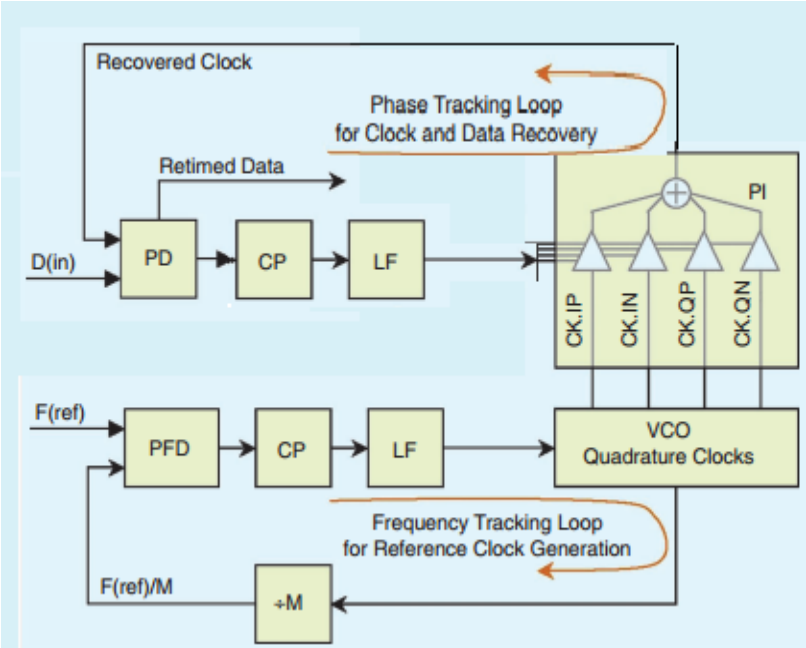


CDR Topologies

	PLL based CDR 1	PLL based CDR 2	DLL based CDR
Block diagram			
Advantages	1-input jitter rejection 2-input frequency tracking	Avoids the problem of multiple VCO pulling	Low power , No jitter accumulation , More stable
Disadvantages	1-jitter peaking 2-large loop filter Area	Switching of LD disturbs VCO's control signal & make freq. offset.	Limited phase capturing range s0 can't handle any frequency offset bet. Tx & Rx.

Selected Topology
PI based CDR

- Solves the Problem of limited capturing range of DLL based CDR
- Half rate topology
- Analog PI



Advantages:

1-Multichannel Share Input Clocks.

2-high resolution so less jitter.

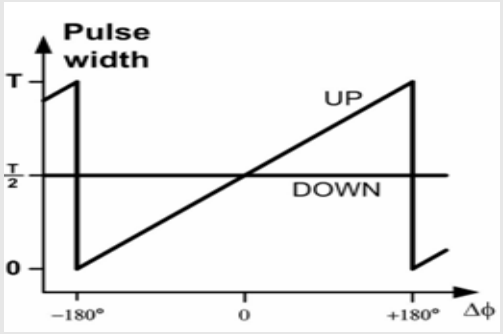
Phase Detector and Charge Pump
(PD and CP)

Presented by : Eman Omar

Outlines

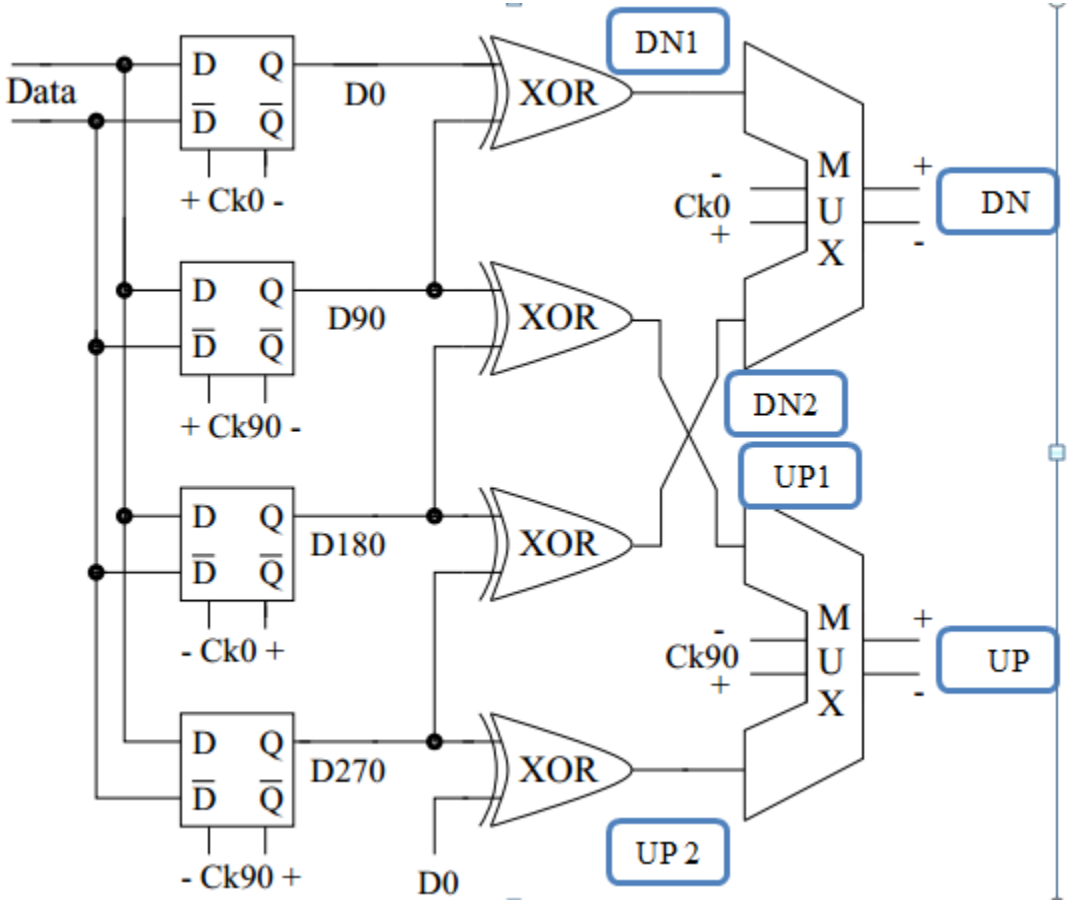
- Phase Detector
- Selected Topology
- Slicer
- XOR
- Multiplexer
- PD Results
- Charge Pump
- Selected Topology
- Simulation Results

Phase Detector
Linear and Binary PD

	Linear PD	Binary PD
Output signals	Provide both phase and magnitude of the phase difference	Provide only the phase of the phase difference
Advantages	Small output jitter	1-Less sensitive to data patterns 2-Power efficient than linear at high speed applications
Disadvantages	Non linearity for non uniform data patterns	High output jitter
Gain		

Selected Topology
Half Rate Alexander PD

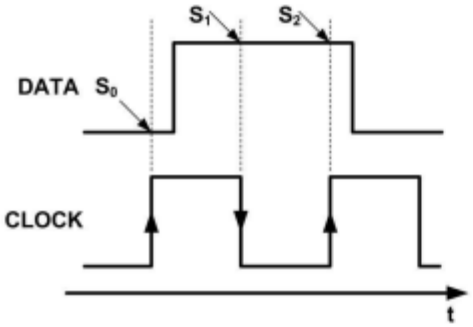
- Uses I & Q clock phases.
- Has two data slicers & two edge slicers.



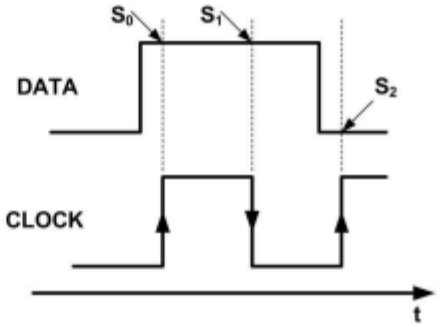
Half Rate Alexander PD (cont.)

Points of Comparison	BGR with PTAT Current Output	BGR with Sub 1-V operation
VREF	Can't be controlled always ~1.205V	Designed to be 1V "adjustable"
	Varies With Temp 2mV	Varies With Temp 2mV
IREF	PTAT current increases with temperature	Constant current , BUT it PTAT due to no ideal Resistors
Stability	Good stability	
PSR	Depending on the design of the OTA	
	Bad	Good

$DN_2 = D_{180} + D_{270}$	$DN_1 = D_0 + D_{90}$
$UP_2 = D_{270} + D_0$	$UP_1 = D_{90} + D_{180}$



Clock late

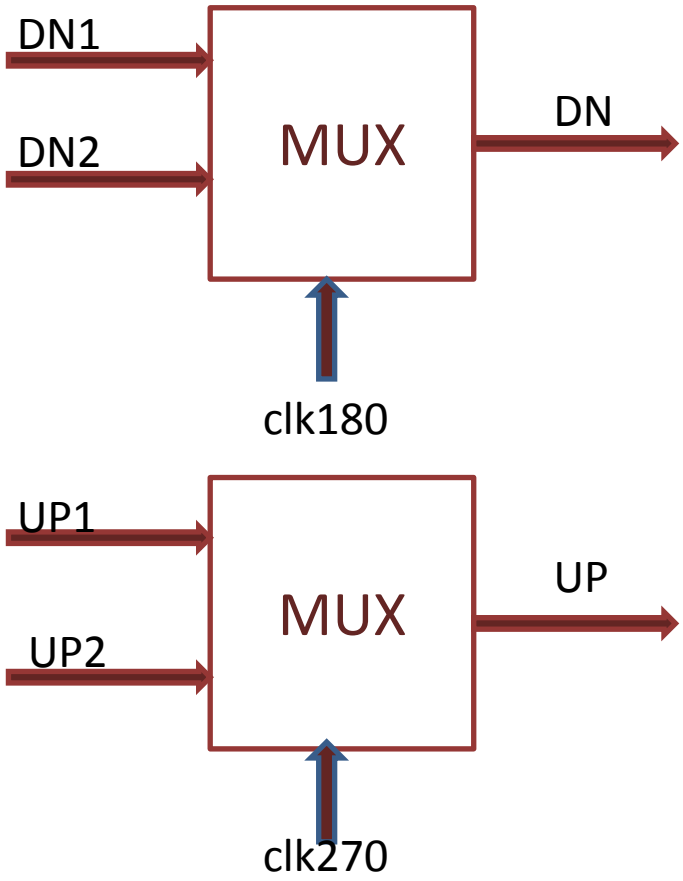


Clock early

90 → 360	90 → 360
270→ 360+180	270→ 360+180
180 → 360 +90	180 → 360 +90
0 → 270	0 → 270

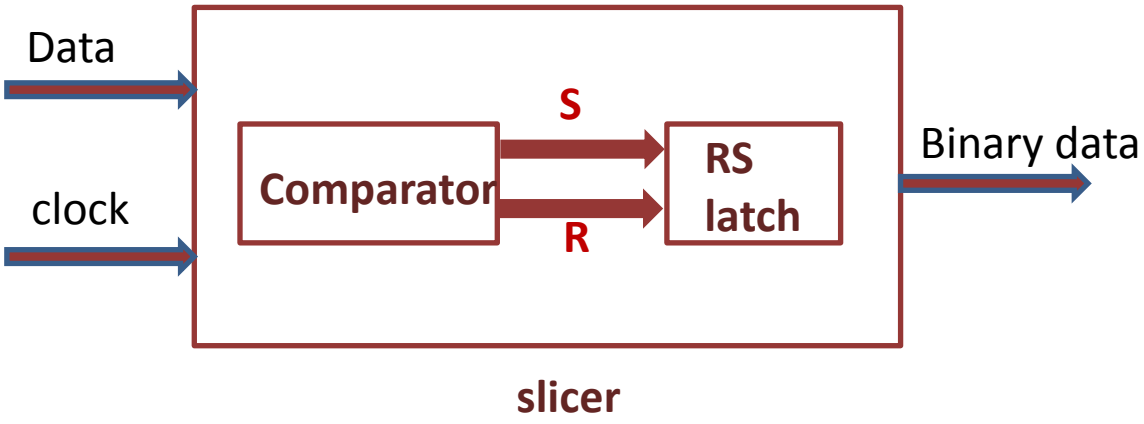
Half Rate Alexander PD (cont.)

Mux clock phases to eliminate the delay from slicer:



Slicer

Slicer is a dynamic comparator followed by an RS latch



Slicer (cont.)

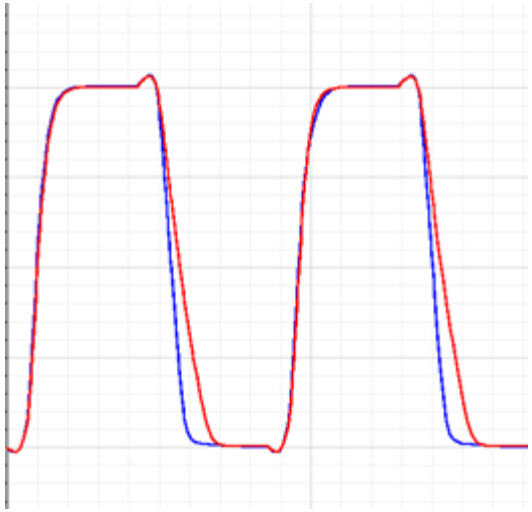
Comparator:

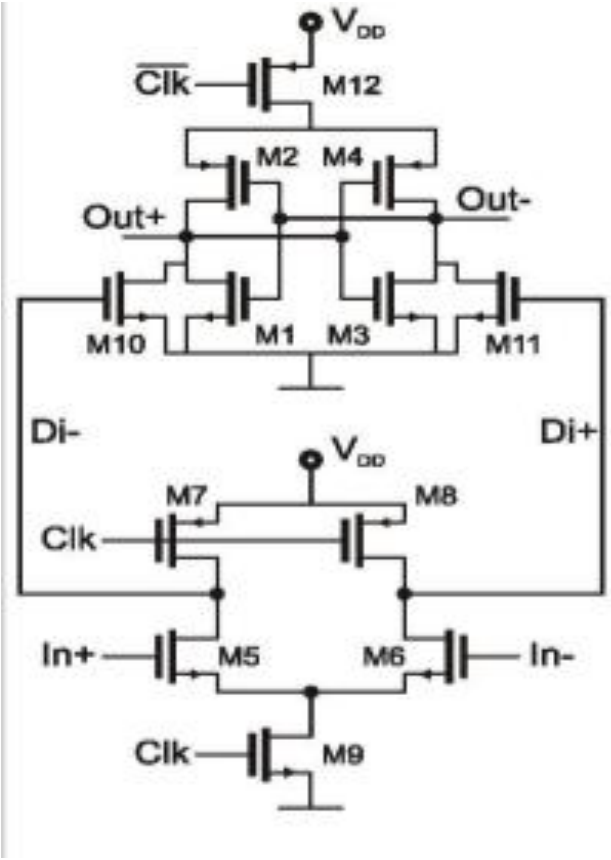
	Strong Arm	Double tail
Advantages	1- lower power consumption.	1- requires small voltage headroom. 2-separation of the input tail current and the latch tail current.
Disadvantages	1- requires large voltage headroom. 2-shows very strong dependency on speed with different common mode input voltages. 3-tradeoff between the latch's speed and the time the gain stage remain in saturation.	1-Higher power consumption. 2-requires clock and clock bar.

Slicer (cont.)
Double Tail Voltage SA

1- Operation .

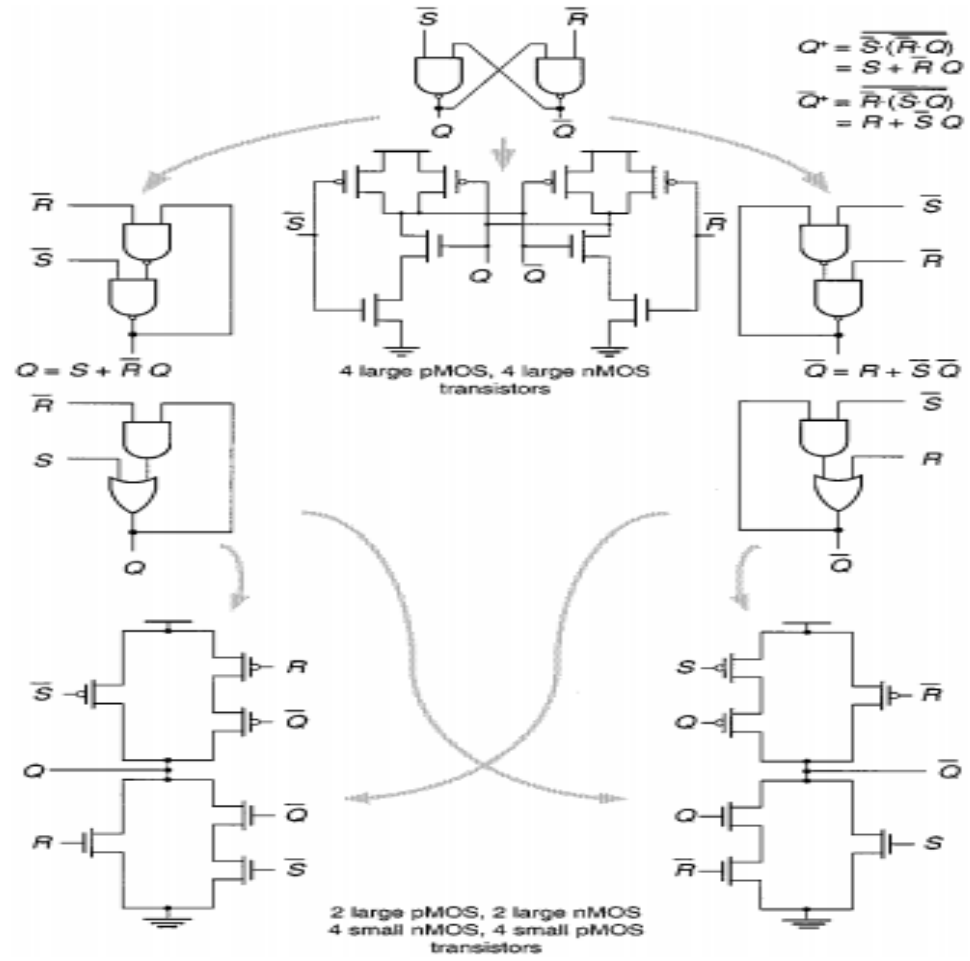
2- Sizing Consideration.



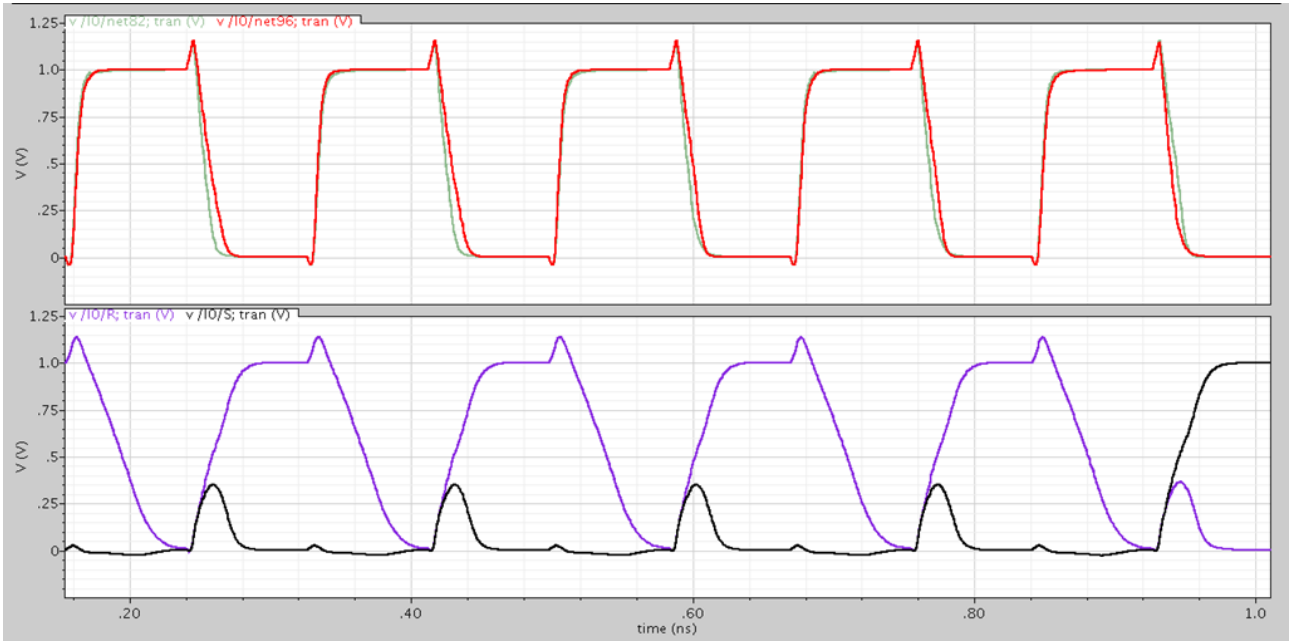


Slicer (cont.)
RS Latch

$$Q^+ = S + \overline{R}.Q$$
$$\overline{Q}^+ = R + \overline{S}.\overline{Q}$$



Slicer (cont.)
Results:



Transient Simulation : D_i^+ , D_i^- , R ,S

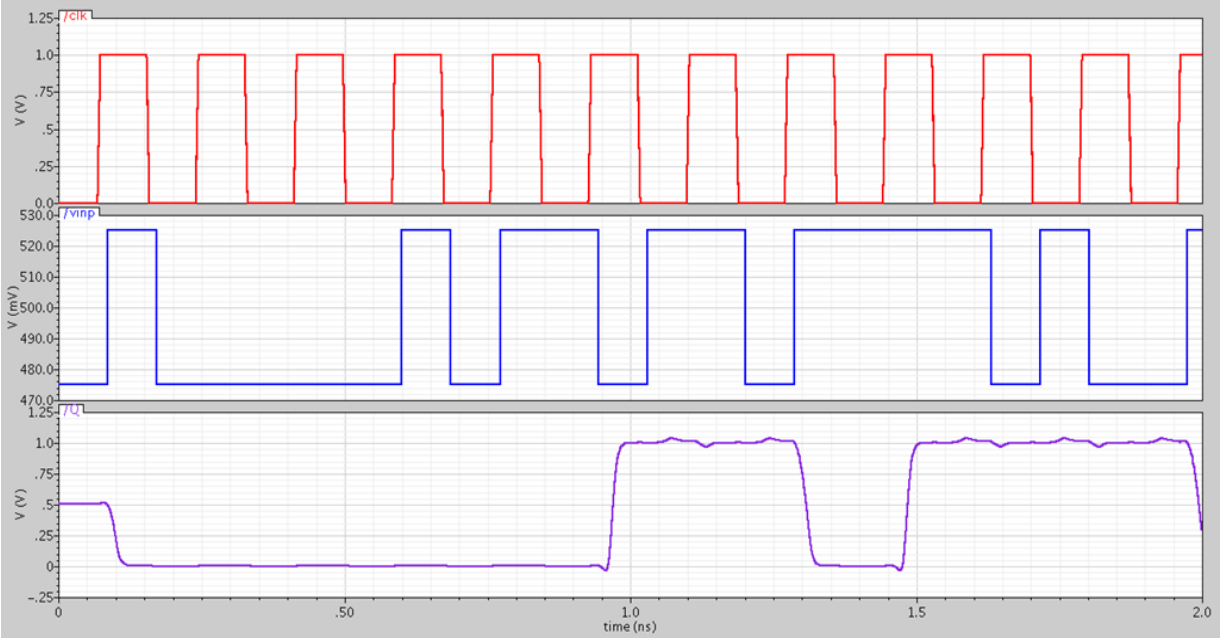
Slicer (cont.)
Results (cont.)

$V_{inpp} = 50\,mv$

Delay = 40.775 psec

Power consumption = 94.8 uw

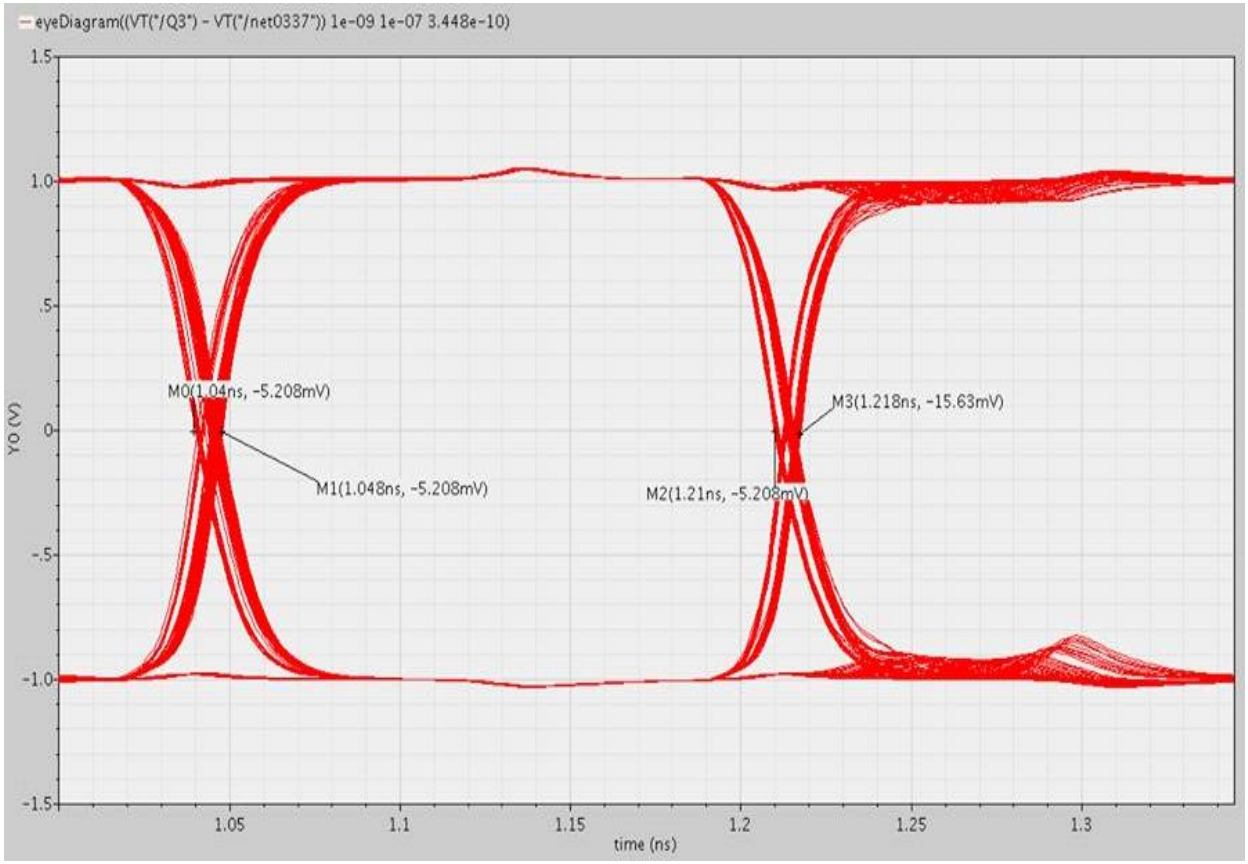
Sensitivity = 4 mv



Transient Simulation: clk , V_{inpp},Q

Slicer (cont.)
Results (cont.)

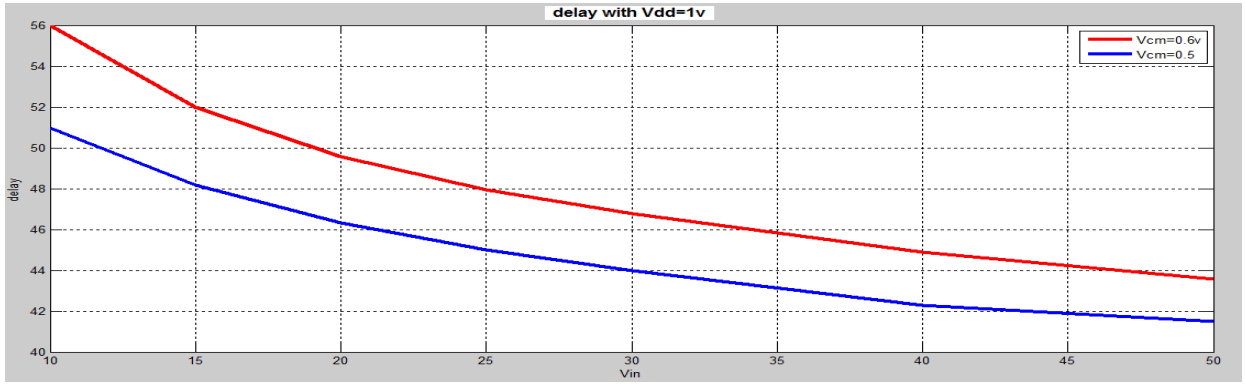
- Eye opening = 162 psec



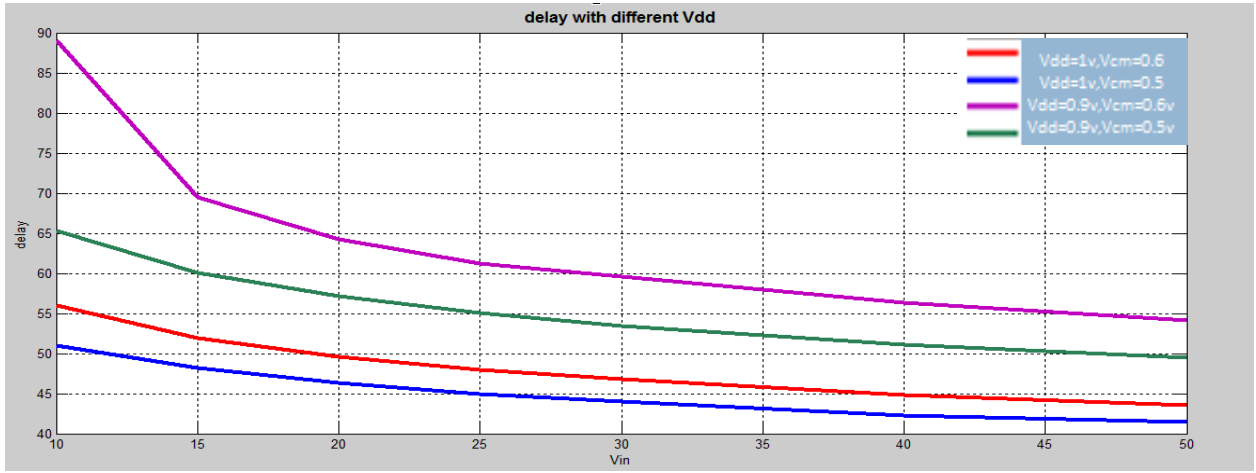
Eye Diagram of slicer output

Slicer (cont.)
Results (cont.)

Sweeping ΔVin for the same vdd = 1v with diff V_{cm}



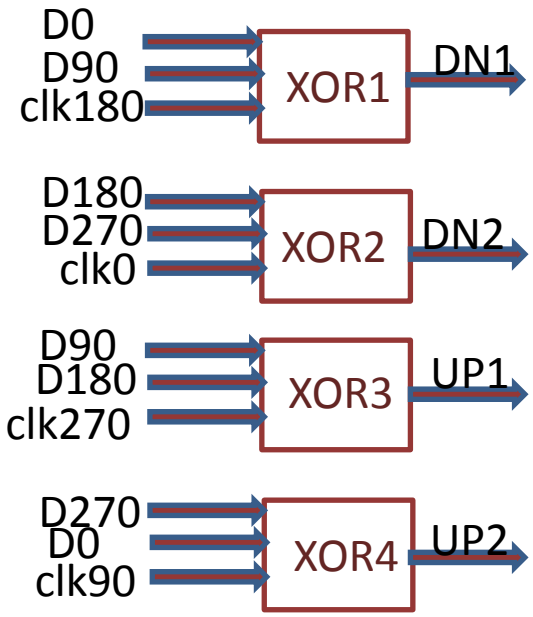
Delay for different vdd:

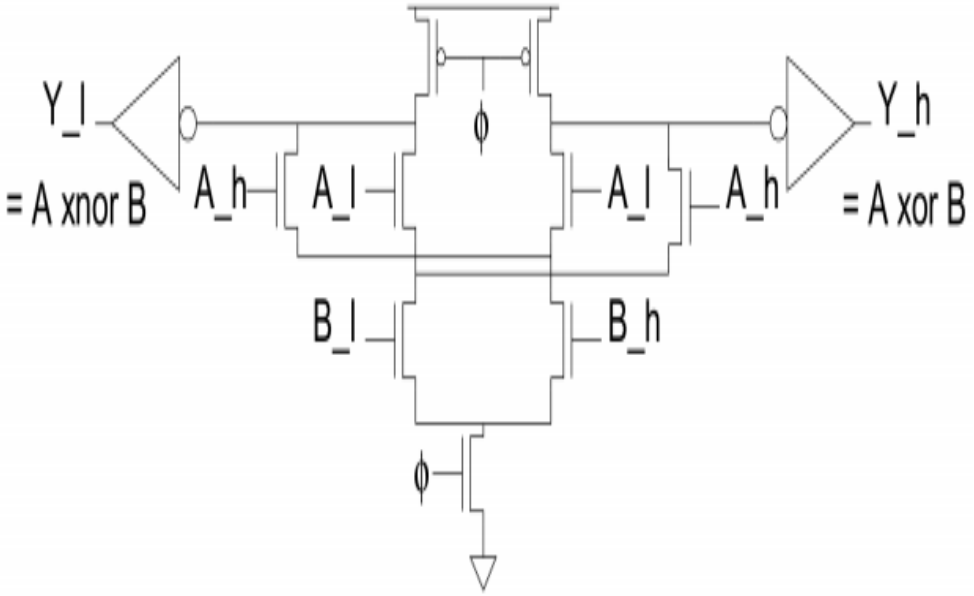


XOR

Dynamic XOR

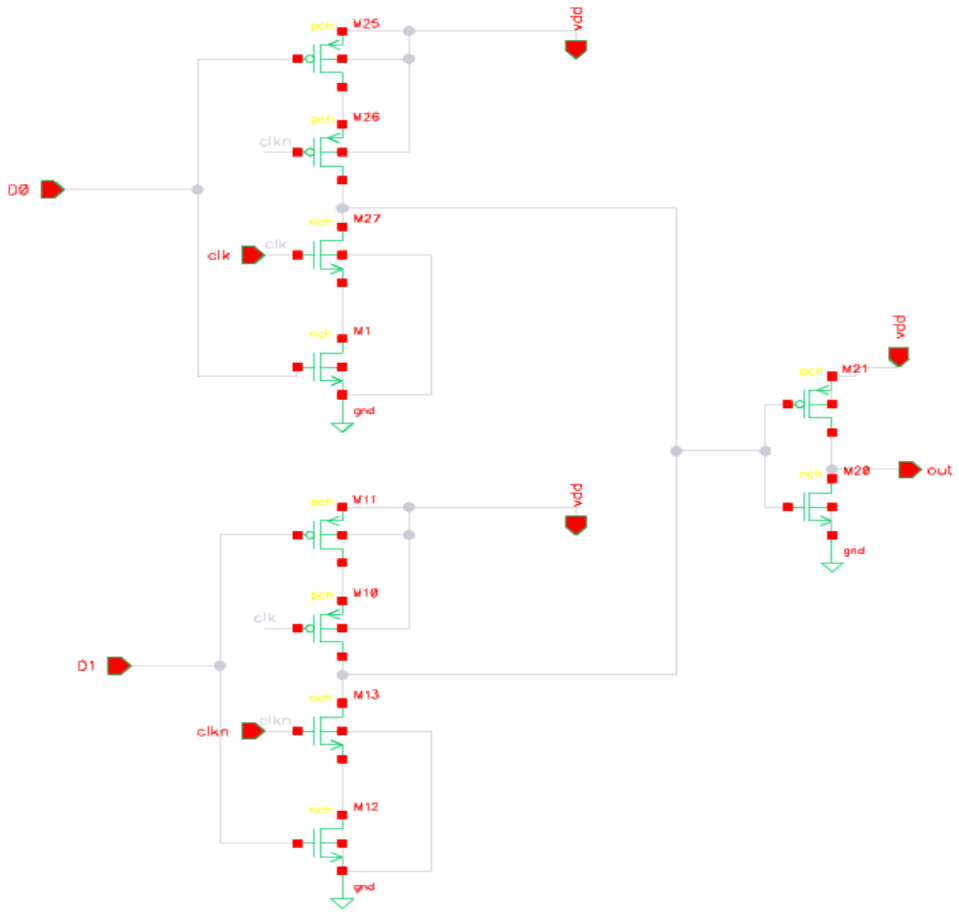
- **Supports the 5GHZ speed.**
- **It's disadvantage to the PD system .**





Multiplexer

Multiplexer Topology:



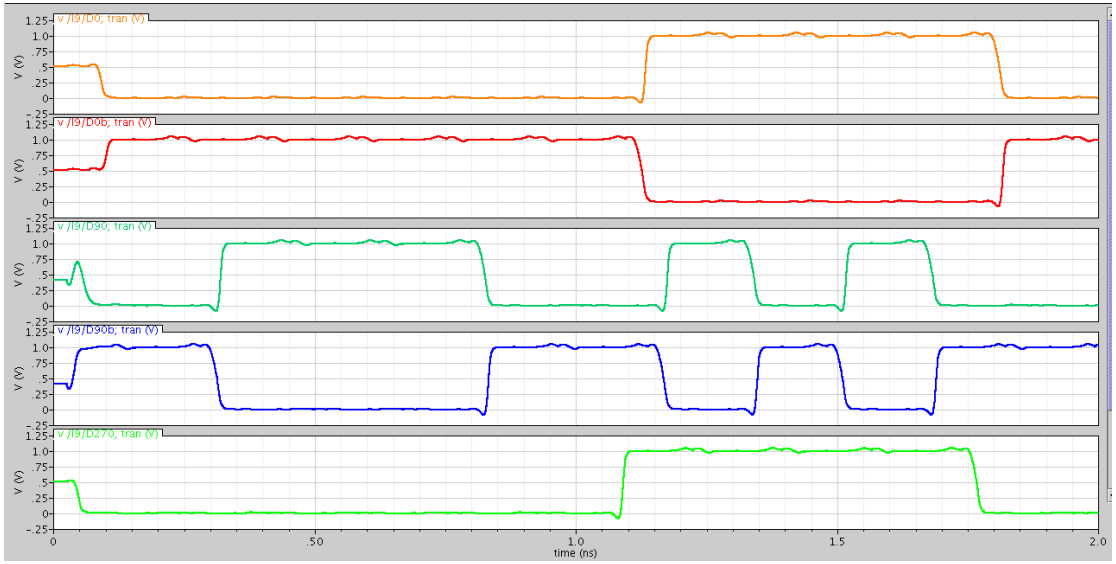
PD Results

Total power of PD = 604.159 uw.

Example:

The clock is late by 30 psec.

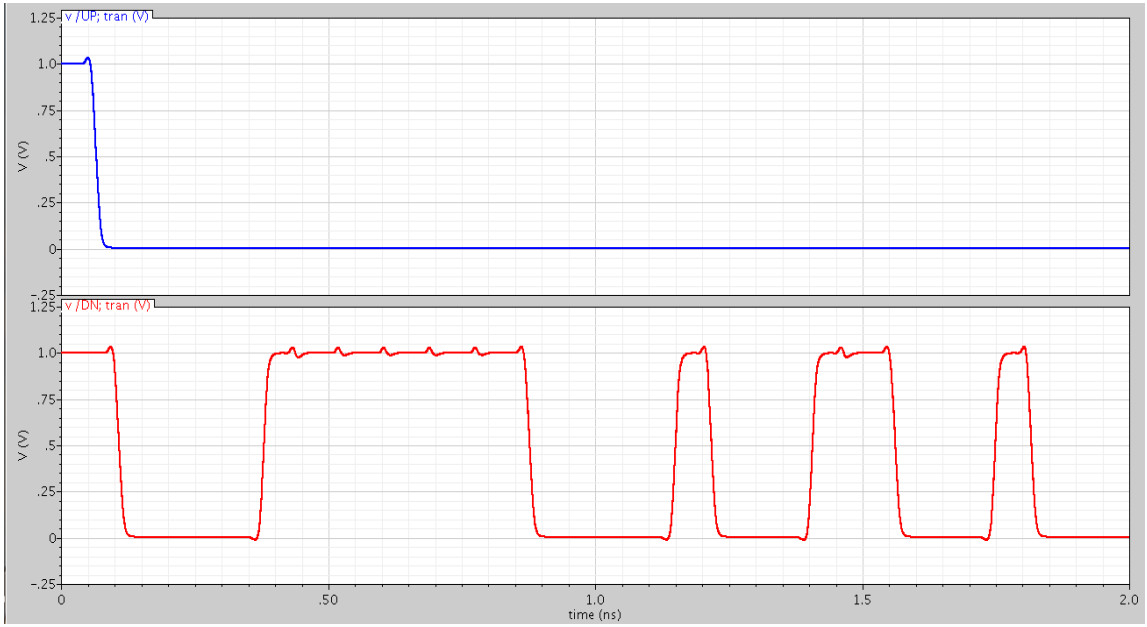
1- slicer output:



D0 , D90 ,D180,D270

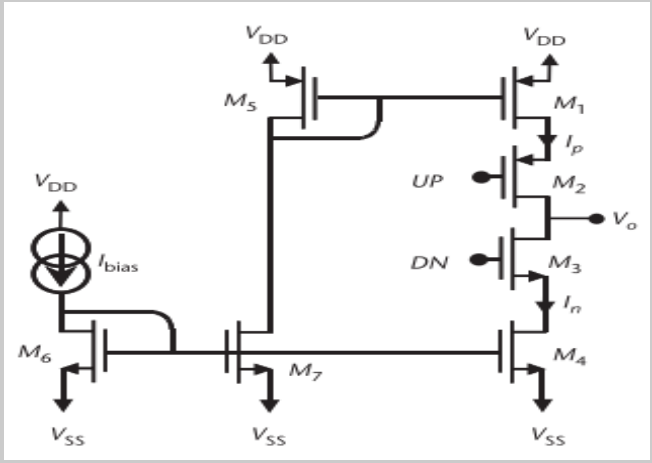
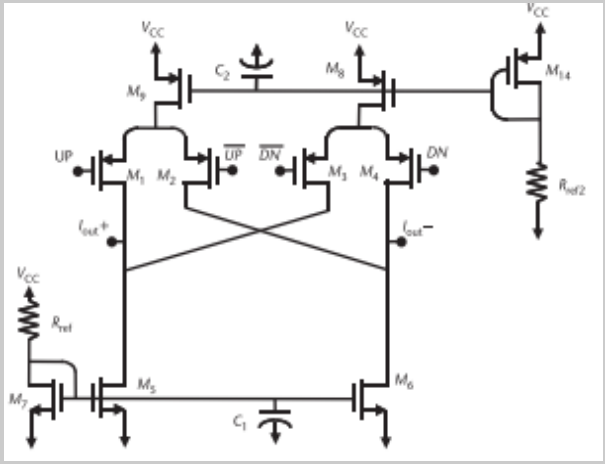
PD Results (cont.)

2-output of Mux :



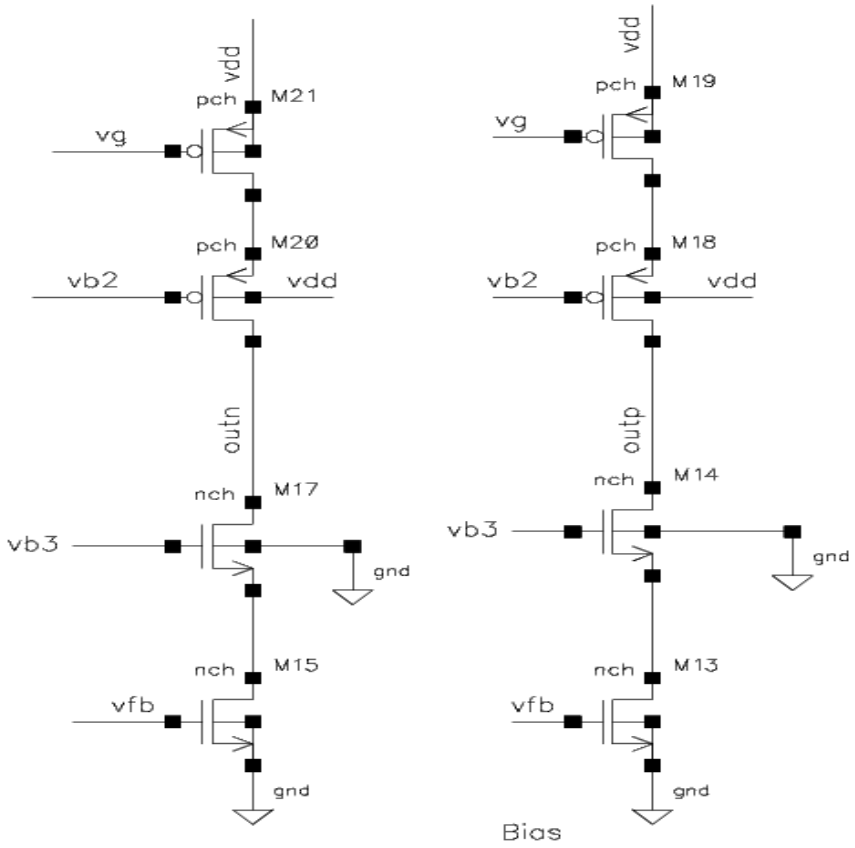
UP , DN

Charge Pump

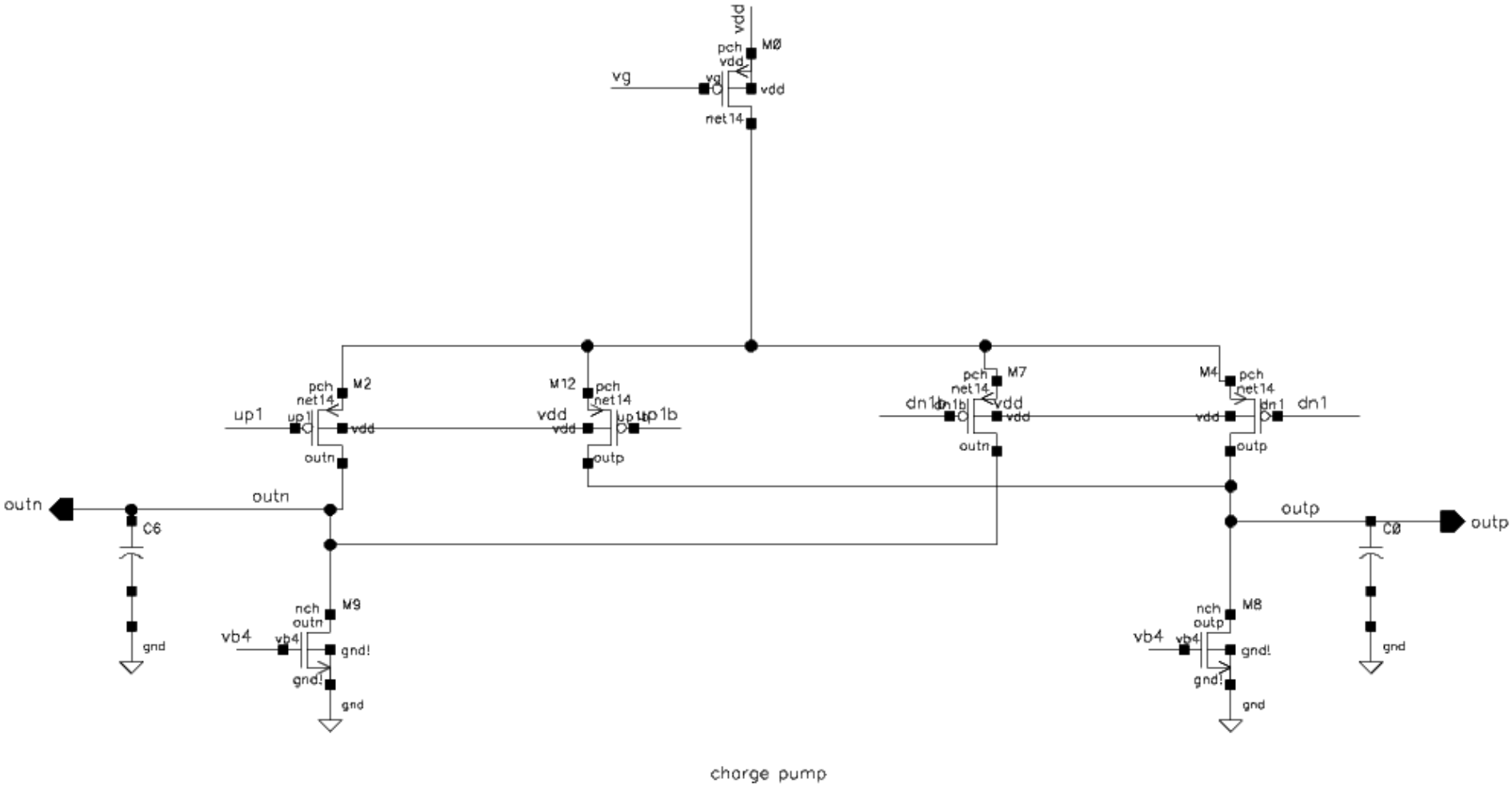
	Single ended	Differential
		
advantages	1- Simple to implement. 2- Low power and Area.	1- Use NMOS switches only or PMOS only. 2-better immunity to supply & substrate noise. 3-double the compliance range.
disadvantages	1-High phase noise. 2- Current mismatches which lower the compliance range.	1- Need of common-mode feedback circuitry . 2- More power dissipation due to the constant current biasing.

Selected Topology

- Selected Filter
- Biasing the output common mode voltage
- Uses a CMFB circuit.



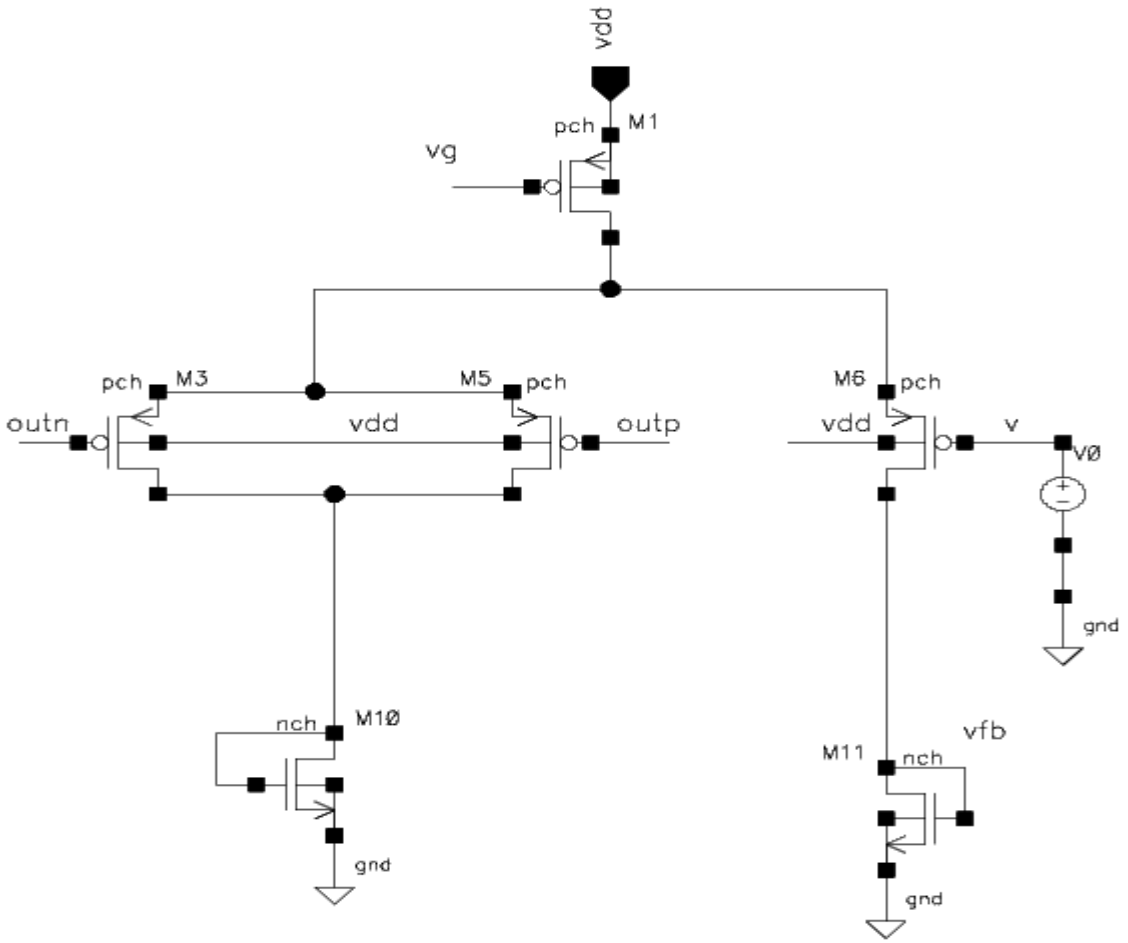
Selected Topology



charge pump

Selected Topology (cont.)

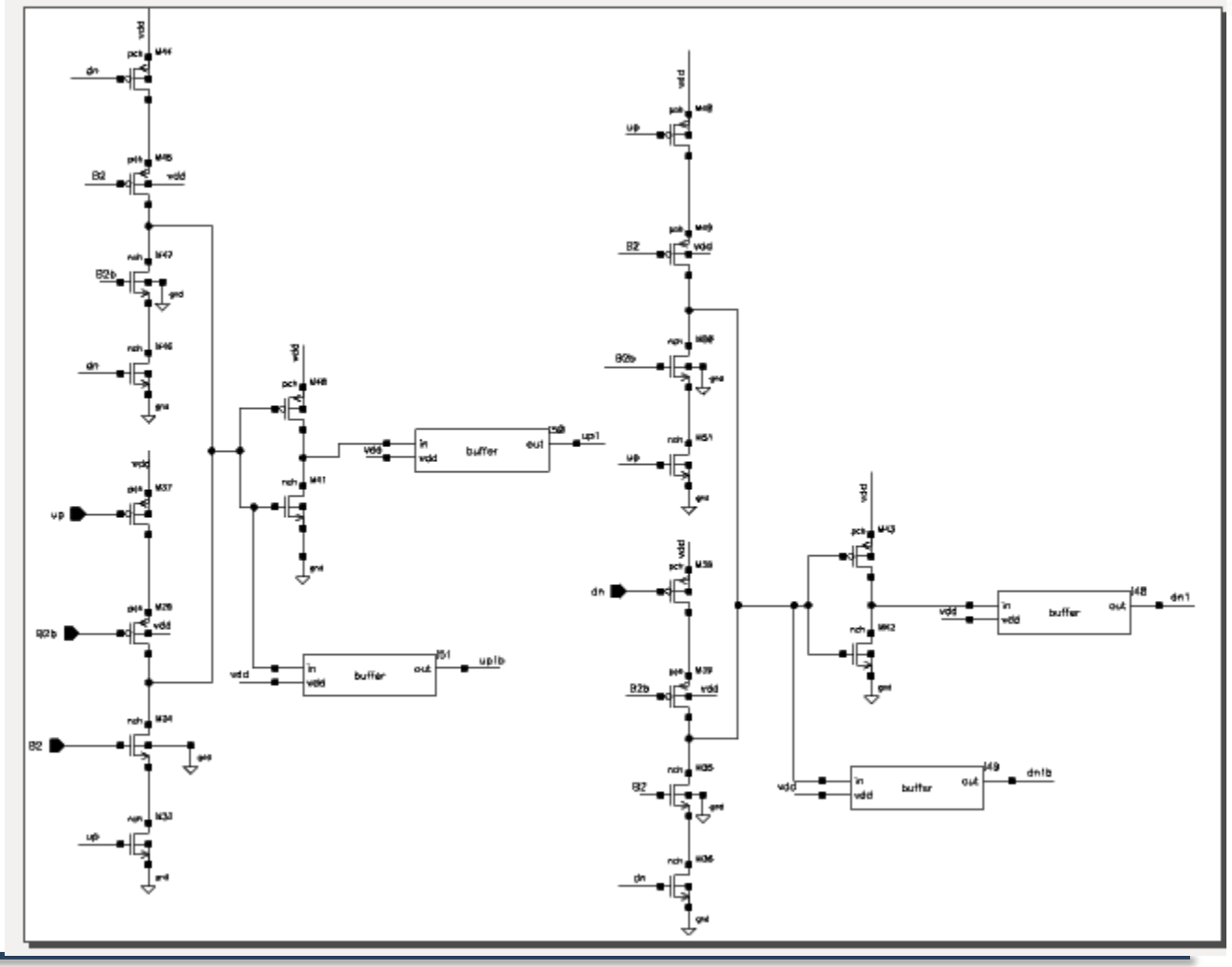
Common mode feedback circuit:



CMFB

Selected Topology (cont.)

Switch circuit:



Simulation Results

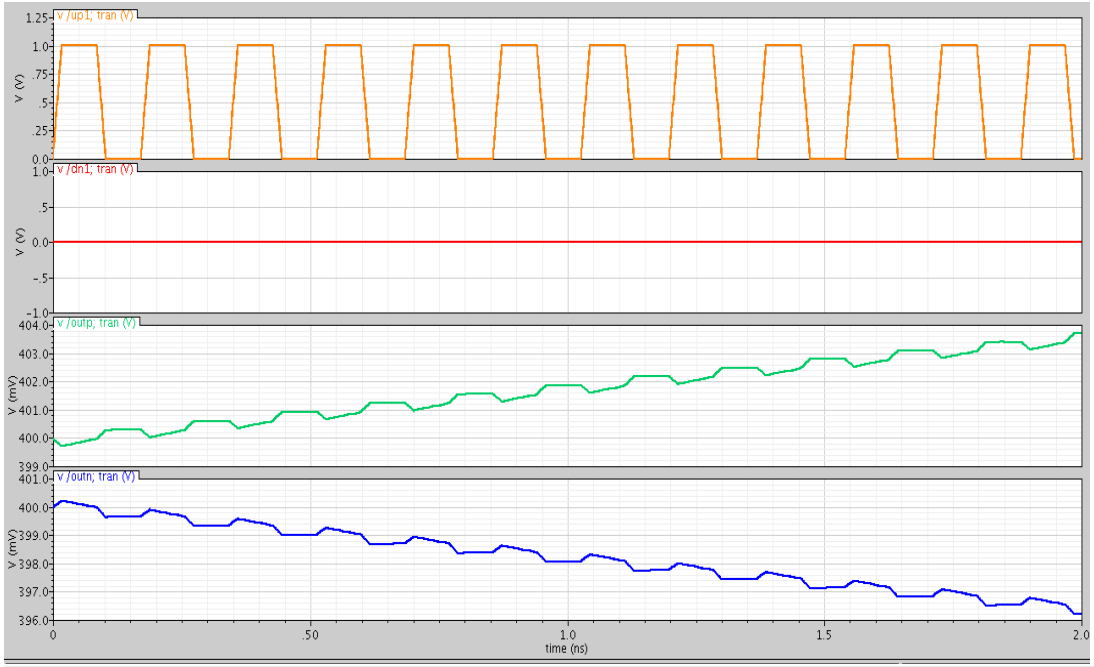
→Step size of the control voltage = 0.2896 mv

As $\Delta v = \frac{\Delta t * I}{C} = \frac{85.851psec * 50.6uA}{15pF} = 0.2869mv$

→This is equivalent to 0.17 degree

→So the PI resolution become 531 point per quad

→Power consumption =1.4m

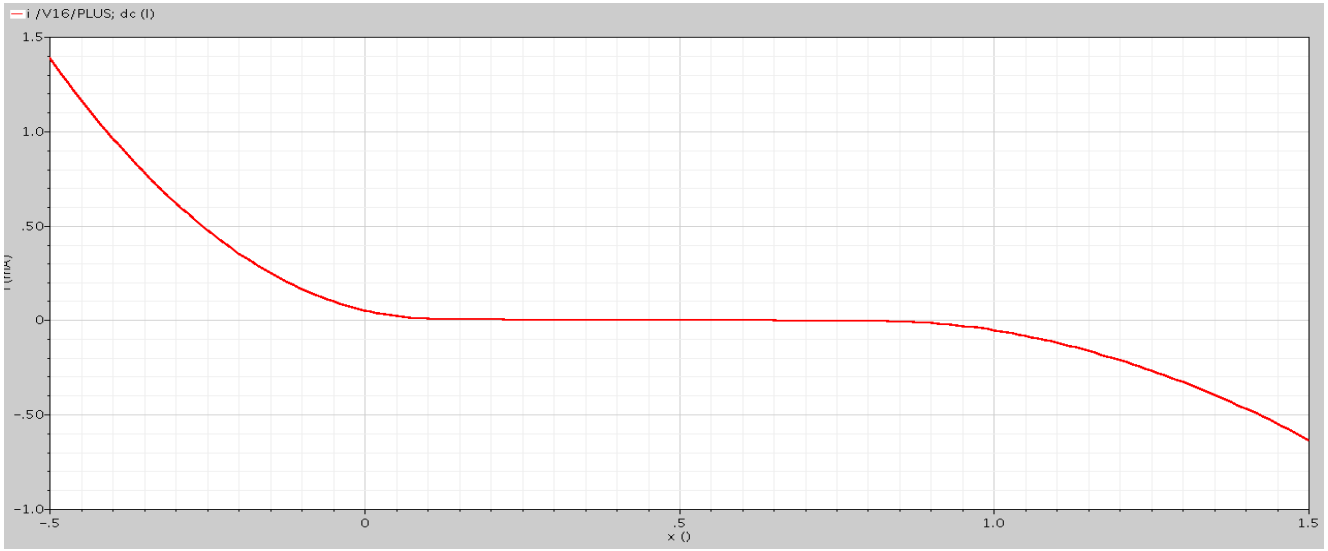


CP transient output

Simulation Results (cont.)

Compliance Range:

1-The compliance range of the charge pump itself without the biasing were from 118.5mv to 791.2 mv

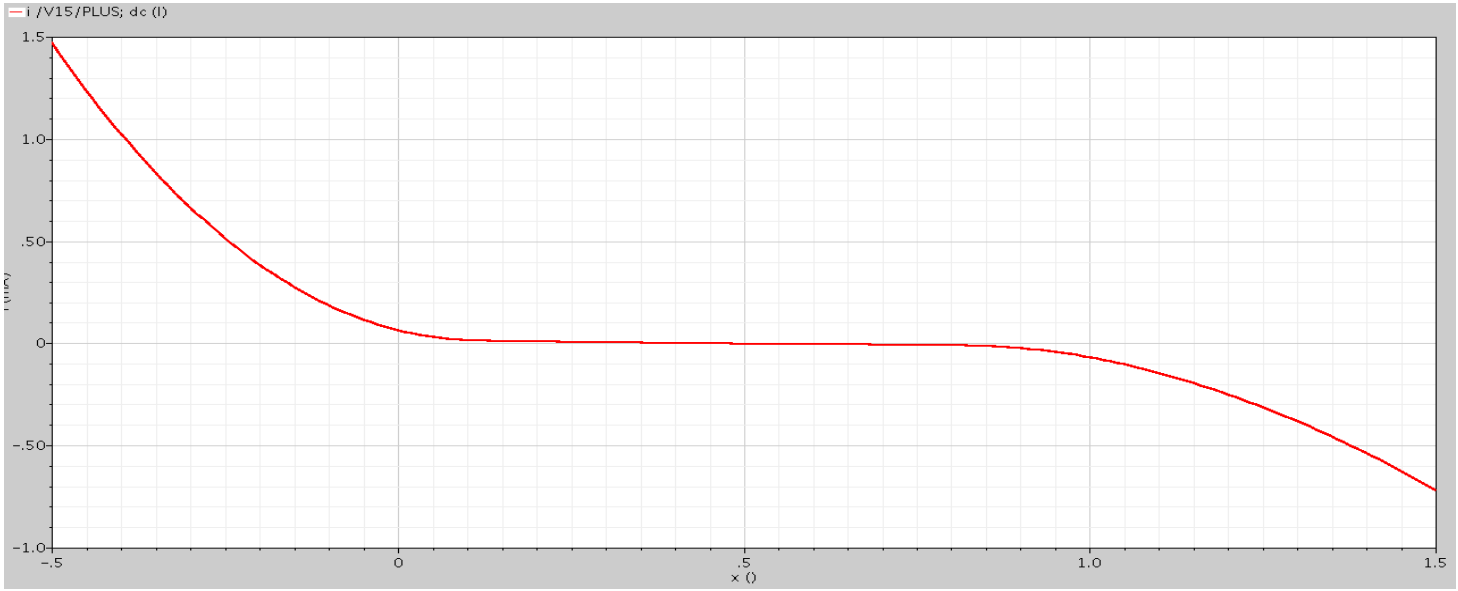


Compliance range of the CP itself

Simulation Results (cont.)

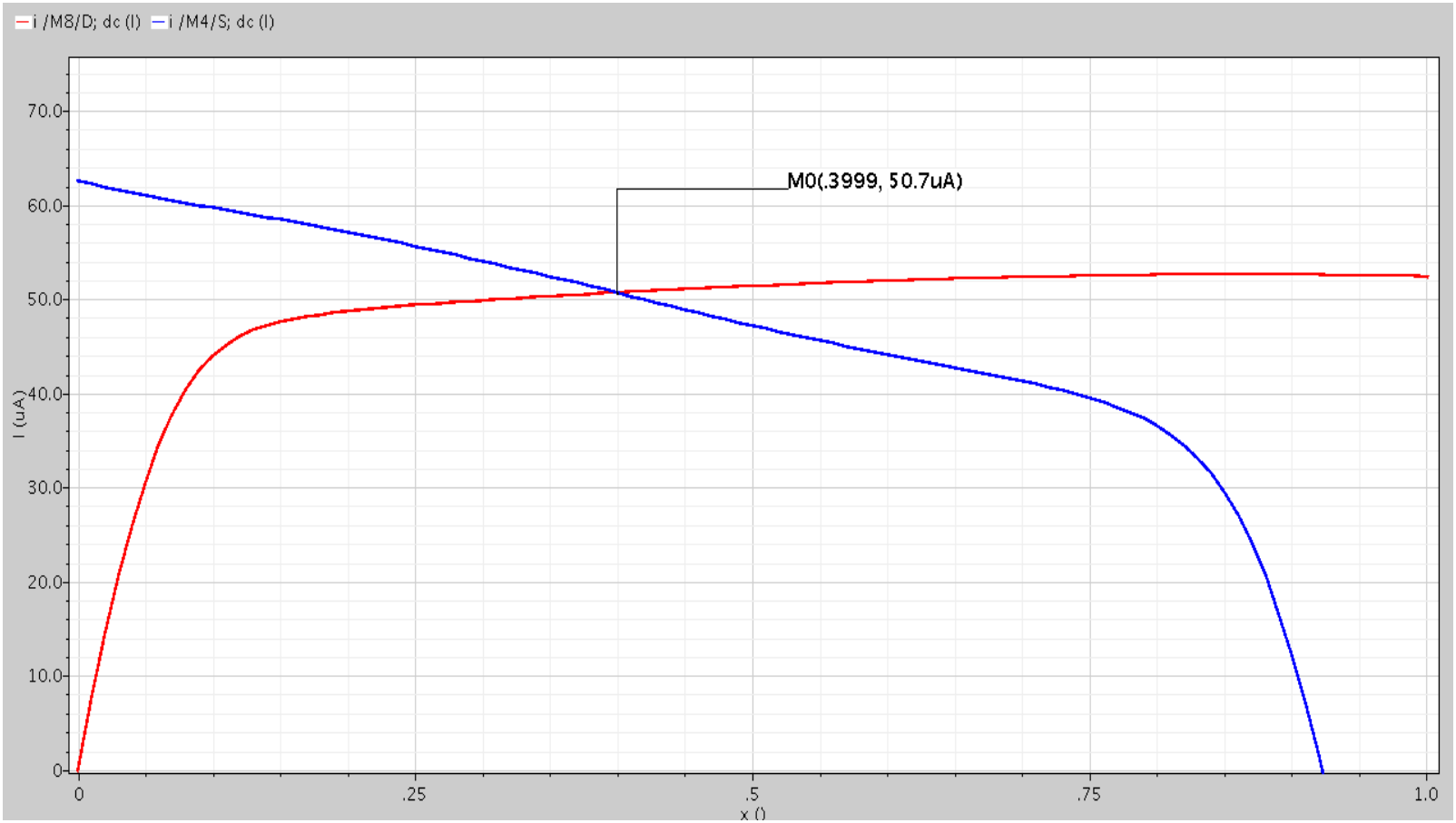
2-After adding the bias current sources as they are cascaded the range decreased to from 271.1mv to 573m

→As the PI works from 300 mv to 500 mv , the range was accepted.

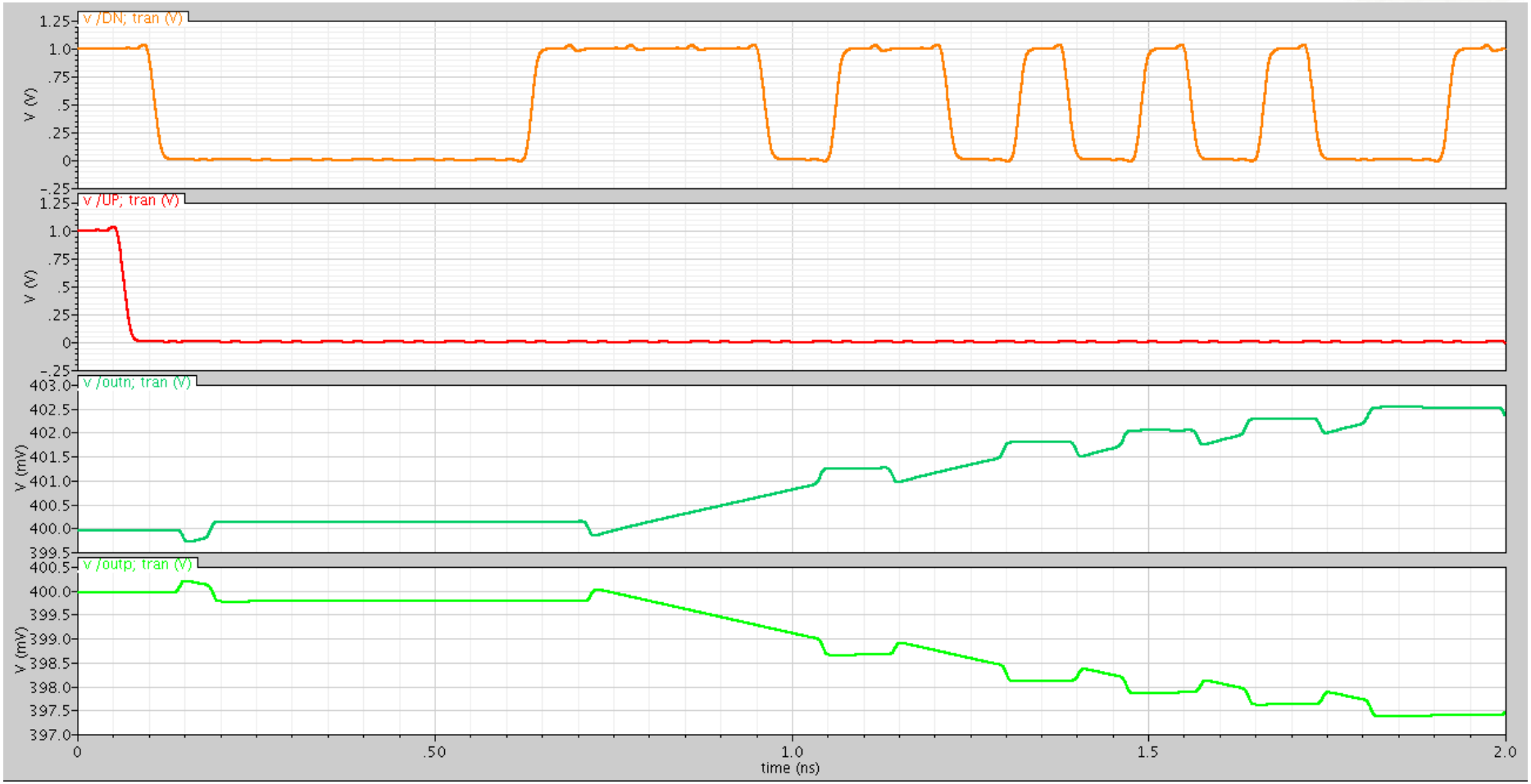


Compliance range of the CP with bias current sources

Simulation Results (cont.)



Simulation of PD + CP



Analog Phase Interpolator (PI)

Presented by : Samar Magdy

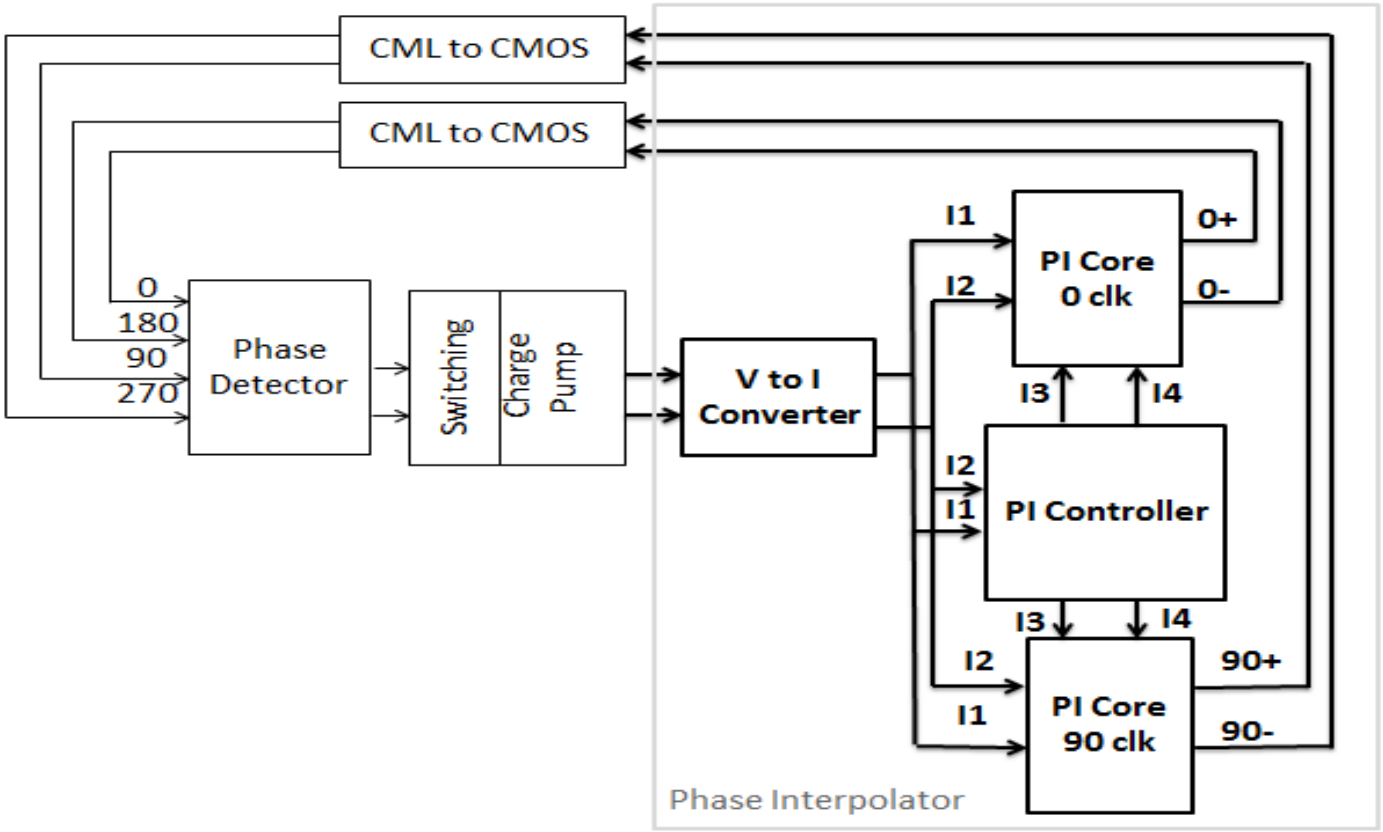
Outlines

- Introduction to Analog PI.
- PI in System Architecture.
- Concept and Circuit Review.
- Final Results.
- CDR Loop Locking.
- CDR Power Consumption.

Introduction to Analog PI

- Digital PI Drawbacks.
  - Degrades CDR Jitter Performance.
  - Speed Limitations.
  - Power Dissipation.
- Analog Phase Controller Advantage.

PI in System Architecture



Concept & Circuits Review

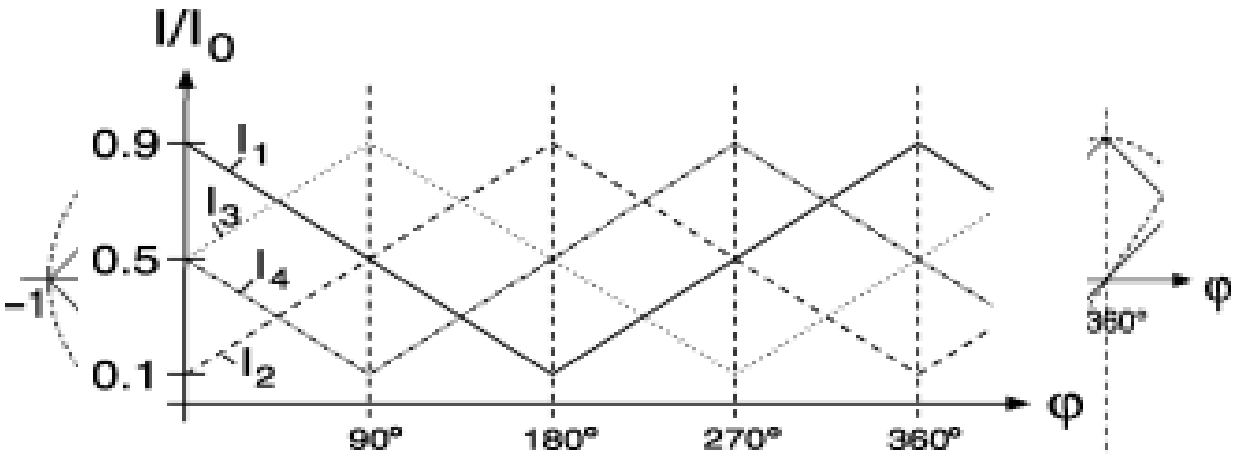
- Interpolation Concept.
- Currents Generation Concept.
  - Clocks **0°** and **90°** PI Cores.
  - V-to-I Converter.
  - PI Controller.
  - Schmitt Trigger Comparators.
  - Spikes Suppression and Voltage Clamping

Interpolation Concept

Sweeping Δ *Vin* for the same vdd = 1v with diff V_{cm}

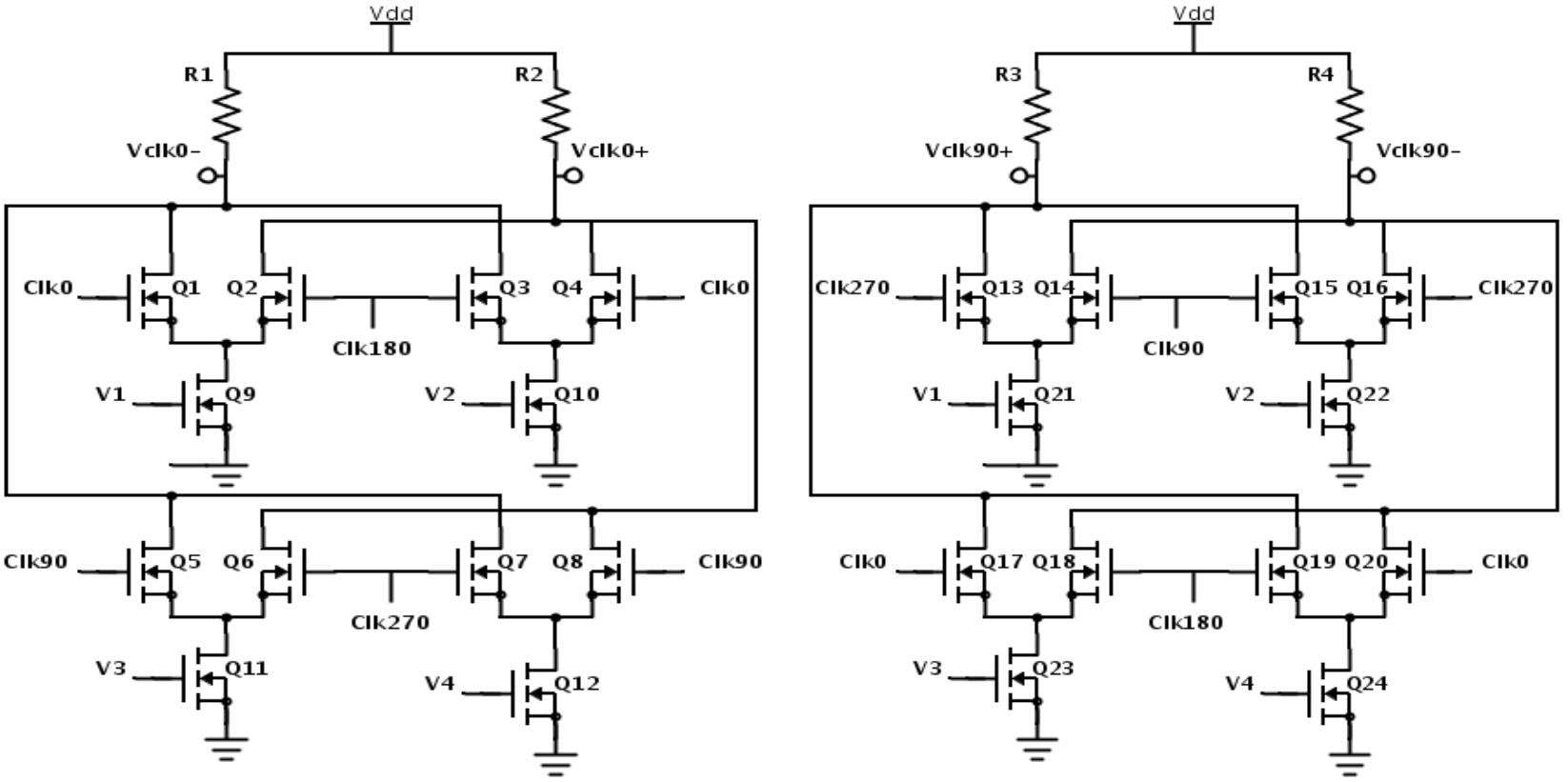
$$a_1^2 + a_2^2 = \text{constant “circle Raduis”}$$

- Linear Approximation $a_1 + a_2 = constant$



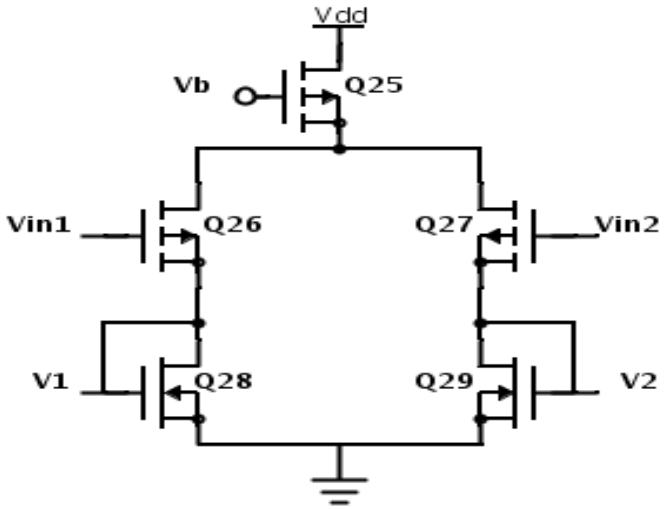
Currents Generation Concept

Clocks **0°** and **90°** PI Cores



Currents Generation Concept

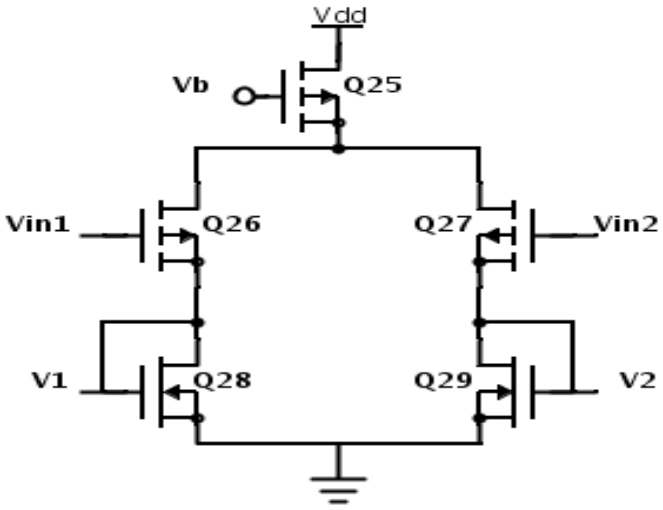
V-to-I Converter

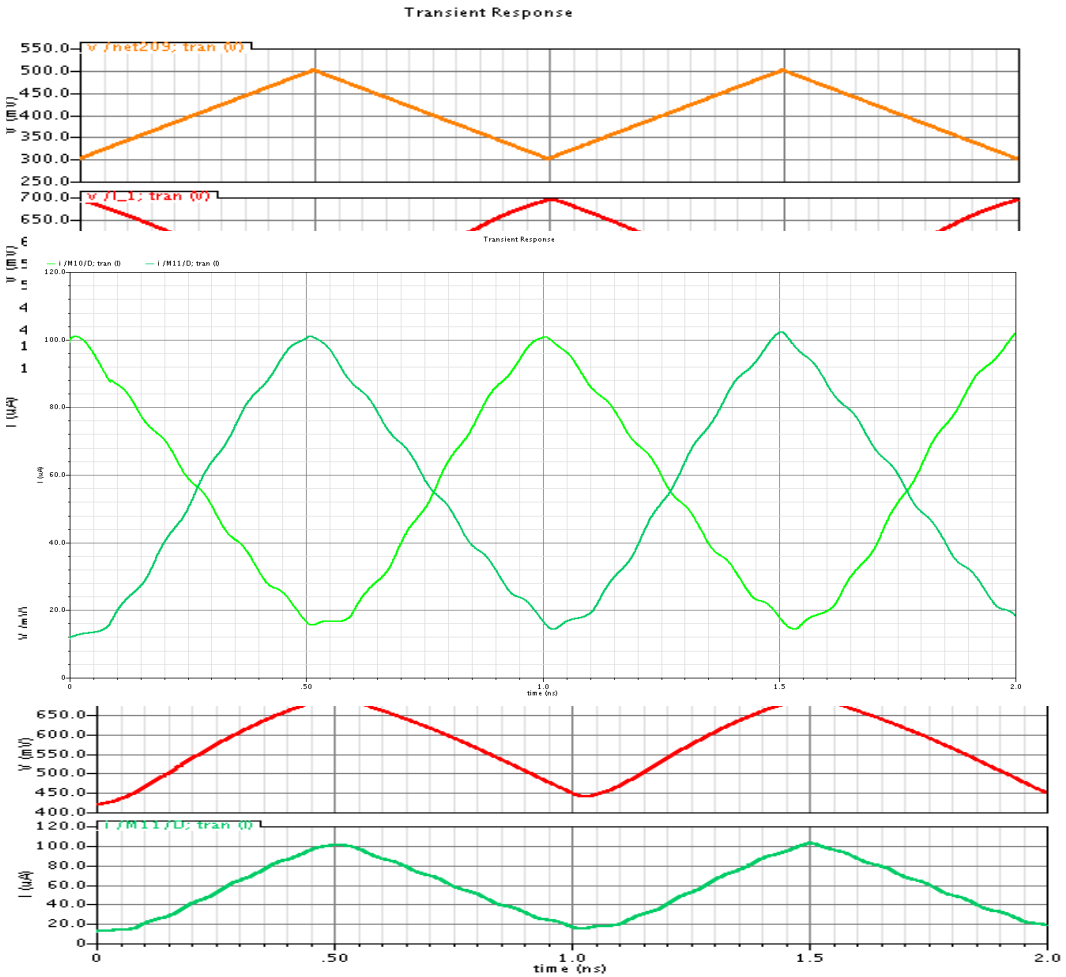


Input Ports	Max-DC value	Min-DC value
Vin1 and Vin2	500mV	300mV

Output Ports	Max-DC value	Min-DC value
V1 and V2	690.5mV	420.5mV

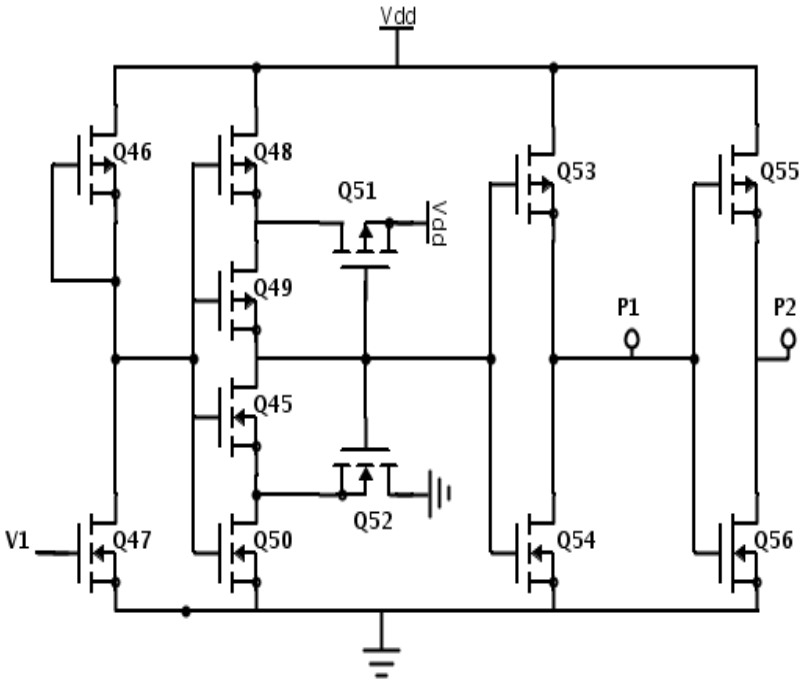
Currents Generation Concept

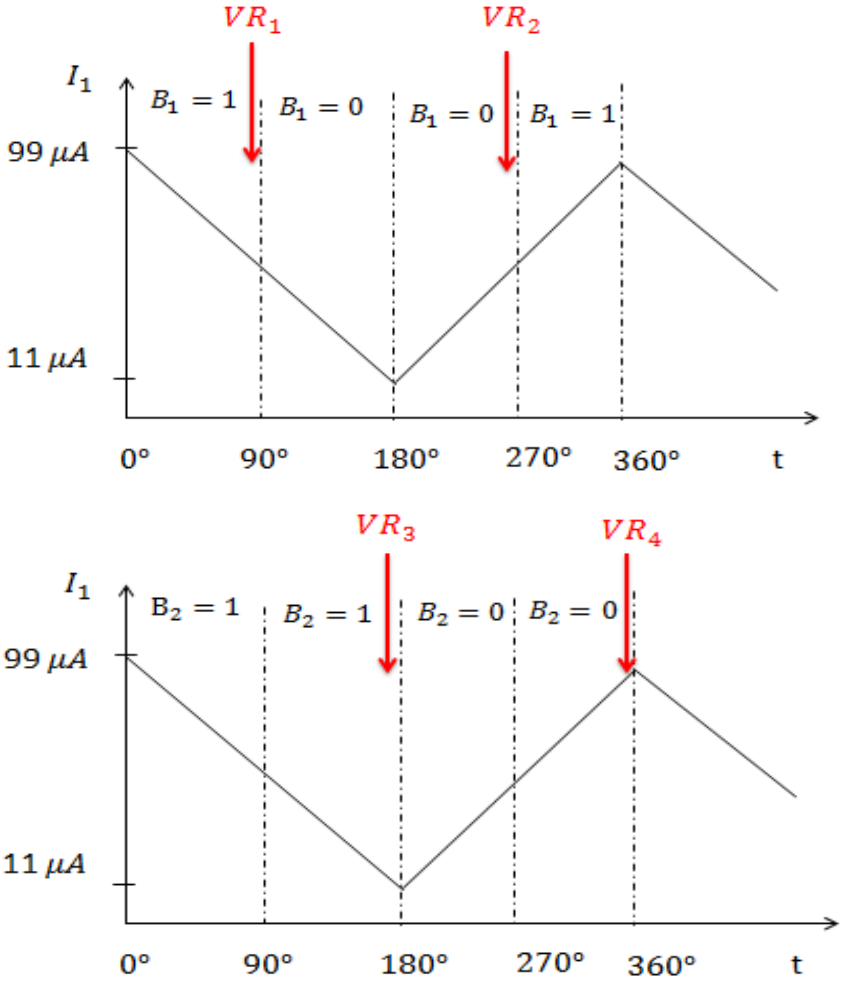




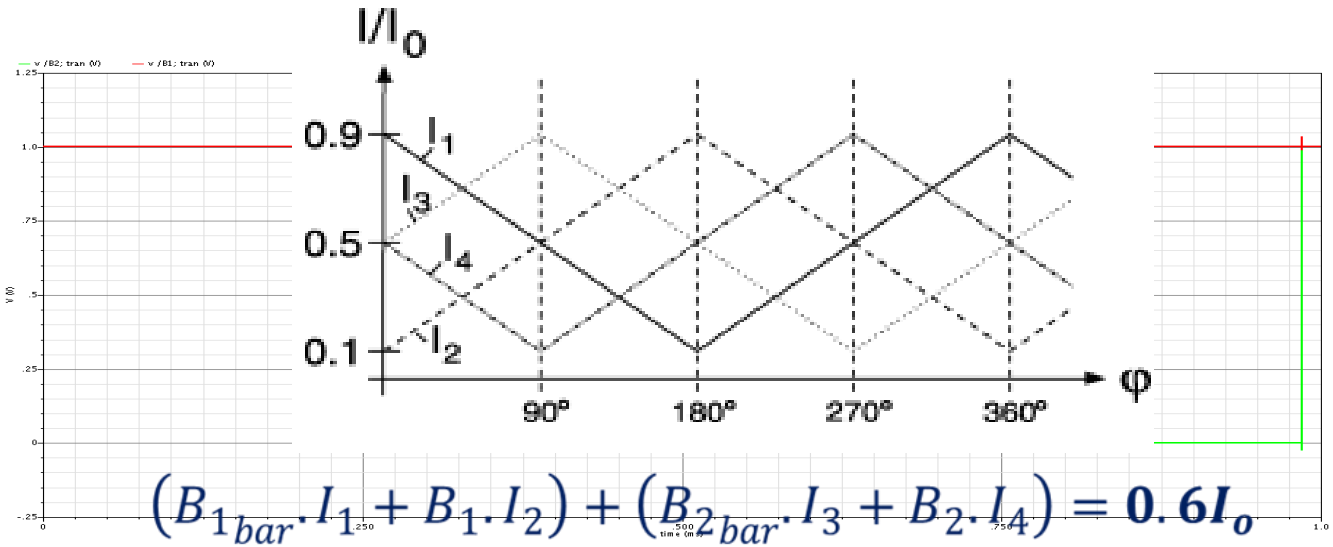
Currents Generation Concept

Schmitt Trigger Comparator





Currents Generation Concept

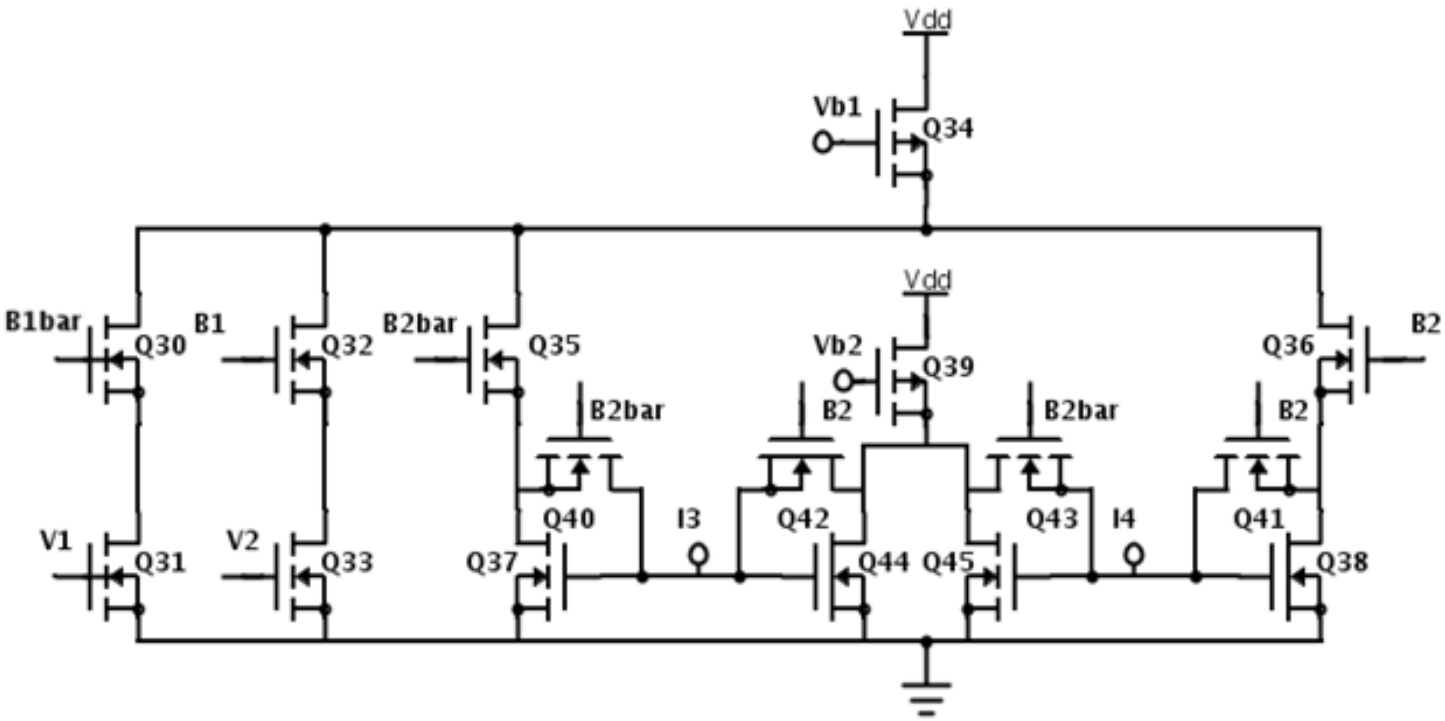


$$\left(B_{1_{bar}}.I_1 + B_1.I_2\right) + \left(B_{2_{bar}}.I_3 + B_2.I_4\right) = \mathbf{0.6}\boldsymbol{I_o}$$

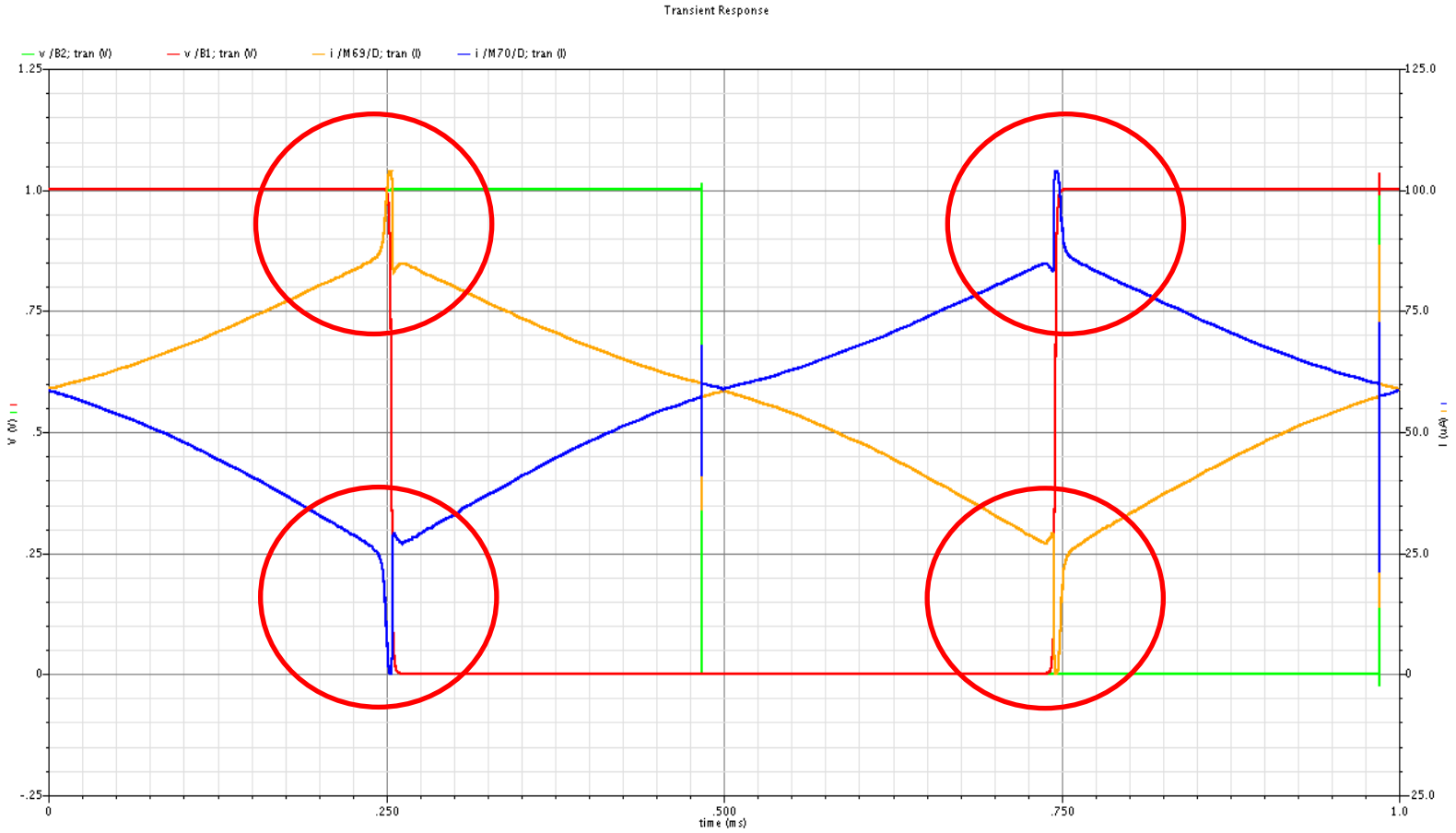
Quads	$B_1\ B_2$
1st	11
2nd	01
3rd	00
4th	10

Currents Generation Concept

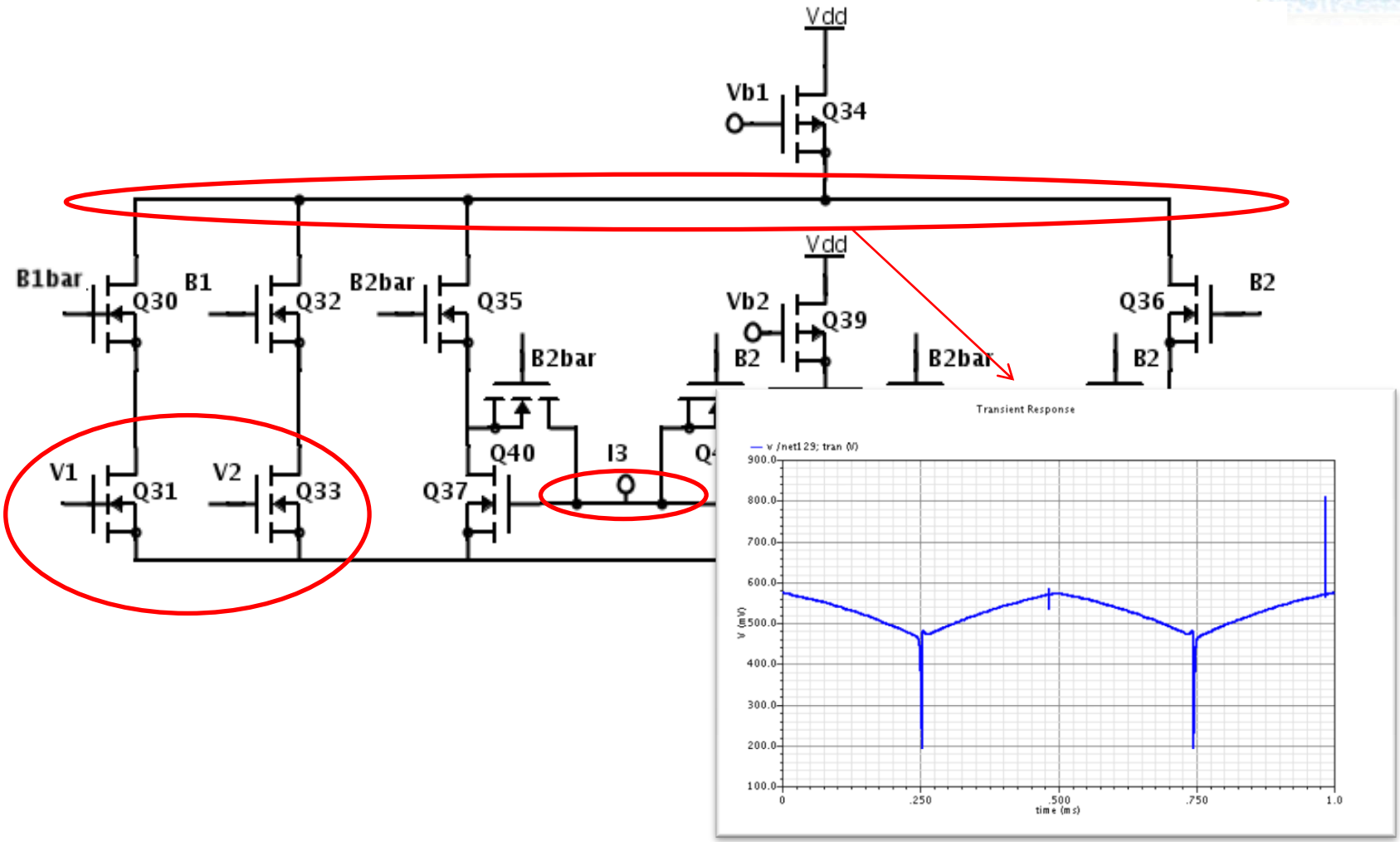
PI Controller



Currents Generation Concept

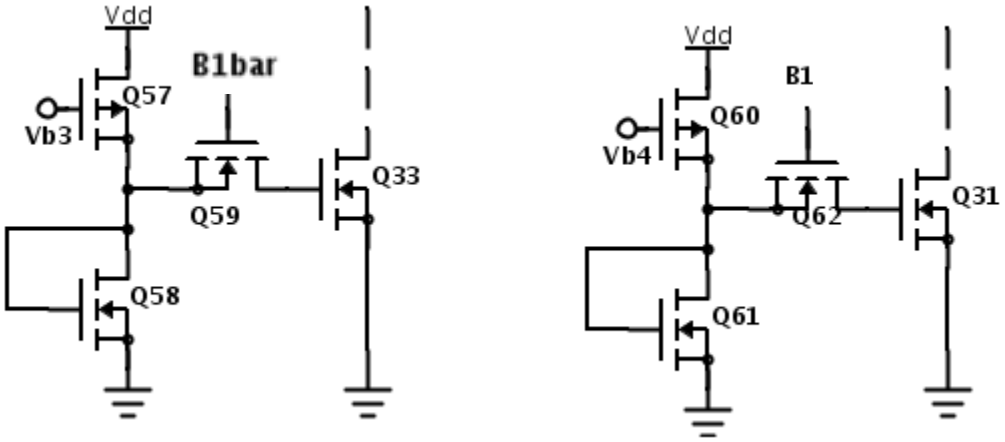


Currents Generation Concept



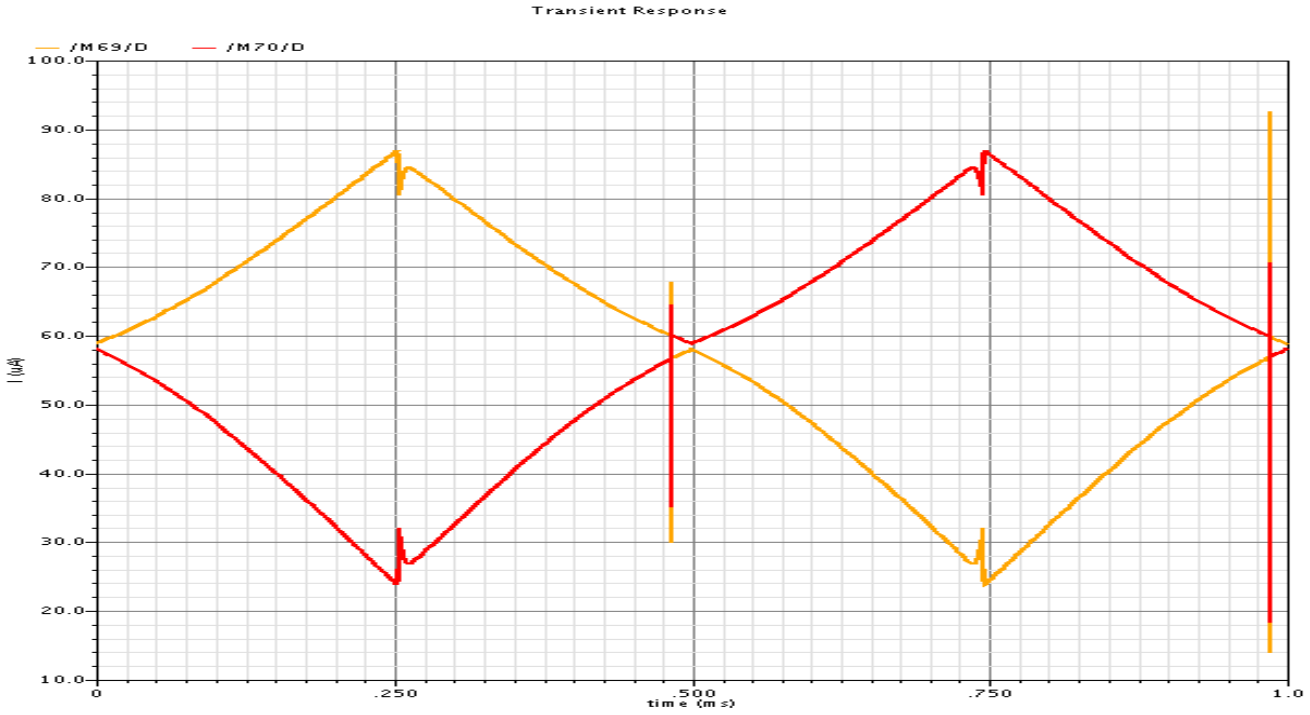
Currents Generation Concept

Spikes Suppression and Voltage Clamping

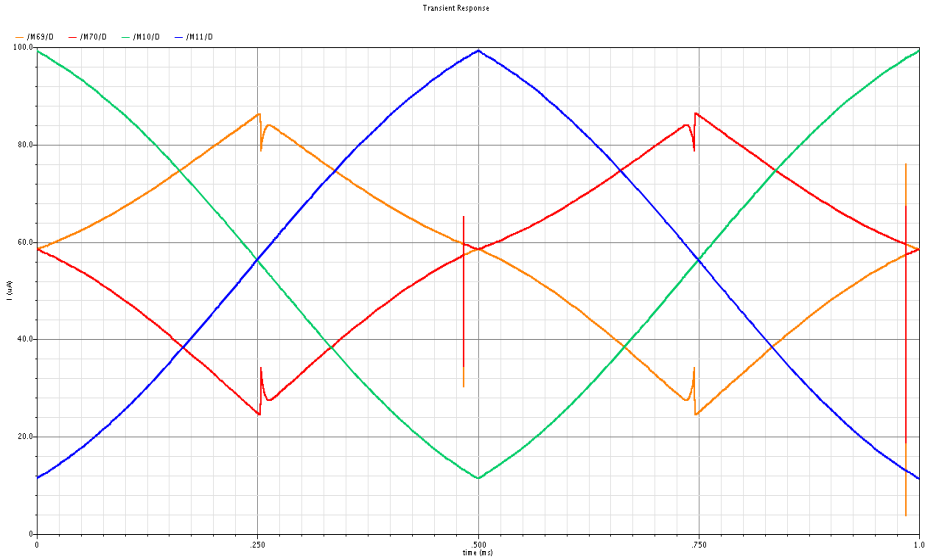


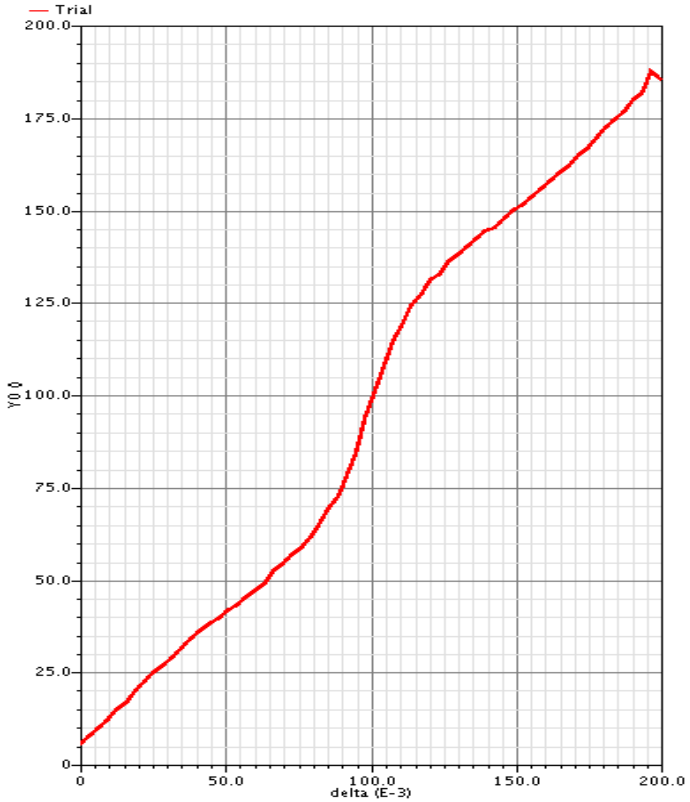
Currents Generation Concept

Spikes Suppression and Voltage Clamping



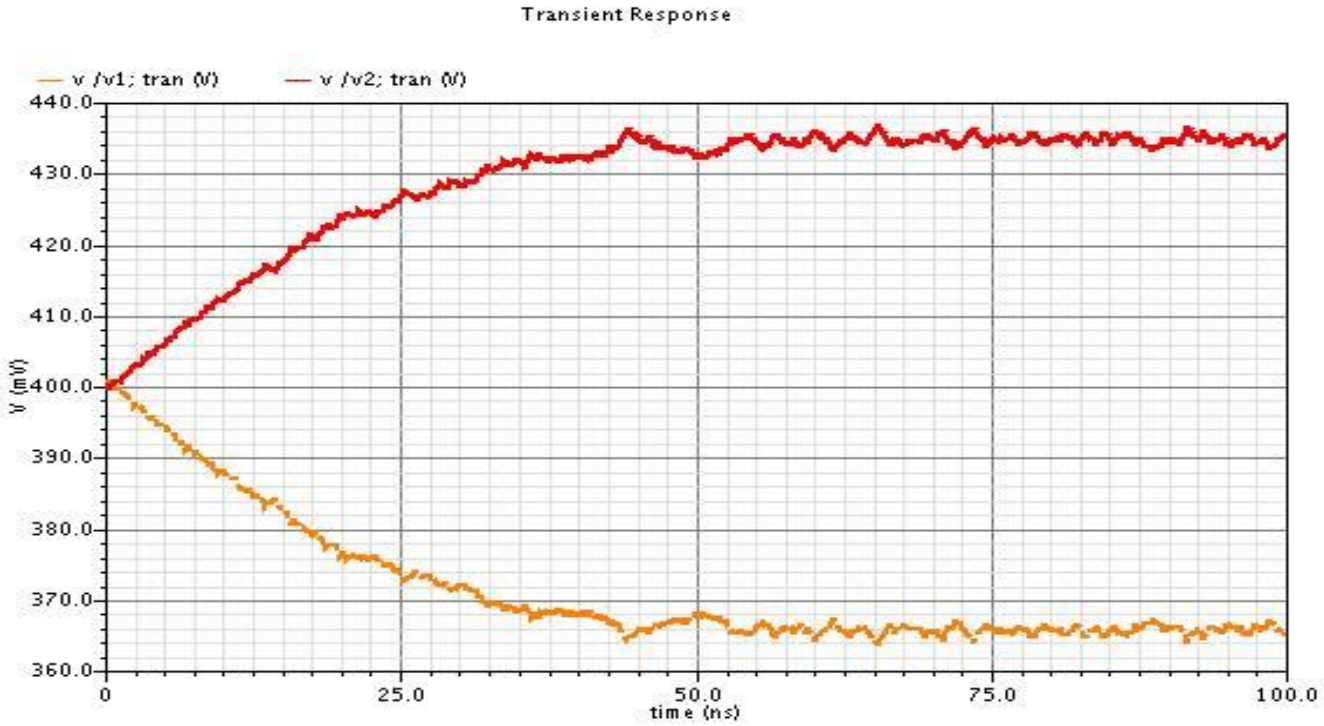
Final Results



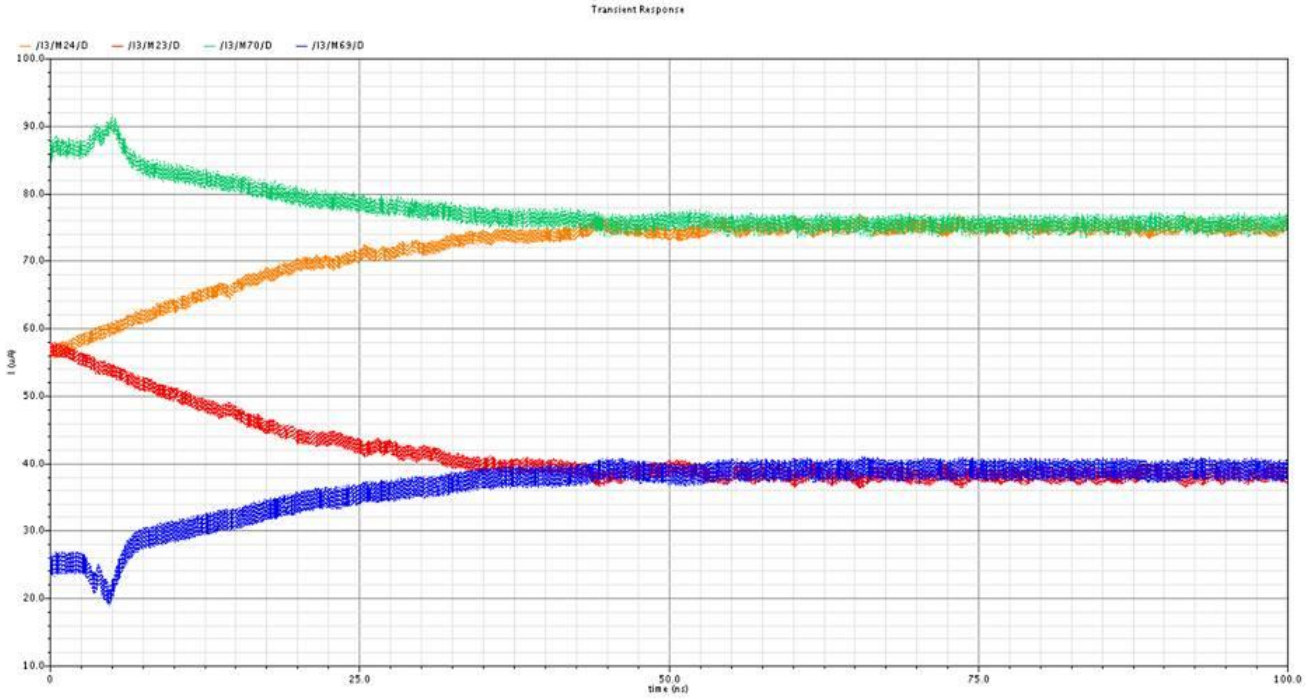


$$K_{PI} = 0.5851°mV$$

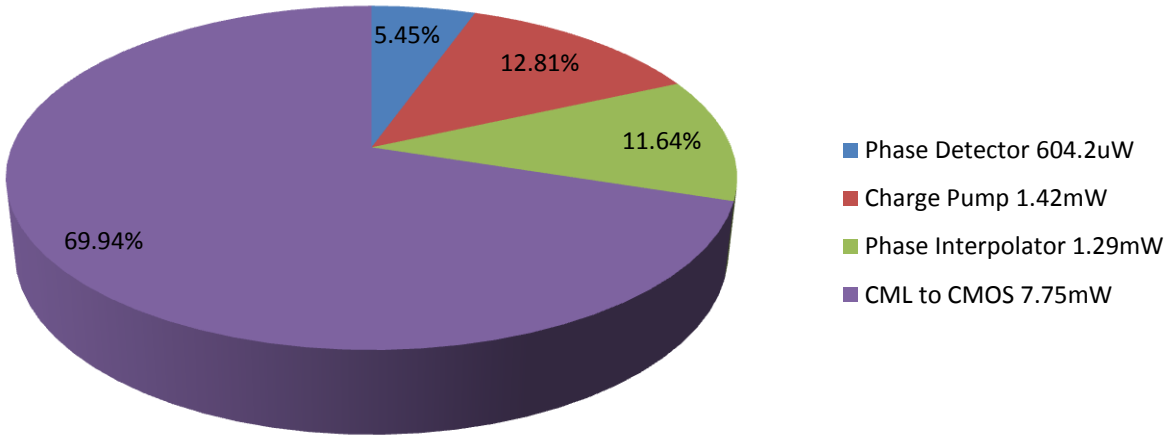
CDR Loop Locking



CDR Loop Locking



CDR Power Consumption



Total Power Consumption 11.08 mw

De-Serializer
(De-MUX)

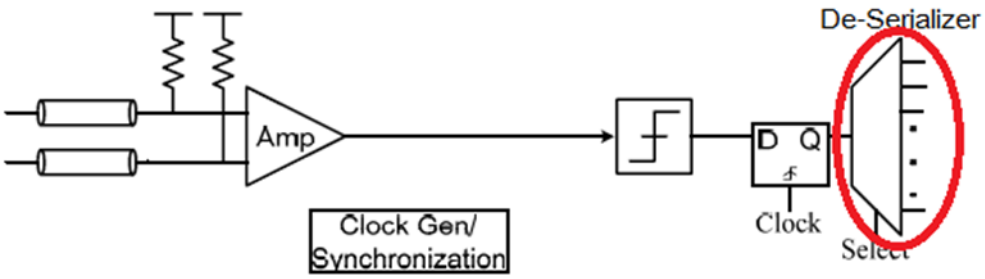
Presented by : Ahmed Hesham

Outlines

- Introduction
- Basic concepts
- Architecture
- Topologies
- Simulation and Results
- References
- Questions

Introduction

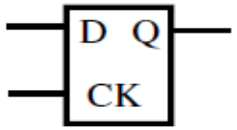
- **De multiplexing:** Transferring serial input data into parallel output. that allows lower frequency relative to data rate.
- The Demux circuit is the far end of our system.
- The input is a 2 single ended lines from the phase Interpolator with data rate equals 5.8 Gb/s.
- The output is 16 single ended lines with data rate 725 Mb/s.



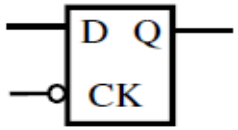
Basic Concepts

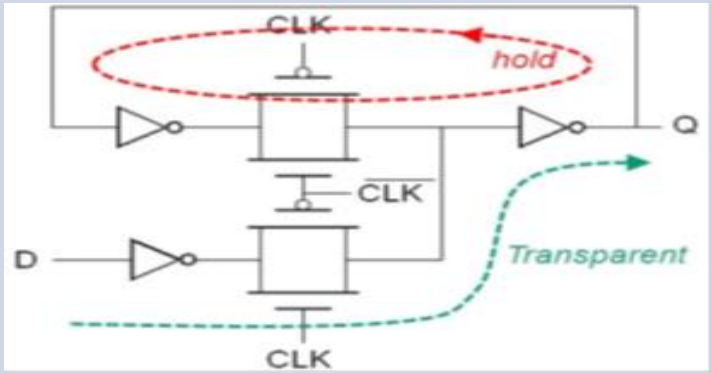
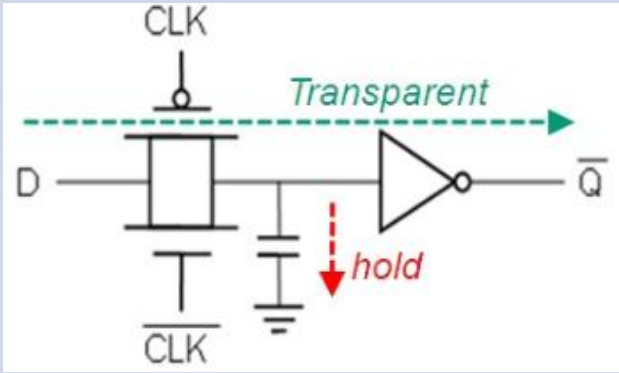
- Latches

Positive Latch
(data pass when clock is high)



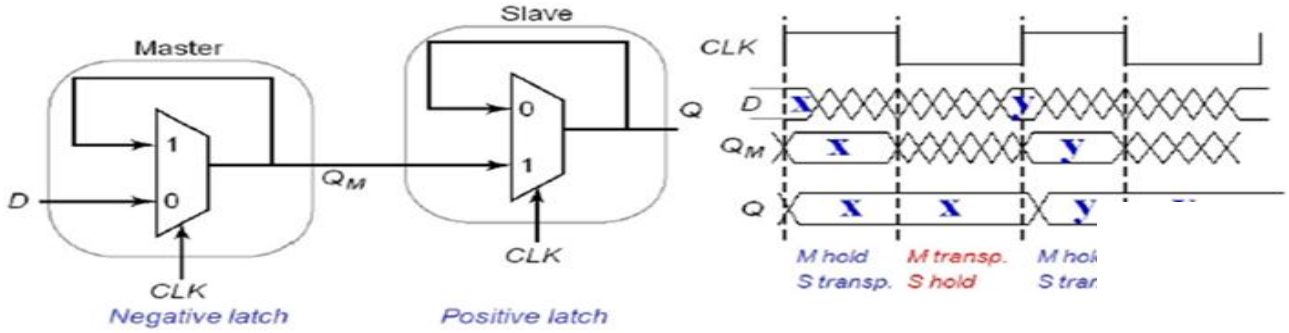
Negative Latch
(data pass when clock is low)



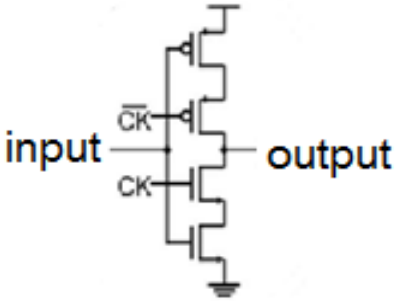
Static Latch	Dynamic Latch
	
CLK high ⇒ D affects Q CLK low ⇒ feedback loop stores Q	CLK high ⇒ D affects Q CLK low ⇒ Q is floating

Basic Concepts

- **Master-Slave Flip Flops:** Two latches can be connected as Master& salve to operate as a flip flop.

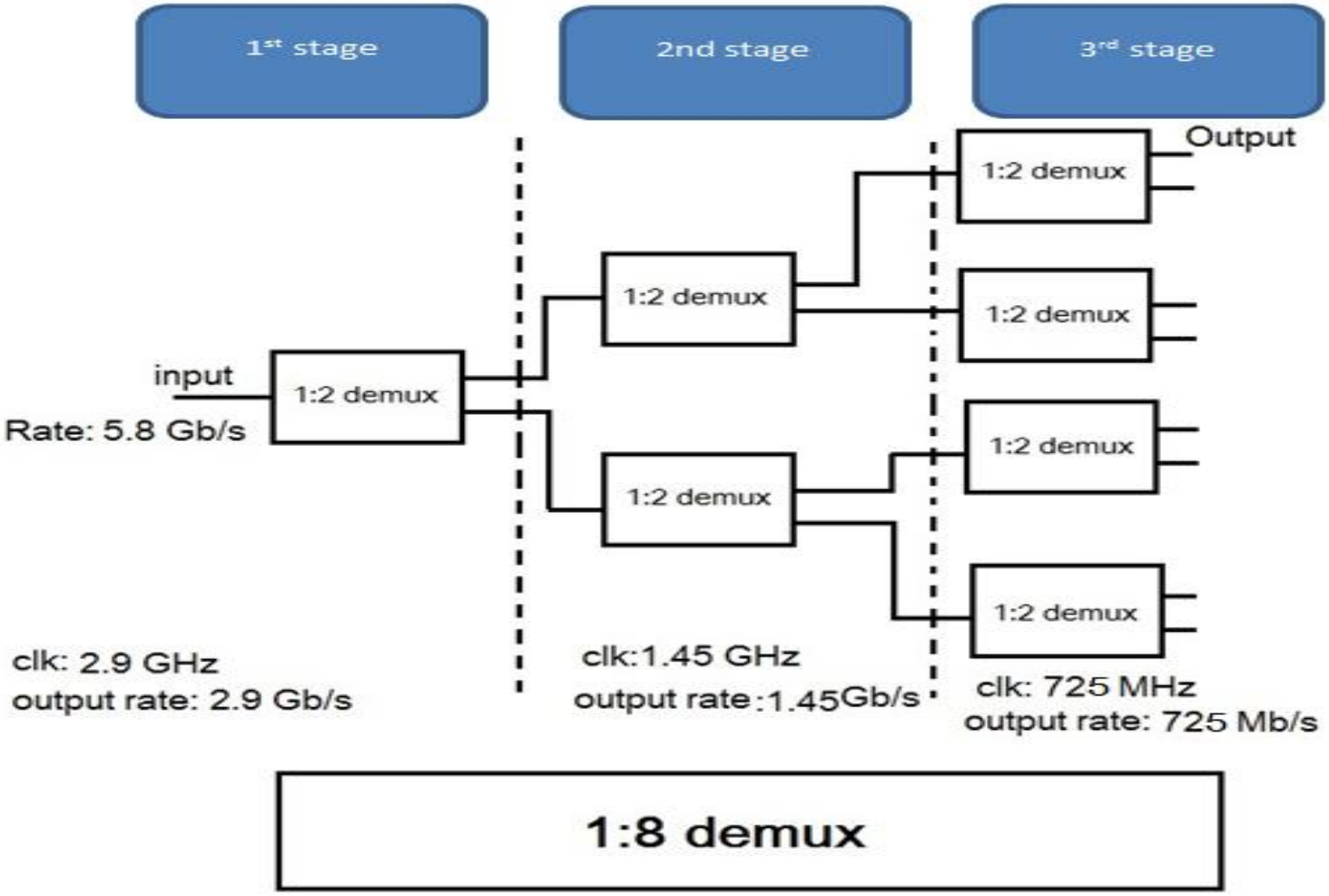


- **Clocked Inverters:**



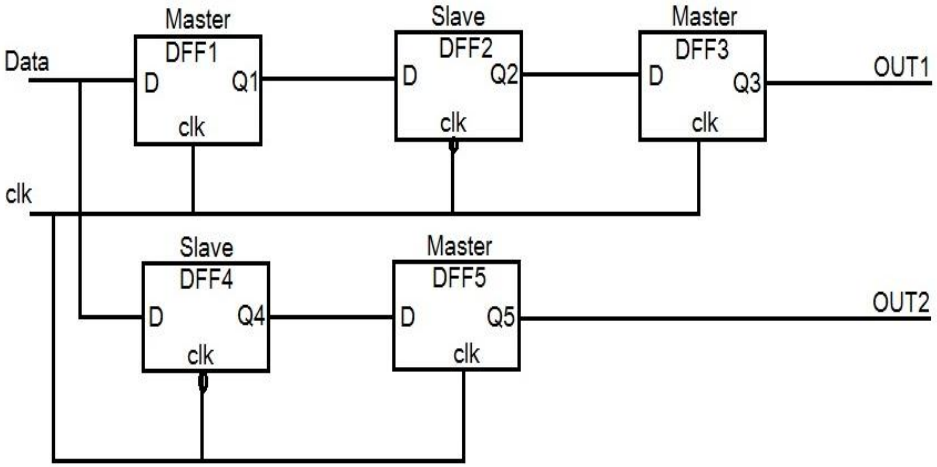
- is an inverter that controls its output by a clock.
- If clk = 1, Inverter pass the input to output & If clk = 0, it holds the data as a latch (high impedance).

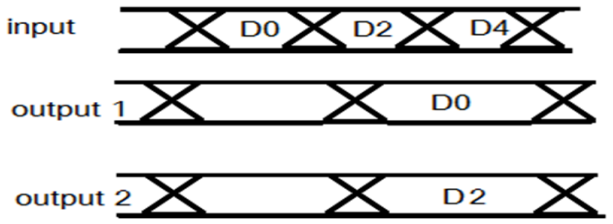
Architecture



Topologies

- The conventional 1:2 Demux cell using 5 Latches

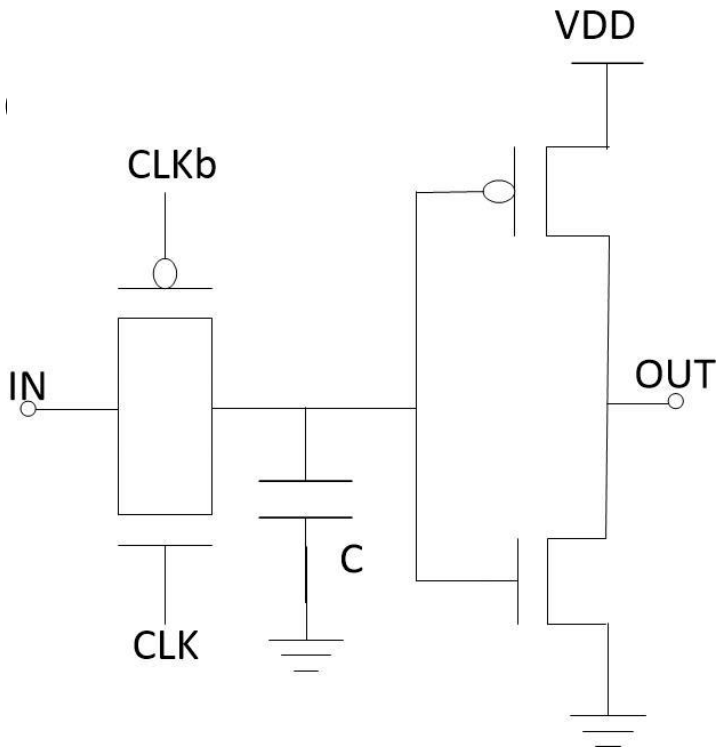




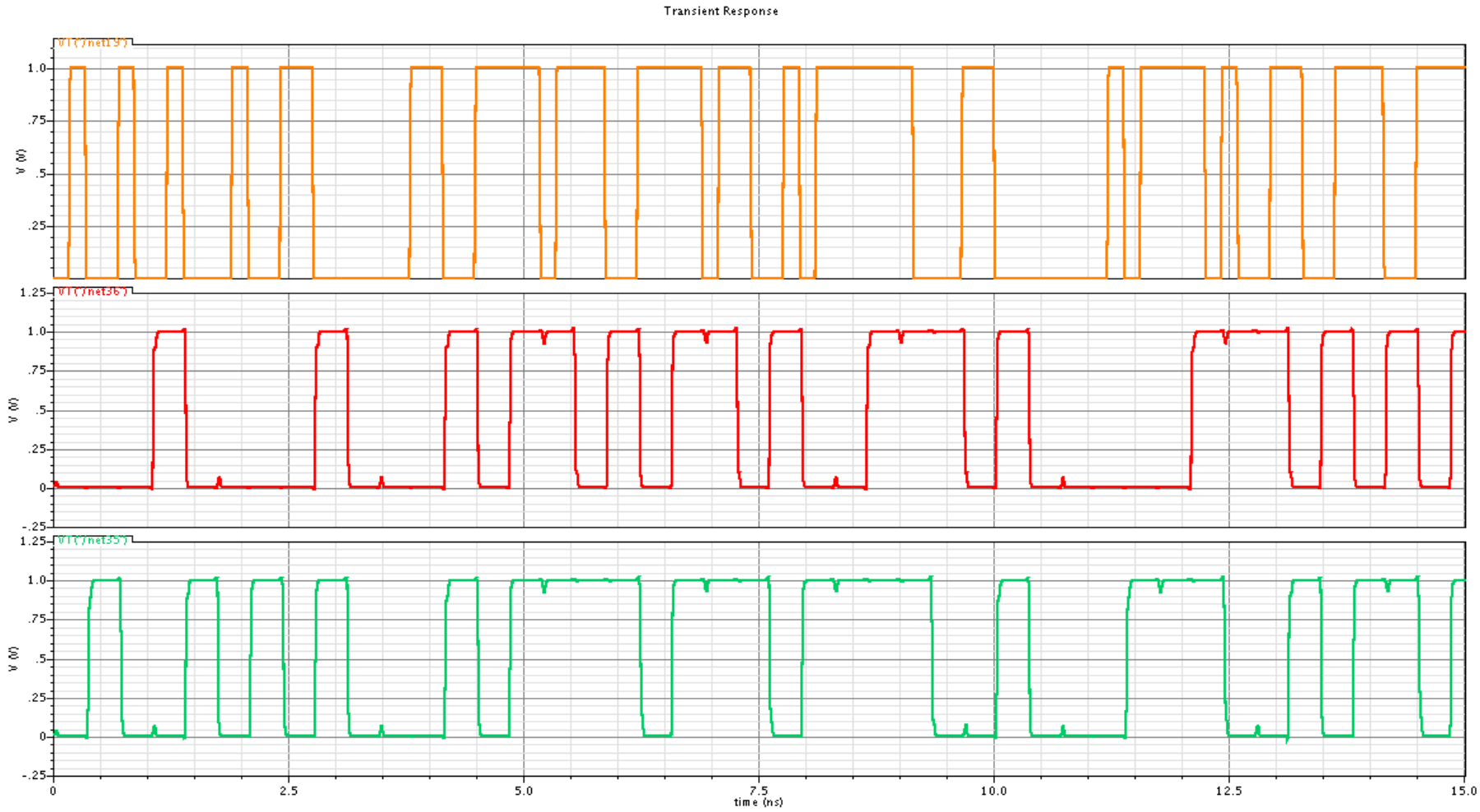
- DFF1, DFF2 makes a falling edge master-slave trigger
- DFF4, DFF5 makes a raising edge master-slave trigger
- In order to synchronize both outputs (1&2) DFF3 is used (half a duty cycle delay)

Topologies

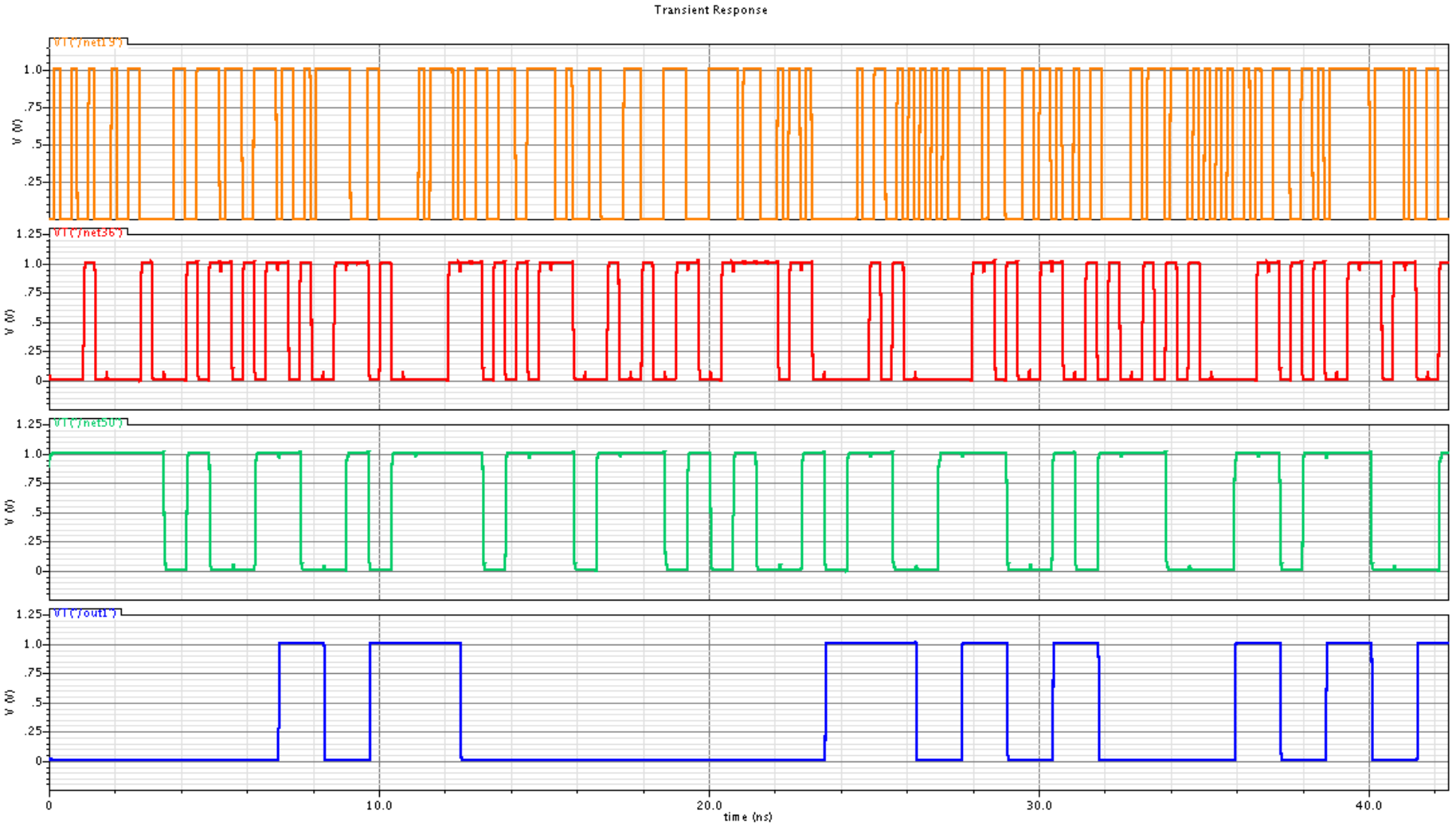
- CMOS Dynamic Latch
- CLK high ➡ IN affects Out n
- CLK low ➡ Out Floating
- Advantage:
- Low power consumption ☺
- Can Handle high speed ☺



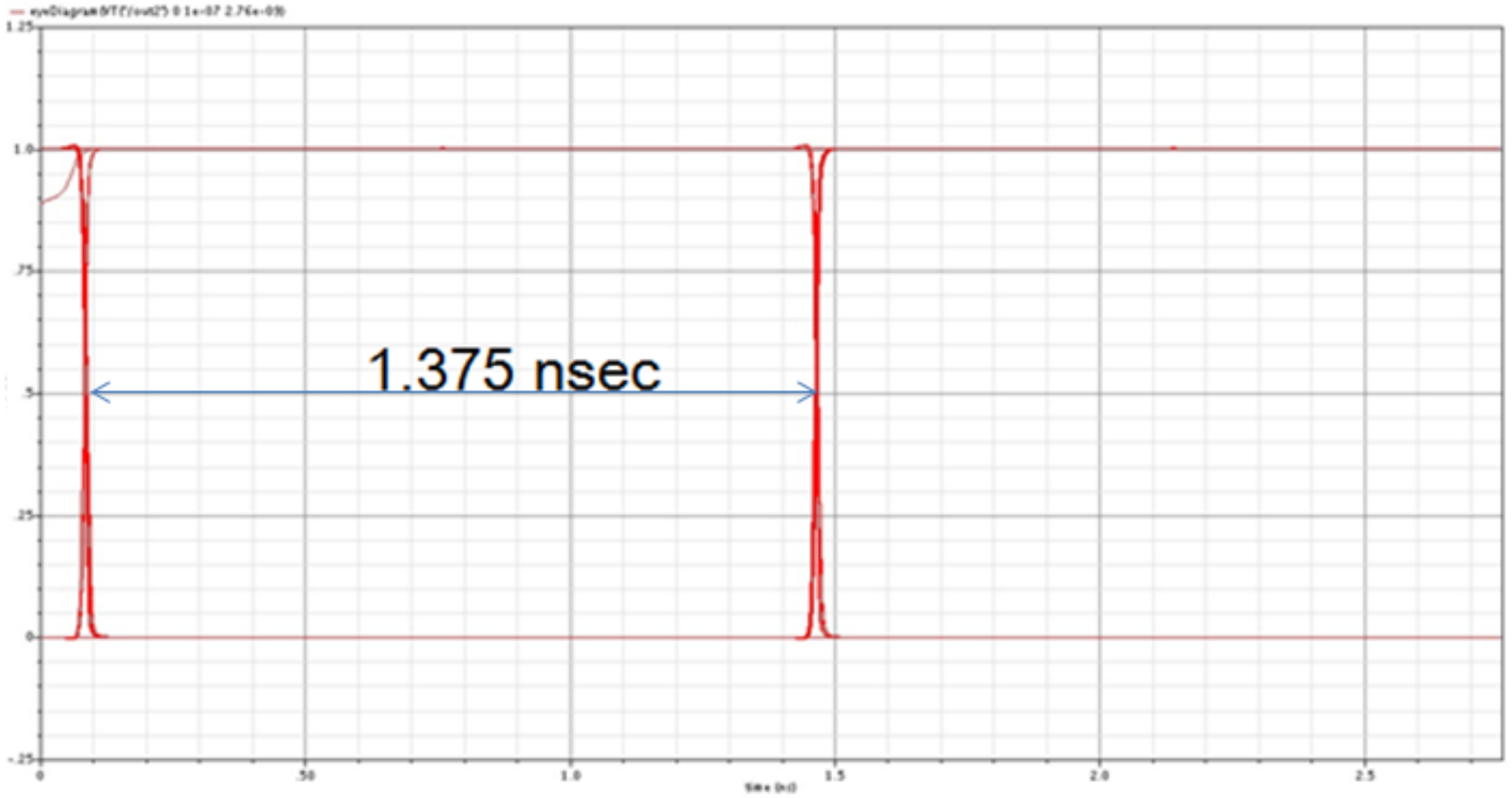
Simulation & Results(1)



Simulation & Results(2)



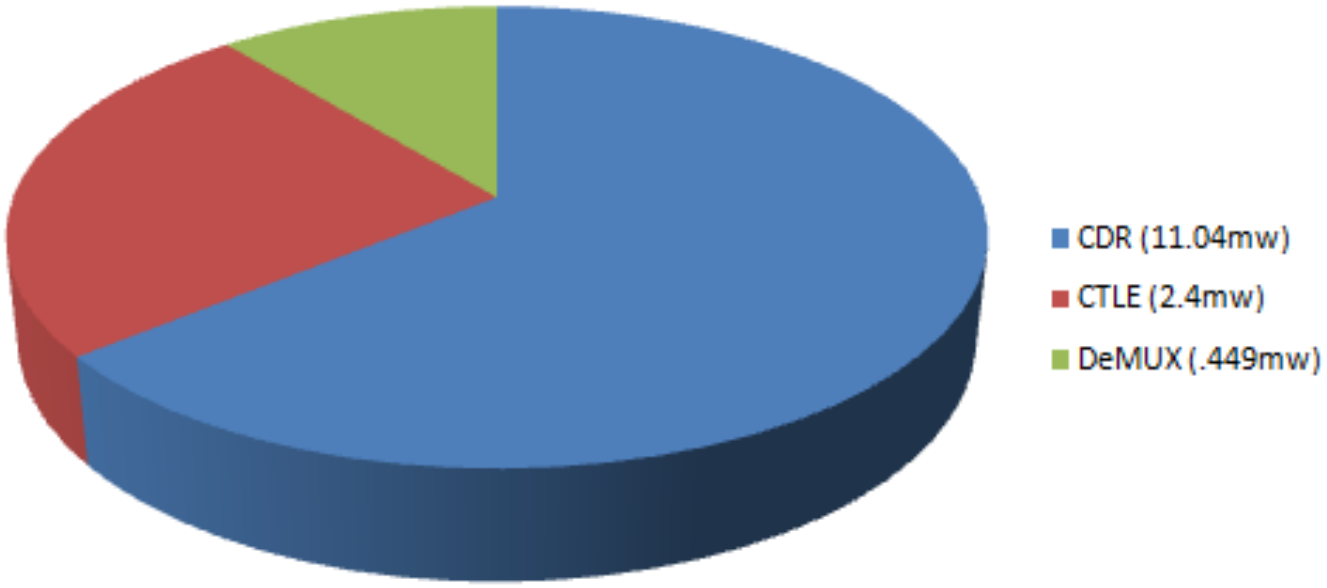
Simulation & Results



References

- 1-Kehrer D, Wohlmuth H D, Knapp H, et al. 40-Gb/s 2:1 multi-plexer and 1:2 demultiplexer in 120-nm standard CMOS. IEEEJ Solid-State Circuits, 2003, 38(11): 1830
- [2] Kanada K, Yamazaki D, Yamamoto T, et al. 40 Gb/s 4:1MUX/1:4 DEMUX in 90 nm standard CMOS. IEEE Int Solid-State Circuits Conf Tech Dig, 2005: 152055007-4
- Zhang Changchun et al. May 2009
- [3] Kim B G, Kim L S, Byun S, et al. A 20 Gb/s 1:4 DEMUX with-out Inductors in 0.13_m CMOS. IEEE Int Solid-State CircuitsConf Tech Dig, 2006: 528
- [4] Chien J C, Lu L H. A 20-Gb/s 1:2 demultiplexer withcapacitive-splitting current-mode-logic latches. IEEE TransMicrow Theory Tech, 2007, 55(8): 1624
- [5] Rein H M, Moller M. Design considerations for very-high-speed Si bipolar IC's operating up to 50 Gb/s. IEEE J Solid-State Circuits, 1996, 31(8): 1076
- [6] 0165.Digital Integrated Circuits (2nd Edition) by Jan M. Rabaey

Receiver power consumption



Phase Locked Loop (PLL)

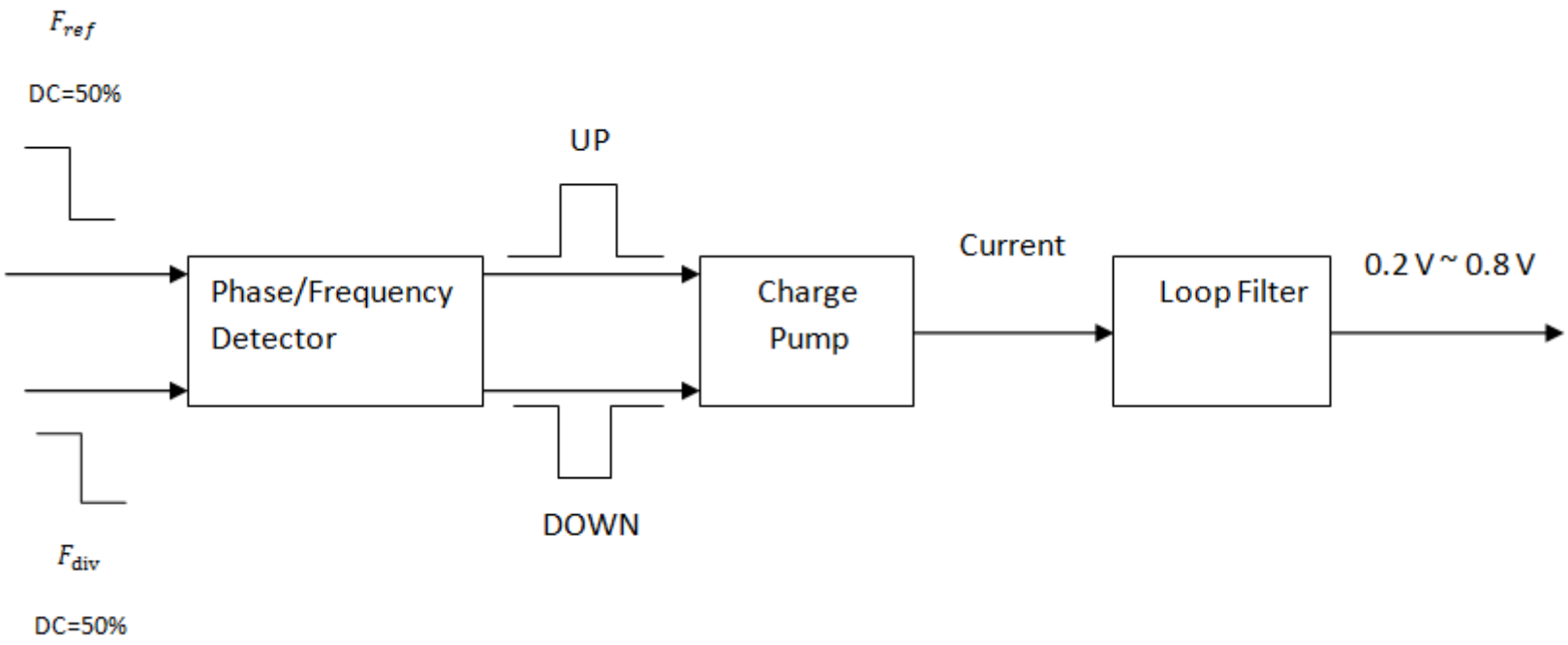
PFD/CP/LF

Presented by : Eman Salah El-Din

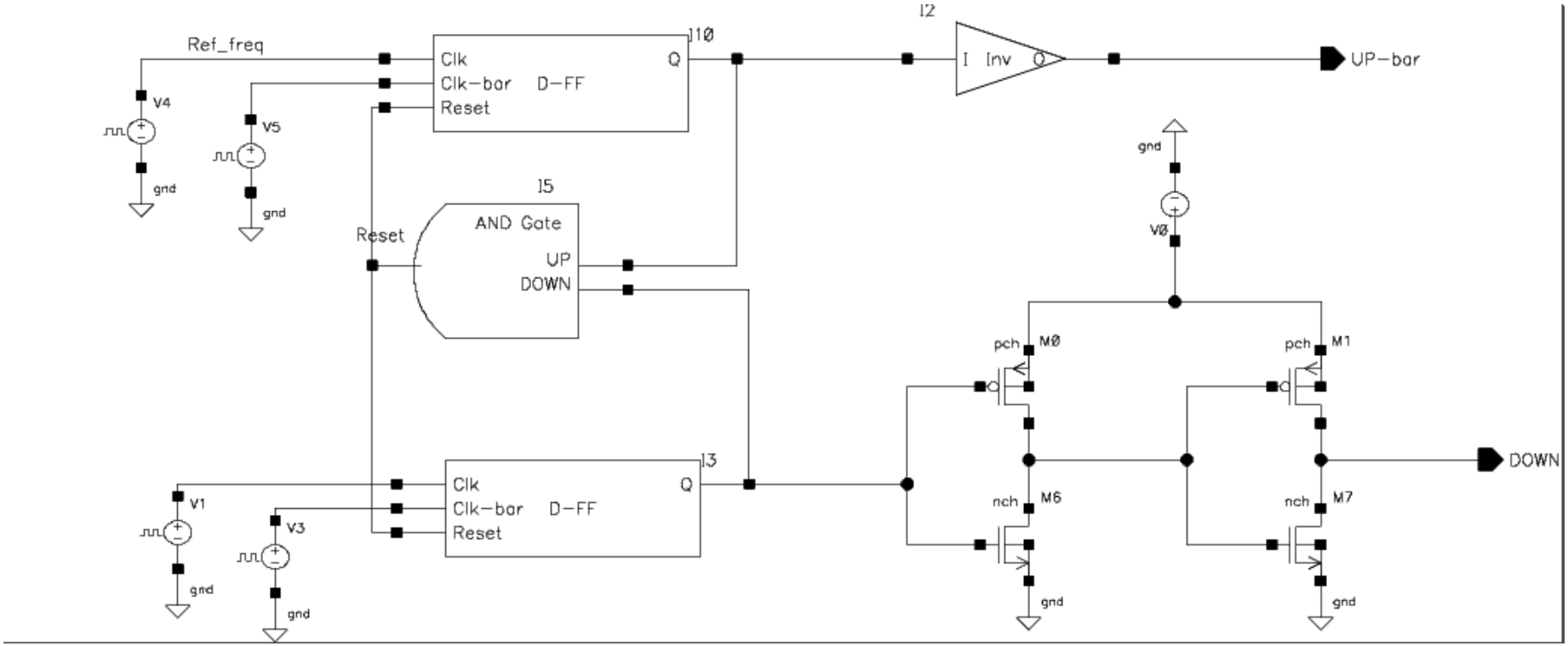
Outlines

- PFD/CP/LF Block Diagram
- Circuit Design
  - PFD
  - Charge Pump/LF
- Simulation Results
  - PFD
  - Charge Pump/LF
- Corners

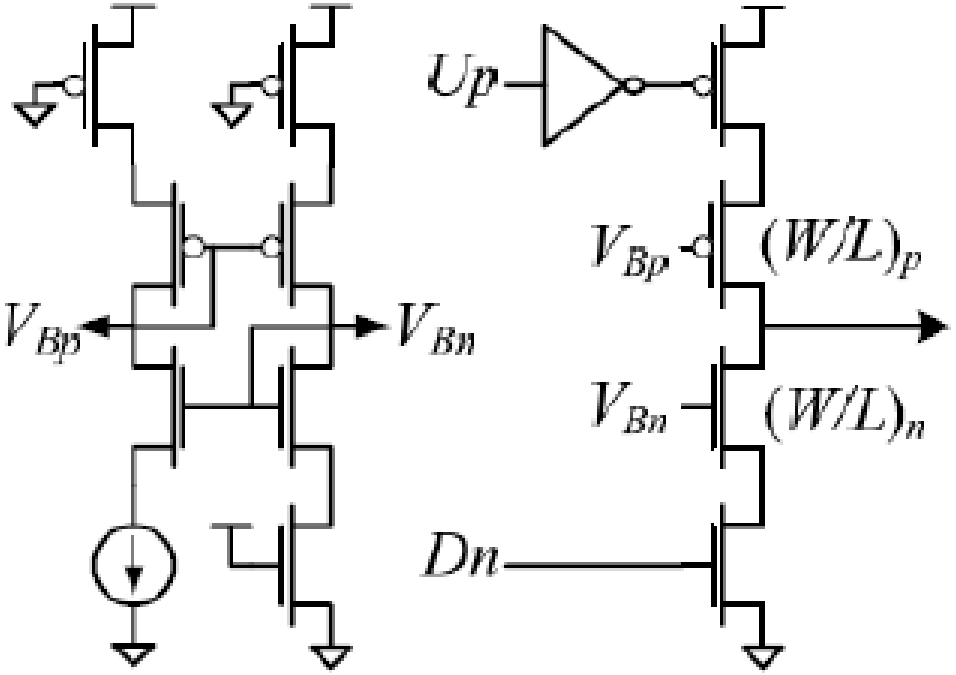
PFD/CP/LF: Block Diagram



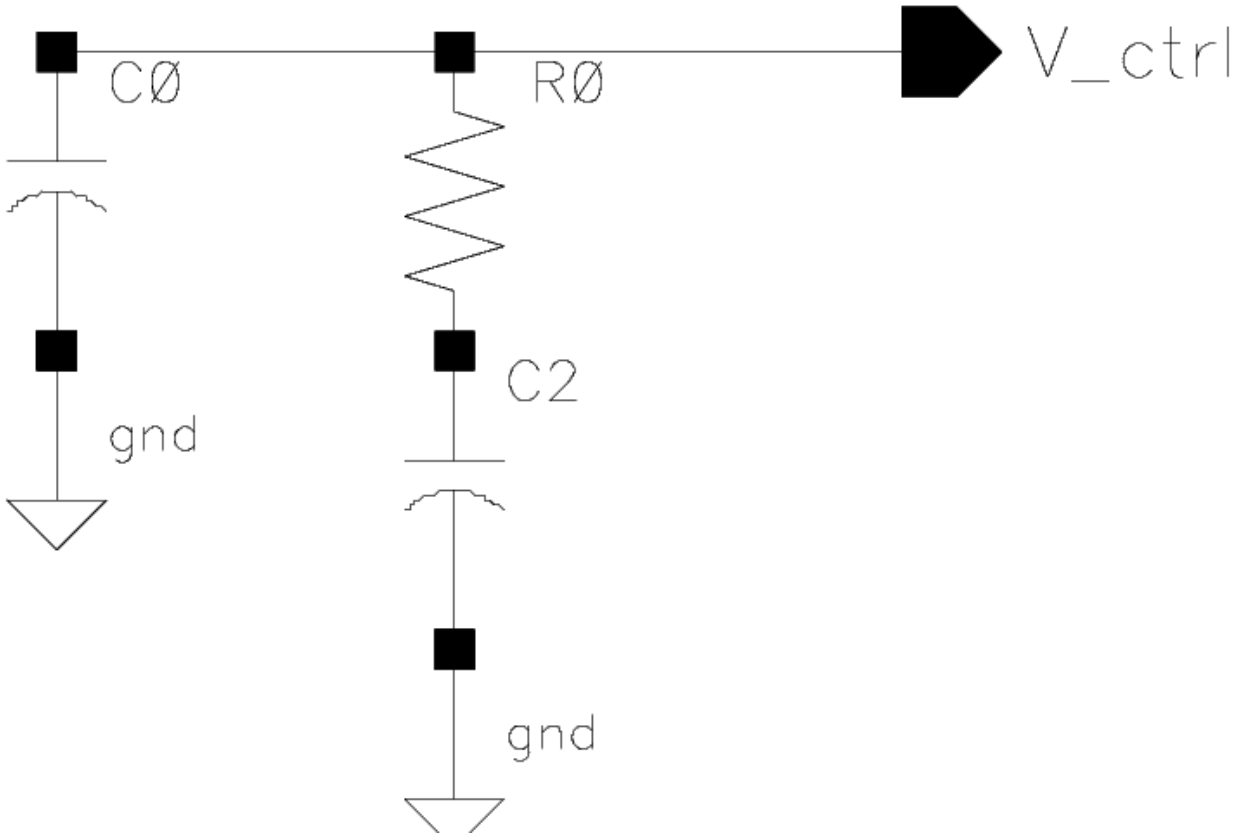
PFD Circuit


Ref_freq
V4
gnd
V5
gnd
Clk
Clk–bar
Reset
D–FF
Q
I10
I2
I
Inv
O
UP–bar
I5
AND Gate
Reset
UP
DOWN
gnd
V0
pch
M0
pch
M1
nch
M6
nch
M7
gnd
gnd
DOWN
V1
gnd
V3
gnd
Clk
Clk–bar
Reset
D–FF
Q
I3

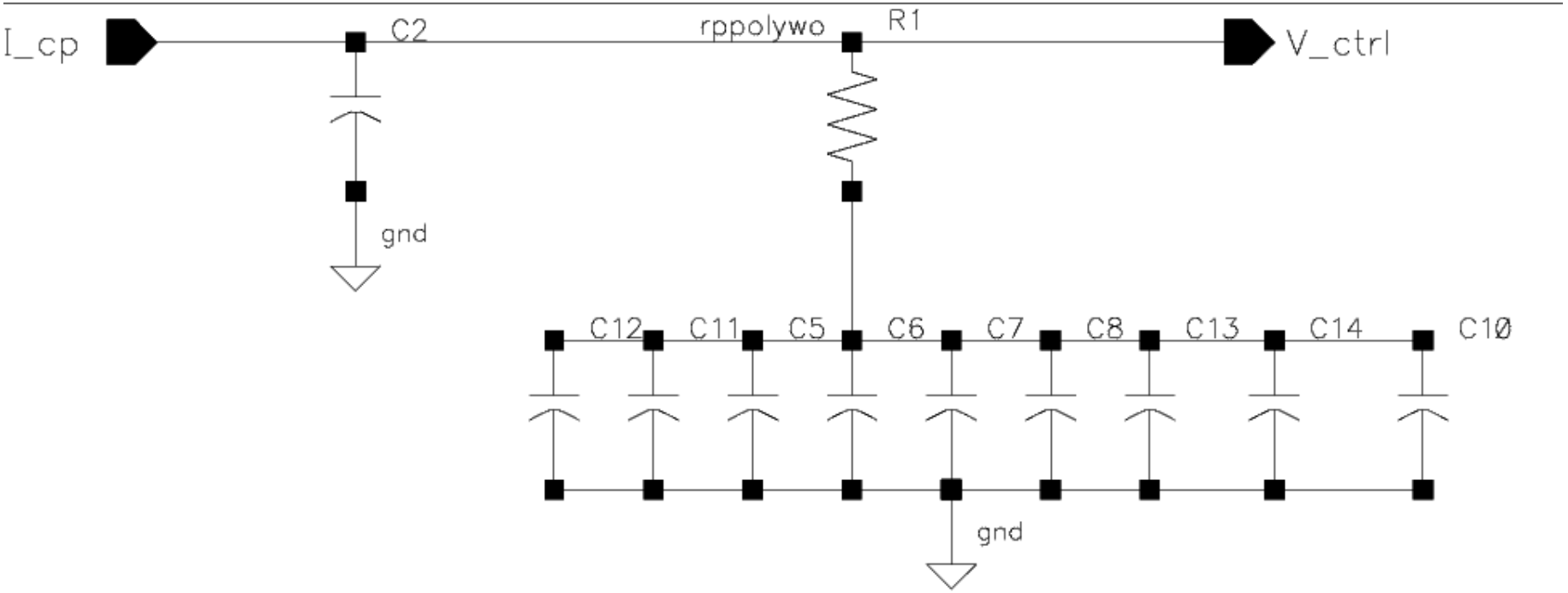
CP Circuit



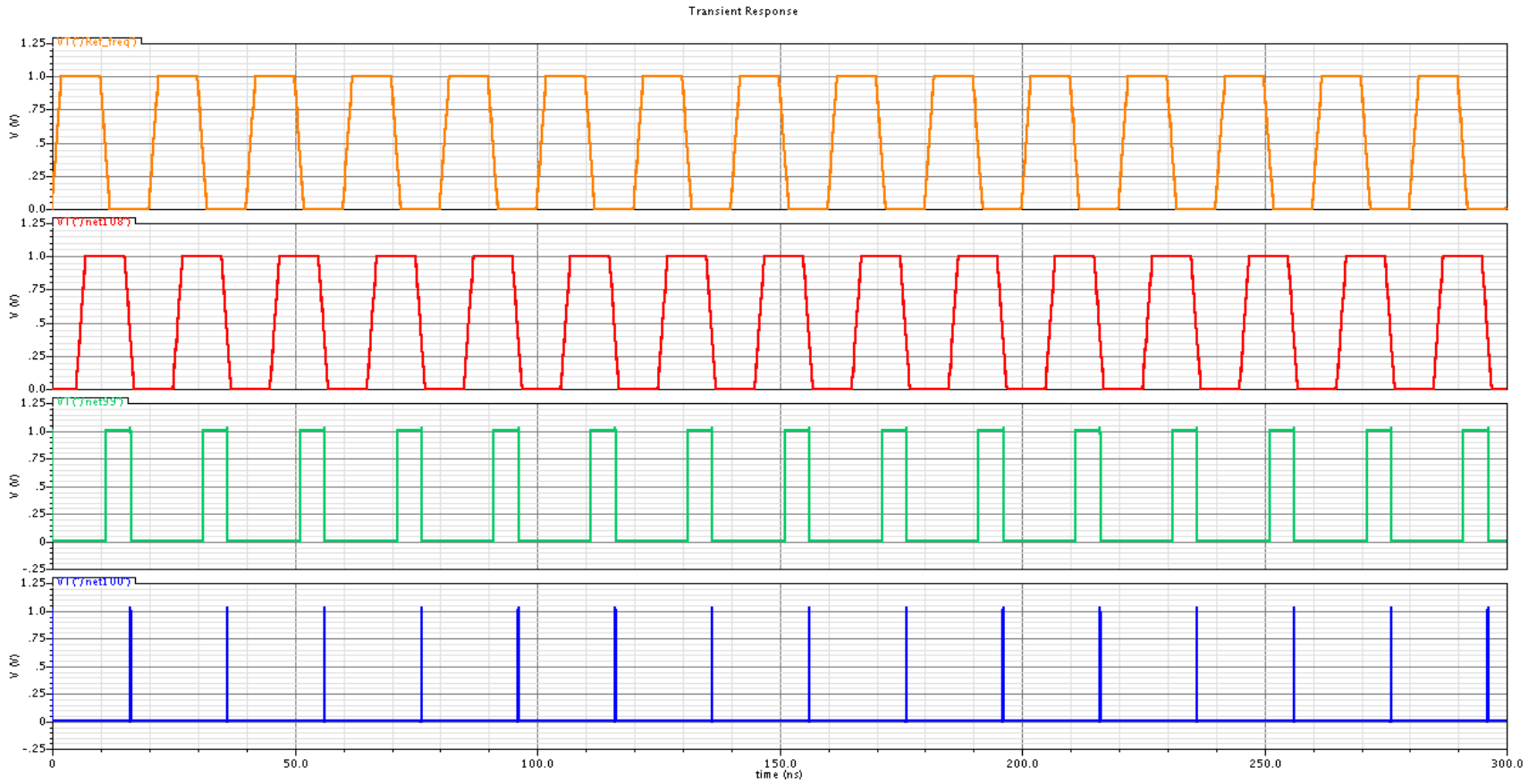
Loop Filter



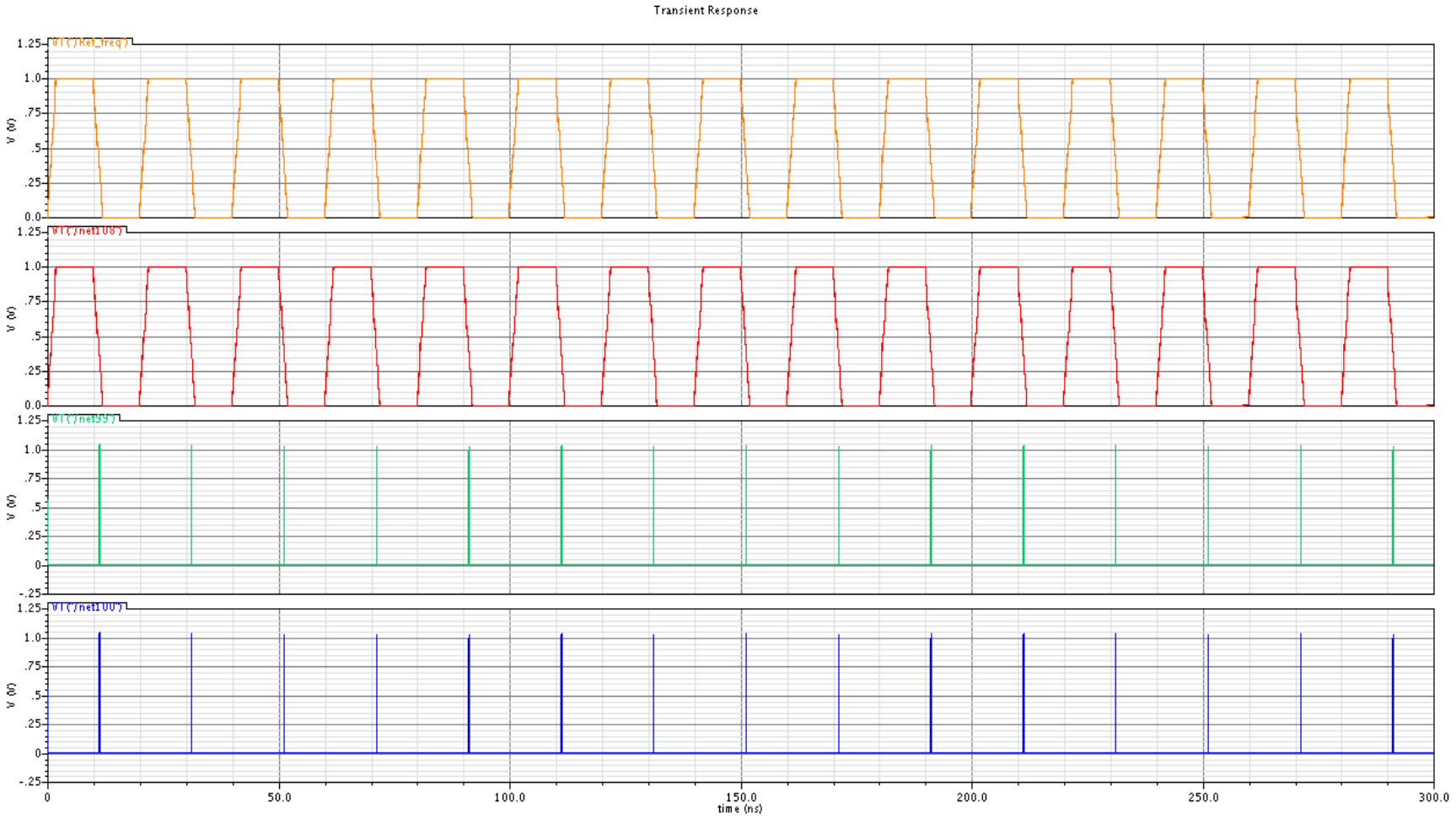
Loop Filter



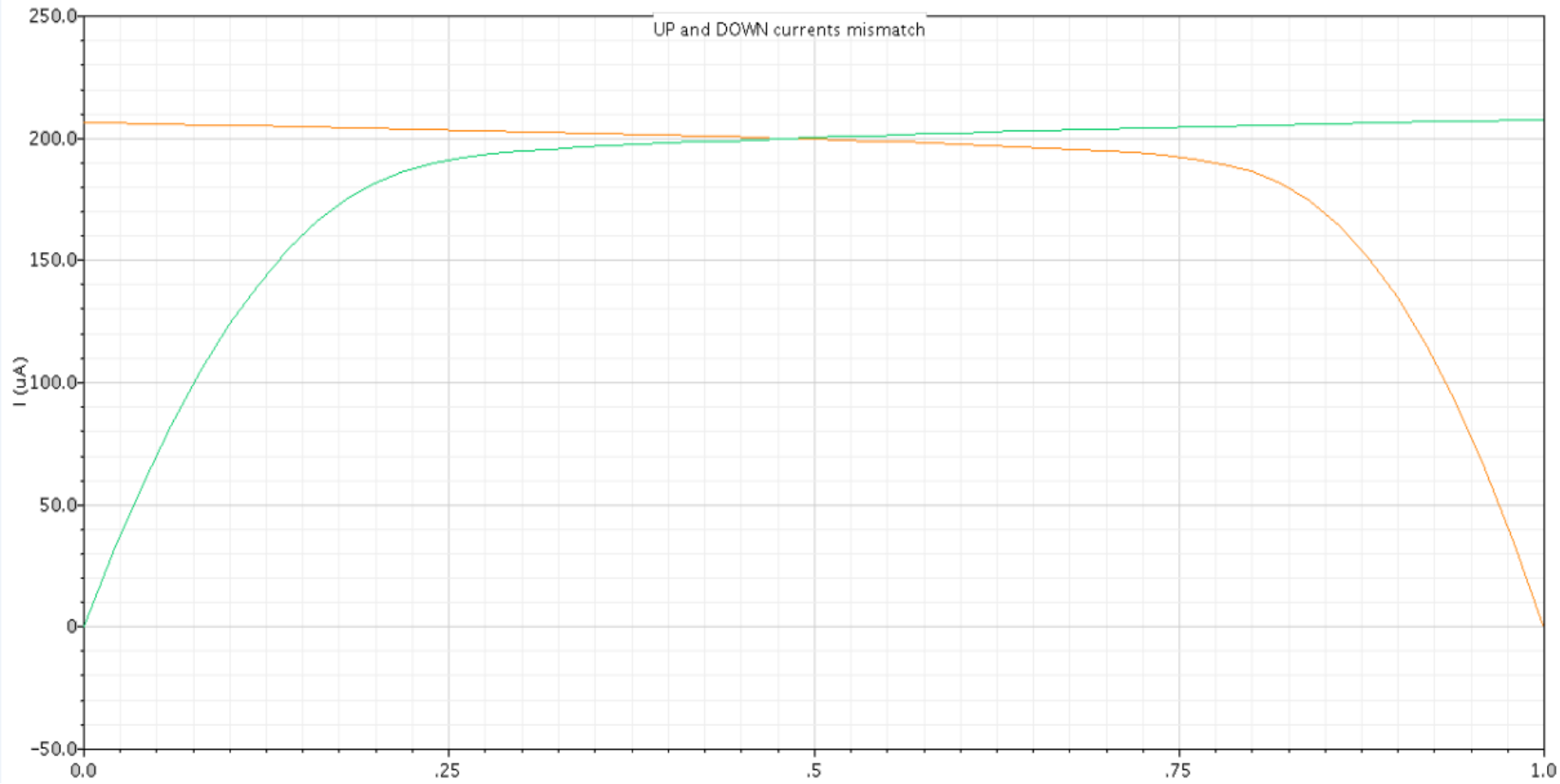
PFD: Results



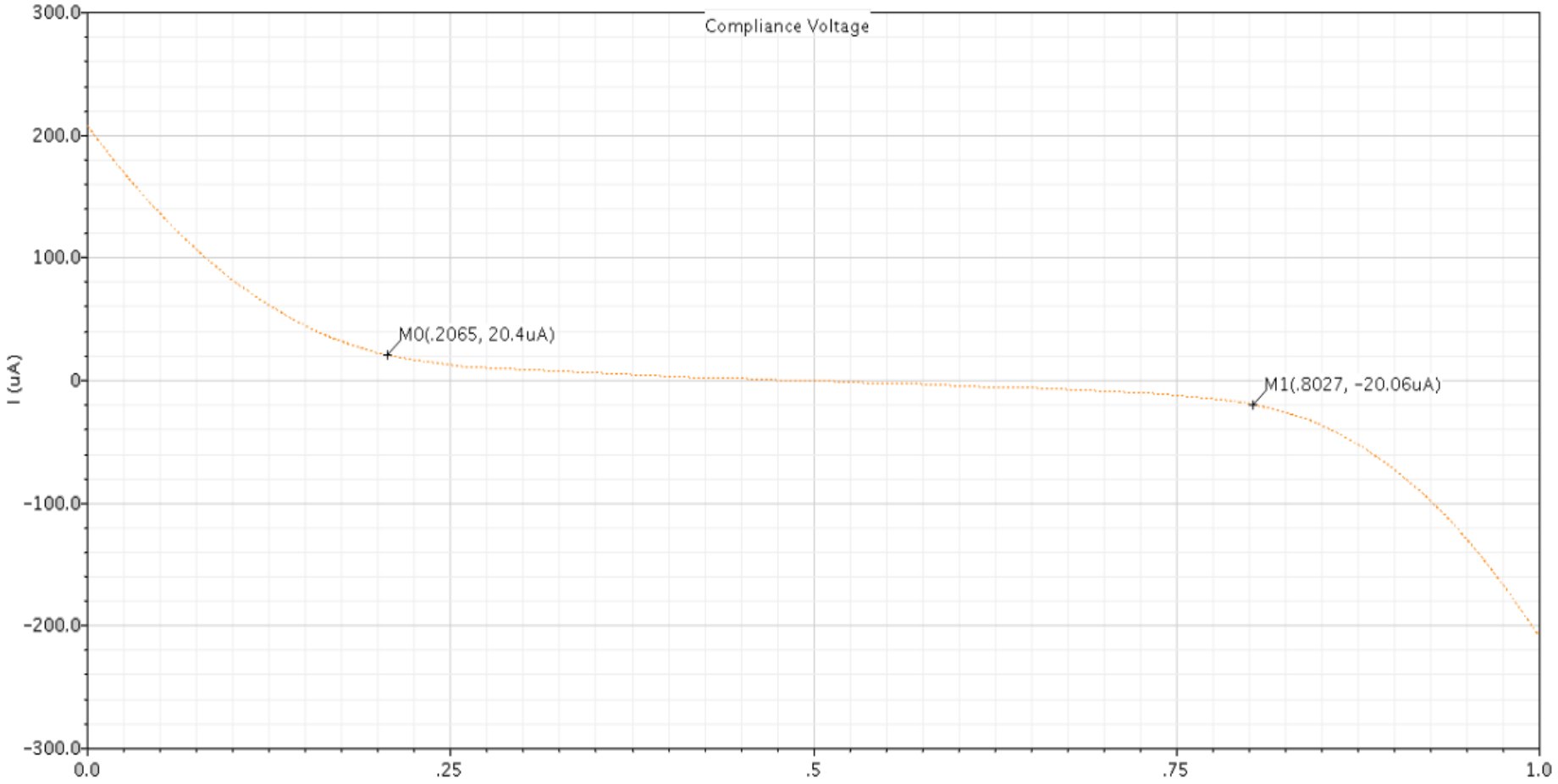
PFD: Results


Transient Response
V1(/Ref_freq)
V1(/net108)
V1(/net99)
V1(/net100)
V (V)
1.25
1.0
.75
.5
.25
0.0
0
-.25
50.0
100.0
150.0
200.0
250.0
300.0
time (ns)

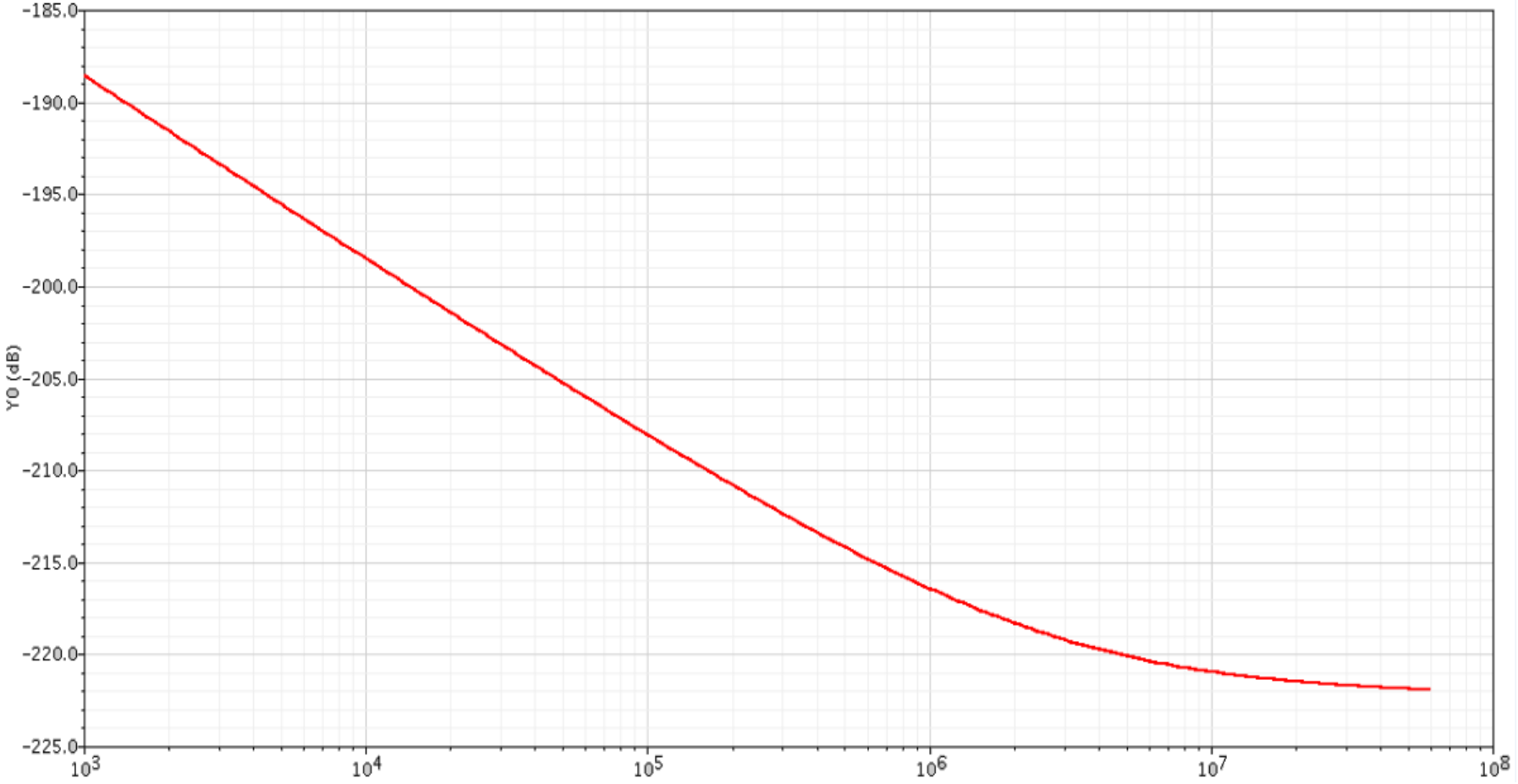
CP: Results:
Matching



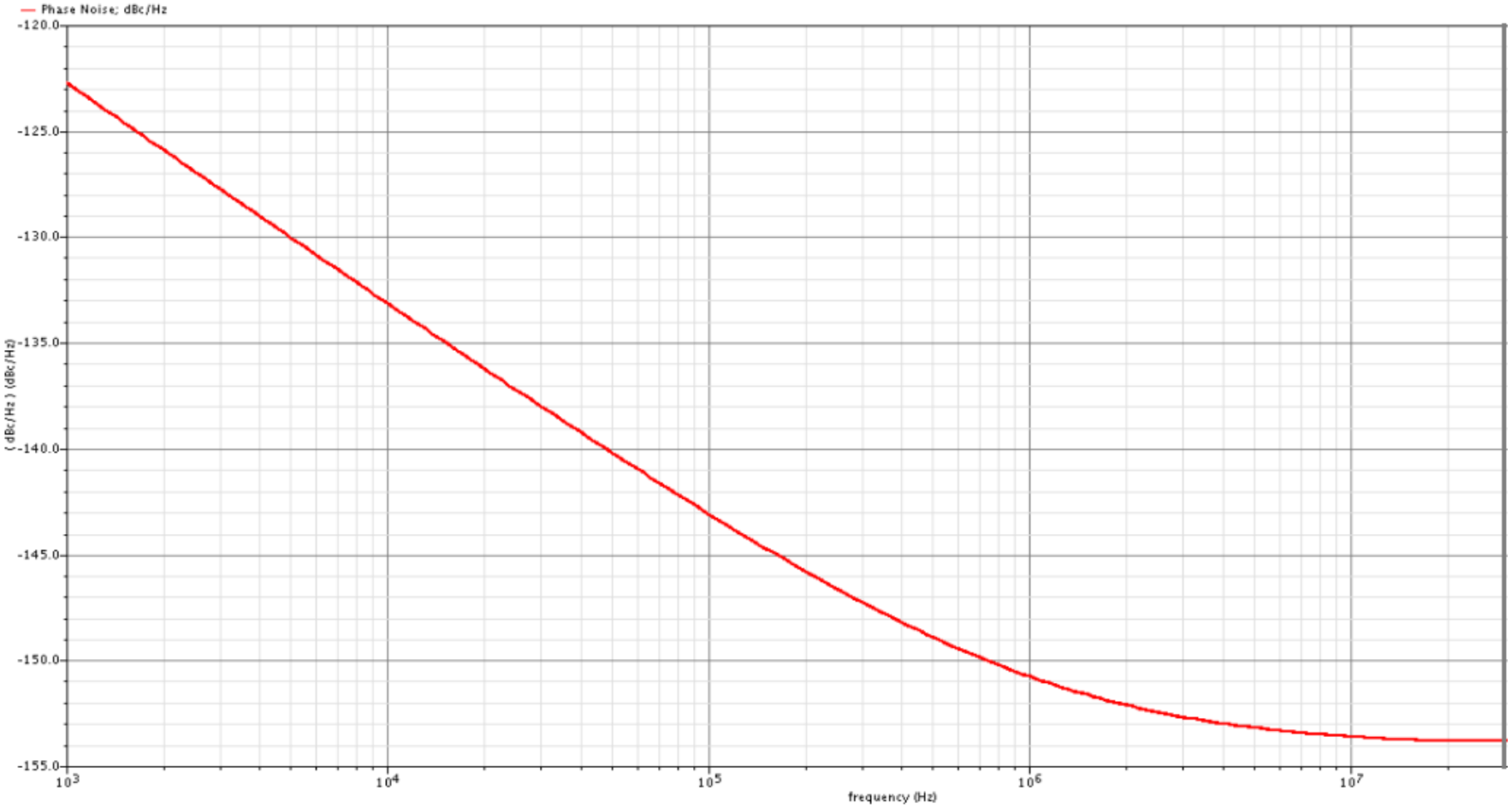
CP: Results:
Compliance Voltage



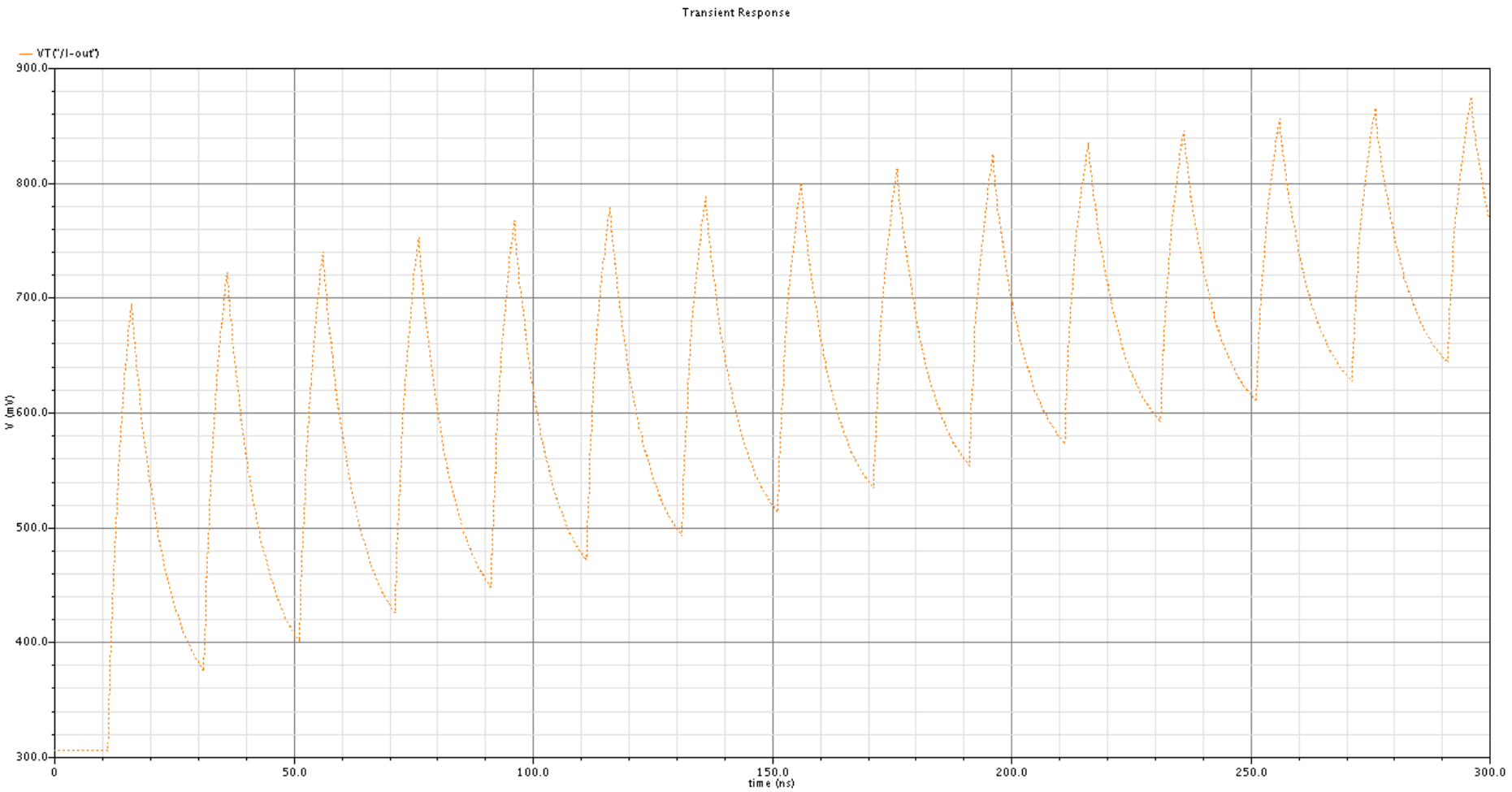
PFD/CP:
O/P Current Noise



PFD/CP:
Phase Noise



LF: Results


Transient Response
VT("/I-out")
900.0
800.0
700.0
600.0
500.0
400.0
300.0
V (mV)
0
50.0
100.0
150.0
200.0
250.0
300.0
time (ns)

Power Consumption

- Power consumption of PFD=6 µW.
- Power consumption of CP=0.52 mW.

Corners:

Using Ocean Code, it was found that:

- The PFD is robust across PVT.
- The CP is robust across PVT.

Voltage Controlled Oscillator (VCO)

Presented by : Alaa El-Din M. Hamed

VCO Outlines

- Ring VCO vs LC VCO
- Maneatis delay cell
- Differential amplifier with variable negative resistance
- DCVSL
- DCVSL-R
- DCVSL-R VCO
- DCVSL-R VCO Final
- Final Results

Ring VCO vs LC VCO

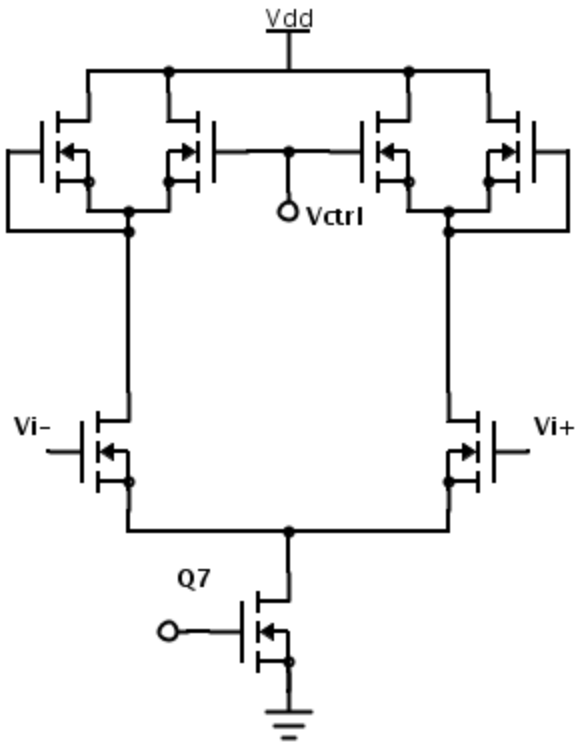
POC	Ring Oscillator	LC Oscillator
Operation	Astable	uses LC Resonator
Output Waveform	non-sinusoidal (usually square)	Sinusoidal
Output Phase noise	High	Low
Output Spectral purity	High harmonic content	Low harmonic content
Area on chip	Small	Large
Power consumption	High	Low

Ring VCO vs LC VCO

As This PLL is used a clock generator for a serial links interface, small area is the main criterion. So, a ring VCO was chosen.

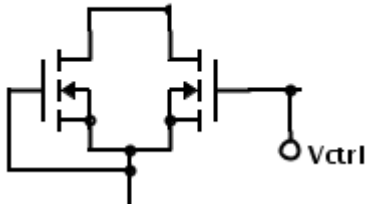
Now, Let's ahead to the three topologies which I designed, problems faced and the final design.

Maneatis delay cell



J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, Vol. 31, no. 11, pp.1723-1732, Nov 1996.

Maneatis delay cell



This is called a symmetric load as it it has two equally sized transistors to linearize the tuning sensitivity as follows:

$$R_{eff} \approx \frac{1}{g_m} = \frac{1}{\beta (V_{ctrl} - V_T)} = \frac{1}{\sqrt{2 \beta I_D}}$$

$$t_d \approx R_{eff} C_{eff} = \frac{C_{eff}}{\beta (V_{ctrl} - V_T)}$$

$$f_{osc} = \frac{1}{2 N t_d} = \frac{\beta}{2 N C_{eff}} \cdot (V_{ctrl} - V_T)$$

J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, Vol. 31, no. 11, pp.1723-1732, Nov 1996.

Maneatis delay cell

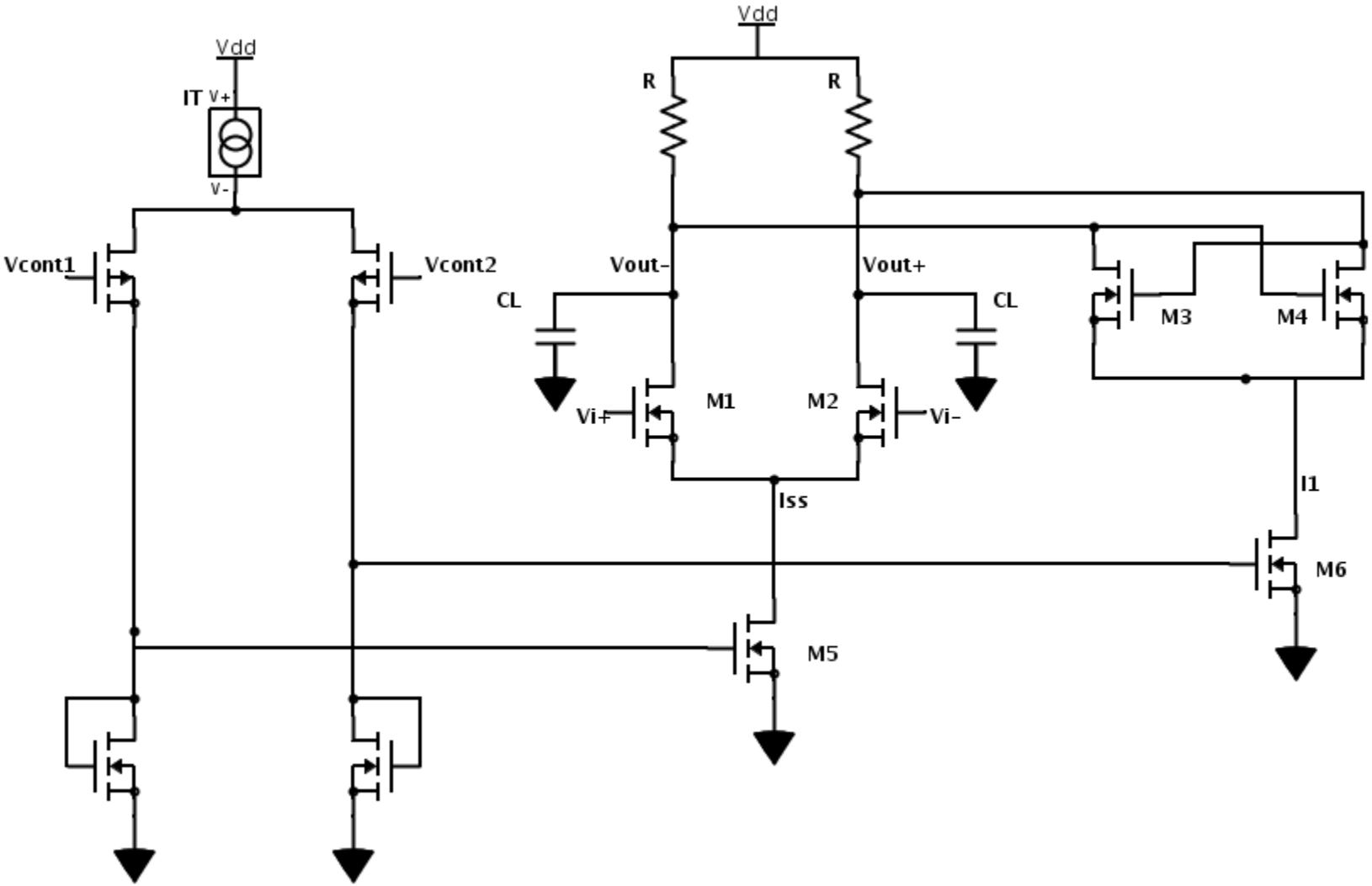
Problems that I faced during designing this topology:

1. Low supply voltage.
2. Short Channel effects (mainly small output resistance) limited the gain requiring large number of delay cells consuming extra power and limiting the speed considerably.

So, I headed for the next topology.

J. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, Vol. 31, no. 11, pp.1723-1732, Nov 1996.

Diff. amp. with negative res.



B. Razavi, " Oscillators," *Design of CMOS Analog Integrated Circuits*

Diff. amp. with negative res.

$$t_d \approx R_{eff} C_{eff}; R_{eff} = R - \frac{1}{g_{m,neg}}$$

$$g_{m,neg} = \sqrt{2\beta I_1}; I_1 = \beta_{cont2}(V_{cont2} - V_T)^2$$

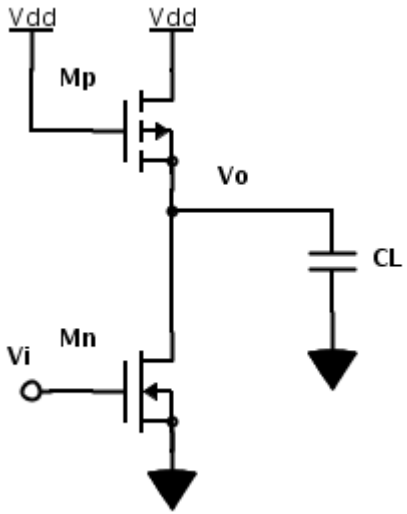
$$g_{m,neg} = \sqrt{2\,\beta\,\beta_{cont2}}\,(V_{cont2} - V_T)$$

$$f_{osc} = \frac{1}{2N t_d} = \frac{\beta}{2N C_{eff}} \cdot \frac{1}{R - \sqrt{2\,\beta\,\beta_{cont2}}\,(V_{cont2} - V_T)}$$

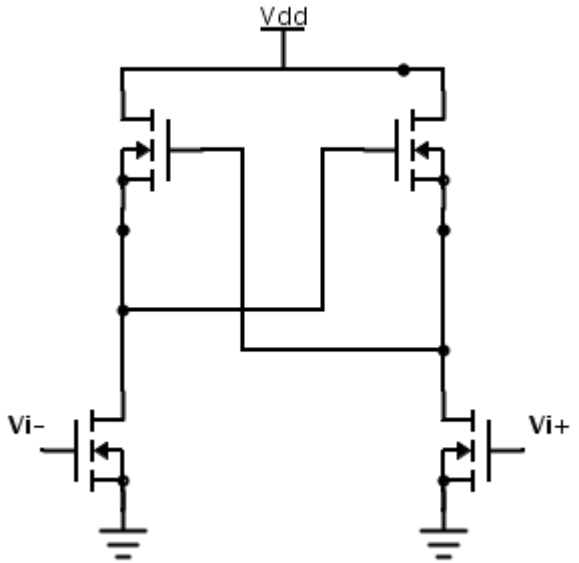
Diff. amp. with negative res.

<u>Problem faced me during designing this topology,</u> R was small (due to high frequency) requiring high $g_{m,neg}$ and $g_{m,i/p}$ (to be able to tune VCO for required frequency range) so when increasing I_1 and I_{ss}, IR drop increased leading to less V_{od} for cross coupled MOSFETs entering subthreshold region.

DCVSL



Pseudo nMOS inverter



DCVSL (**D**ifferential **C**ommon **V**oltage **S**witch **L**ogic)

A. Mason. ECE 410. Class Lecture, Topic: "Advanced Digital", College of Engineering, Michigan State University, Spring, 2008

DCVSL

Advantages:

Rail-to-rail swing.

Nearly no static power consumption

Disadvantages:

Asymmetric transitions.

Solution:

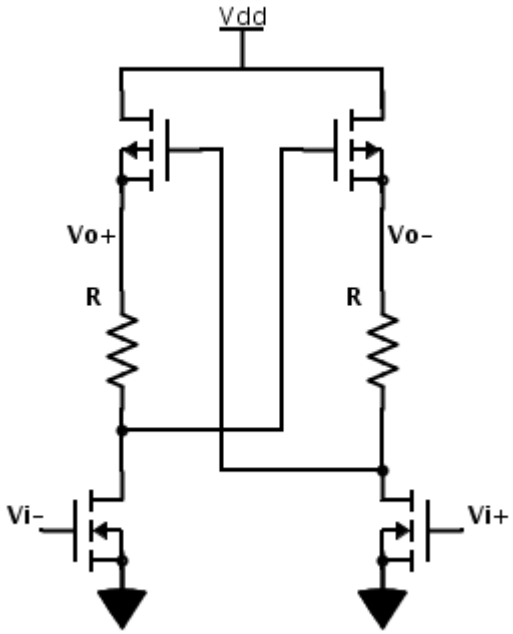
Decrease t_{PLH} .

DCVSL-R

Introduce extra IR drop such that the voltage of gates of pMOS decrease faster leading to less t_{PLH} .

Also, this will not affect t_{PHL} as long as $R < R_{nMOS,on}$.

So, R is designed for symmetric transitions.

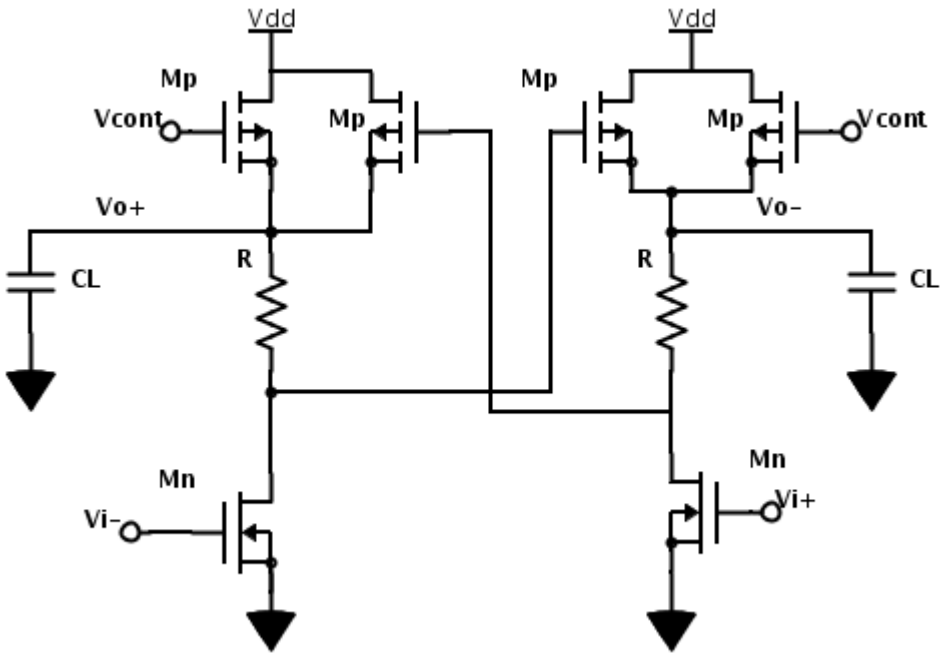


D. Turker, S. Khater, E. Sinencio, " A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, no. 6, pp.1225-1238, Jun. 2011.

DCVSL-R VCO

Here, K_{VCO} is negative as current increases as V_{cont} decreases.

Also, as voltage

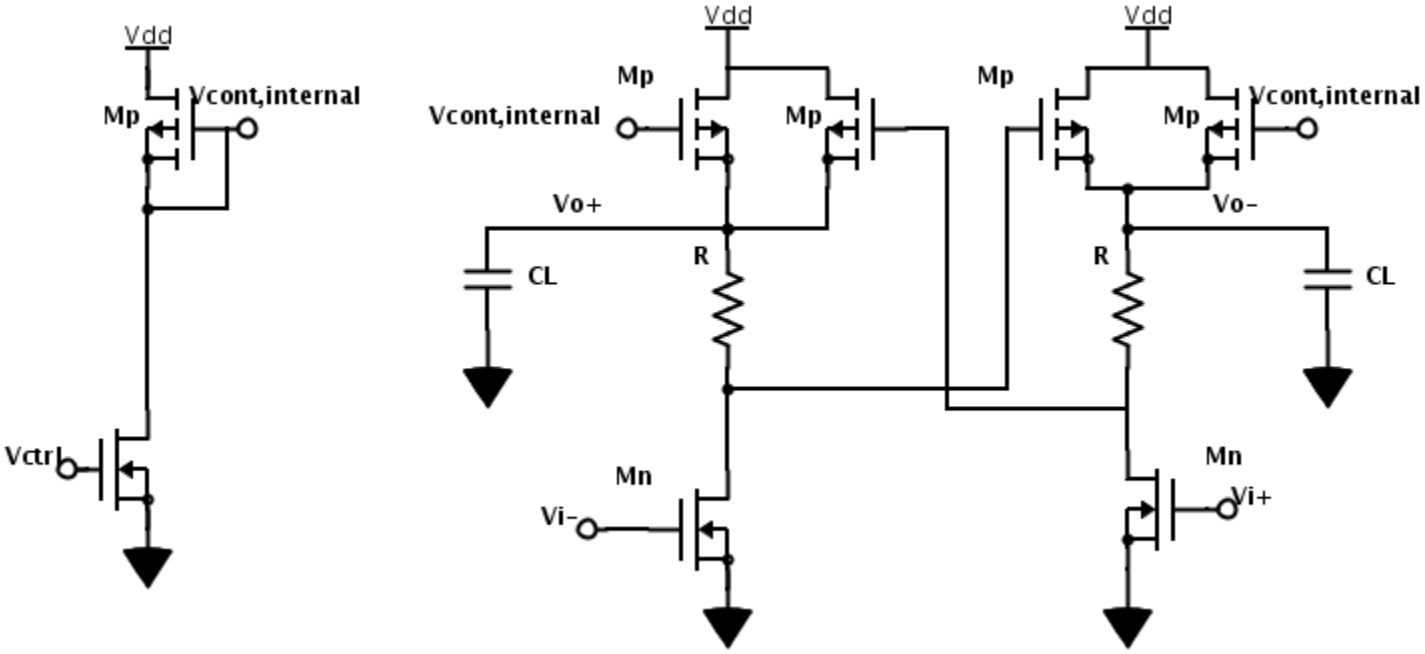


tuning is limited by the V_{CM} of output (nearly 500 mV) making K_{VCO} too high which is undesirable.

D. Turker, S. Khater, E. Sinencio, " A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, no. 6, pp.1225-1238, Jun. 2011.

DCSL-R VCO Final

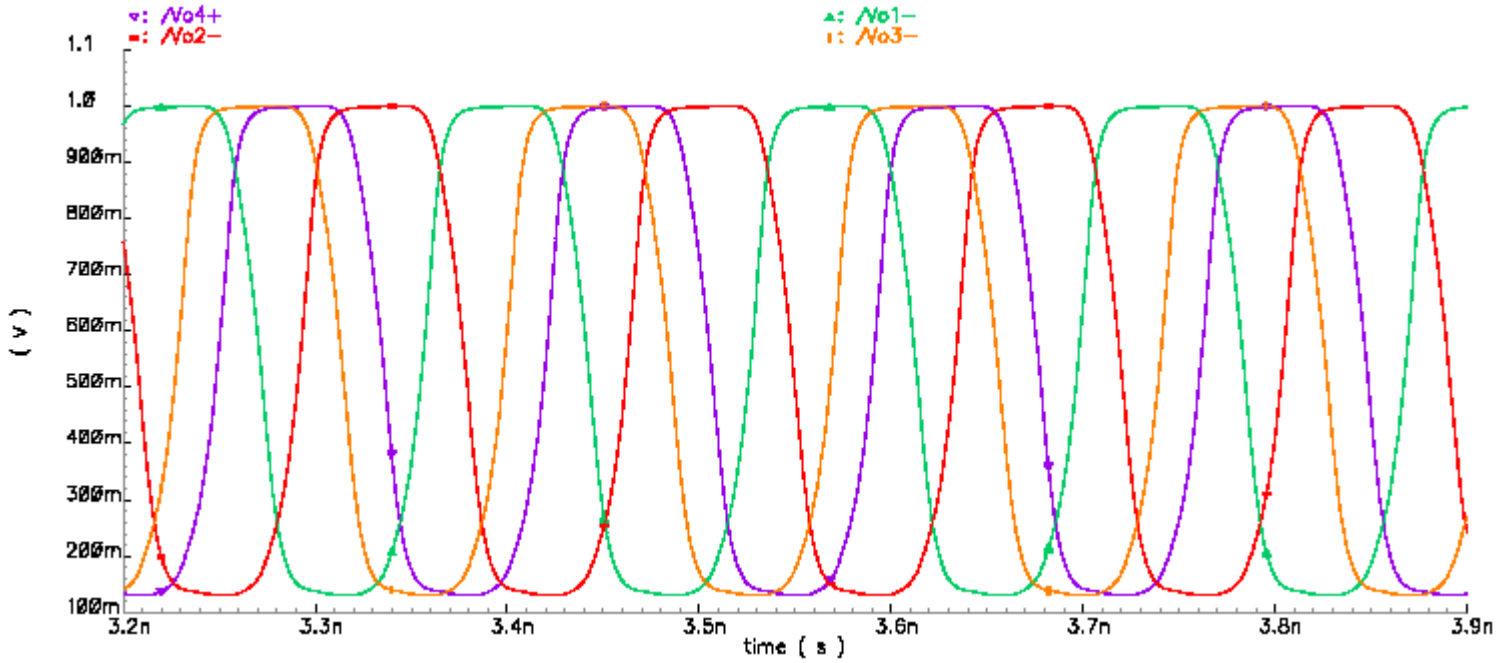
Here is the solution.



K_{VCO} is now positive as required in addition to that the tuning voltage range now increases which leads to less K_{VCO}.

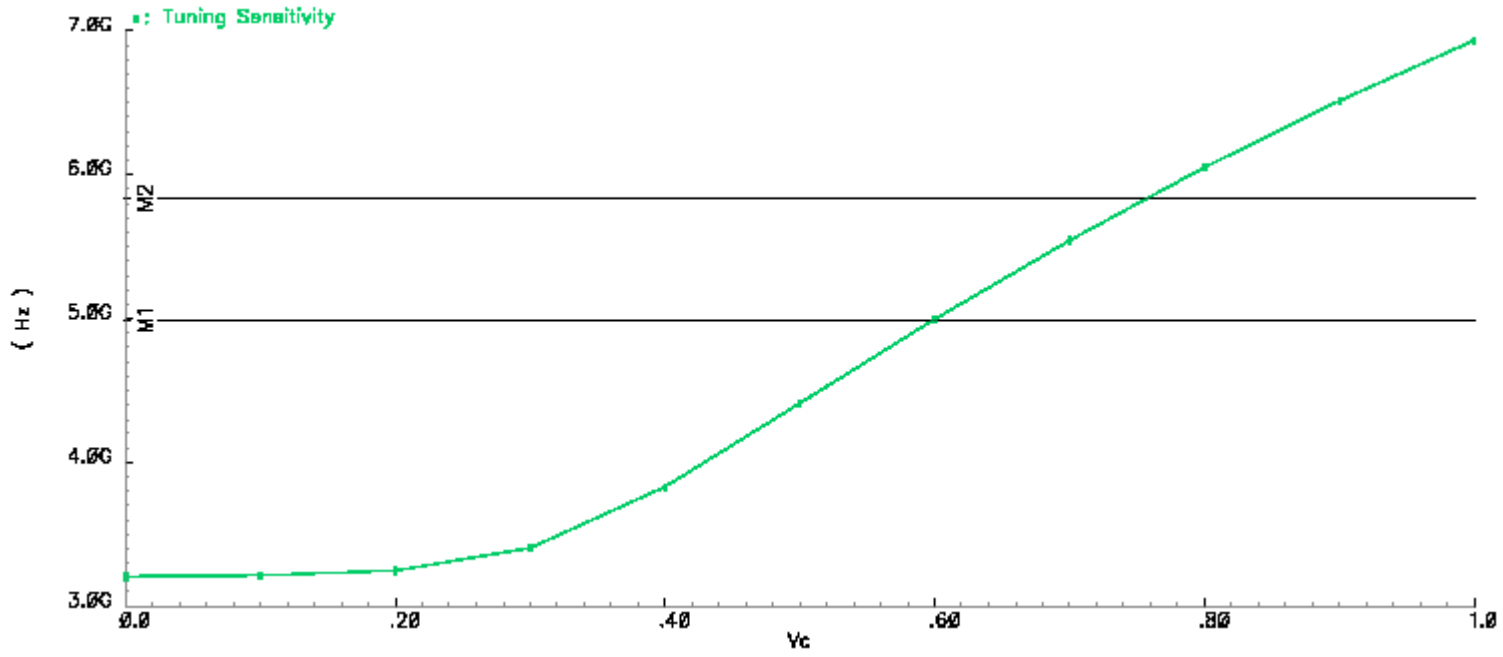
D. Turker, S. Khater, E. Sinencio, " A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, no. 6, pp.1225-1238, Jun. 2011.

Final results



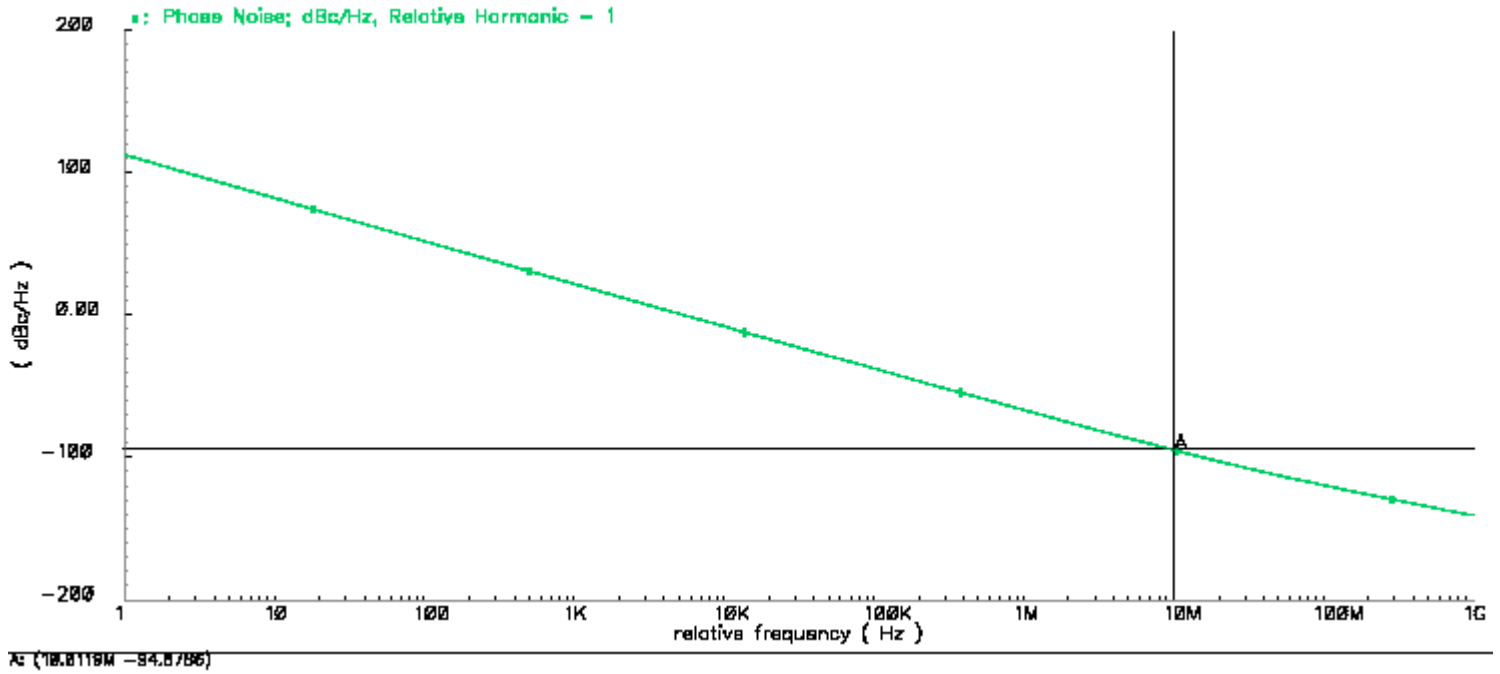
Output Waveforms (Vo1- and Vo3- are in quadrature)

Final results



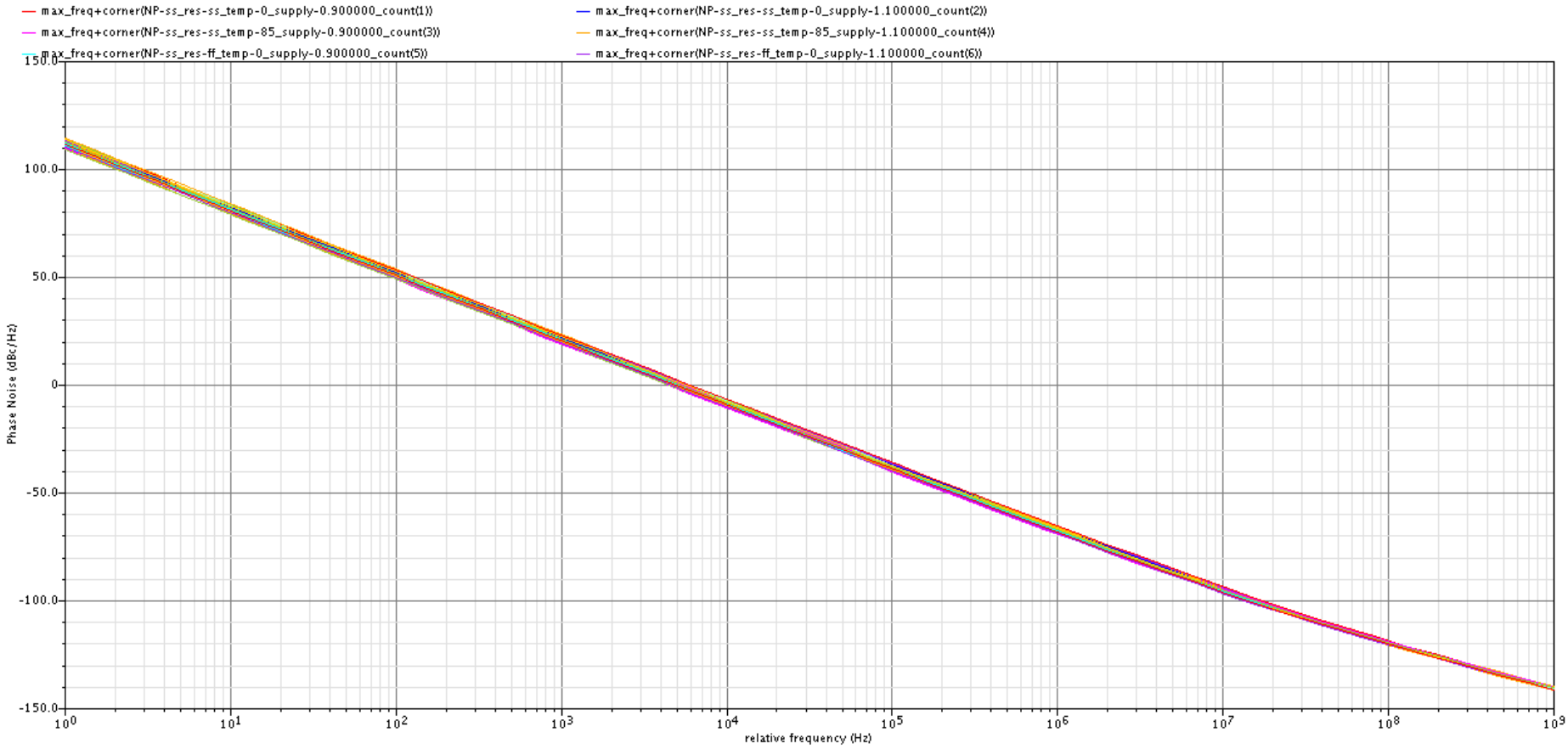
K_{VCO} = 5.3193 GHz/V.

Final results



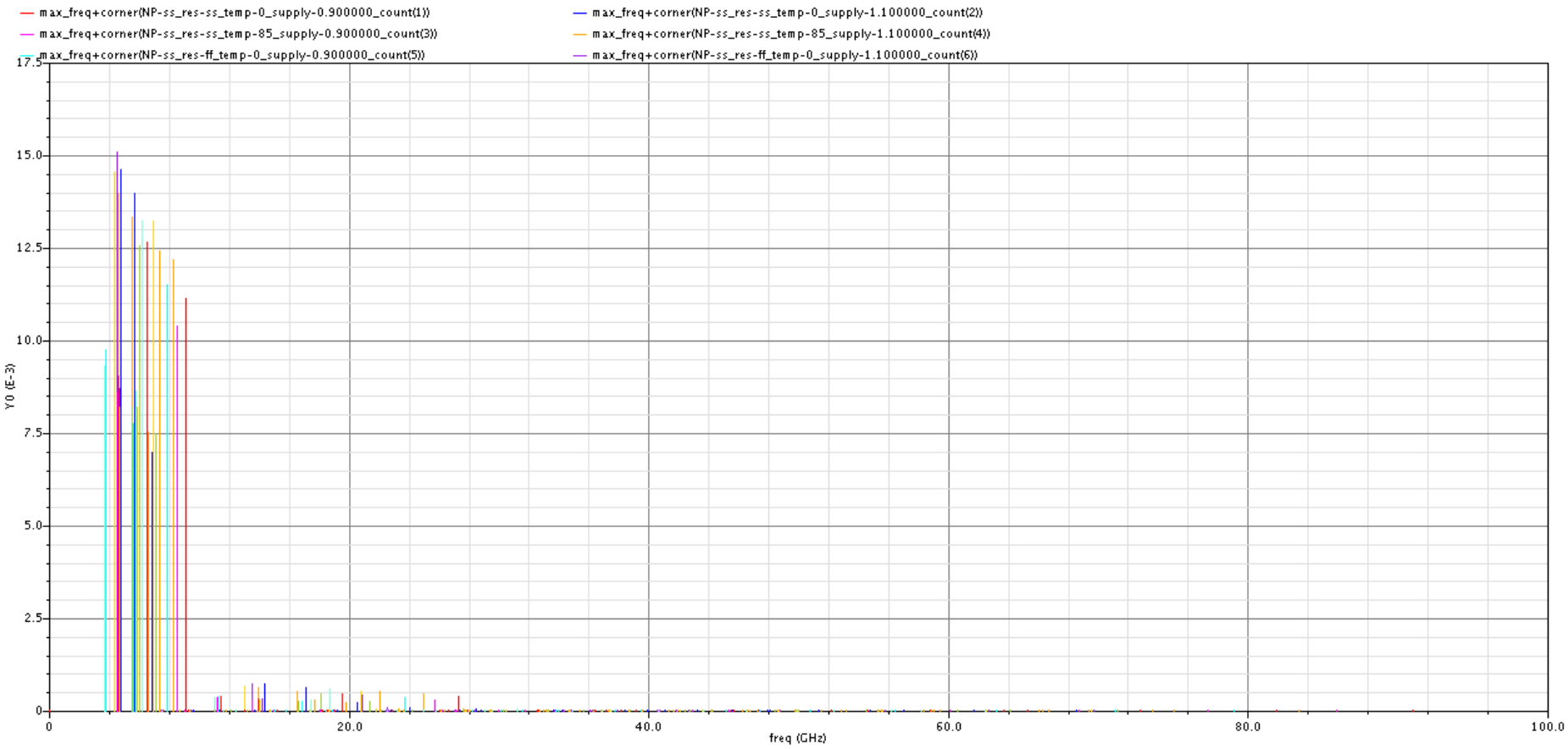
Phase noise = -95 dBc/Hz at 10 MHz offset

Final results



Phase noise across corners

Final results



Output Power across corners (worst case is 15 mW)

Dividers

Presented by : Basma Atef

Outlines

- Block diagram
- Circuit

  -TSPC

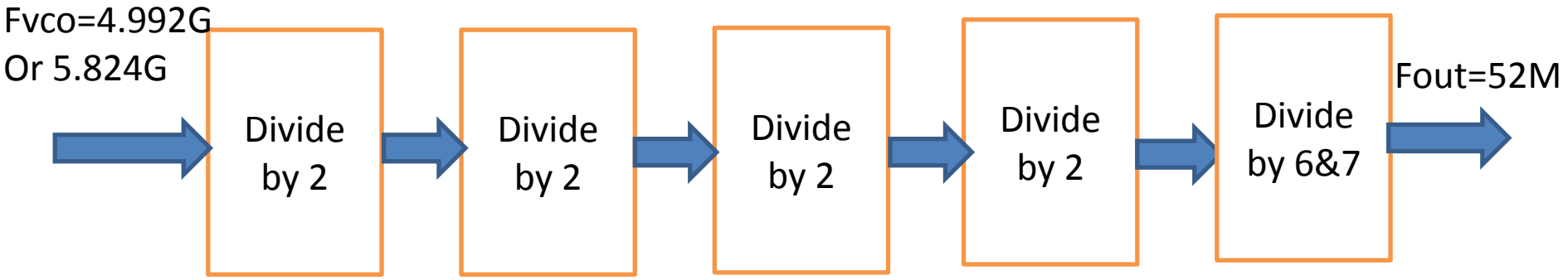
  -Static flip flop

  -Divide by 6&7

  -Divide by 7

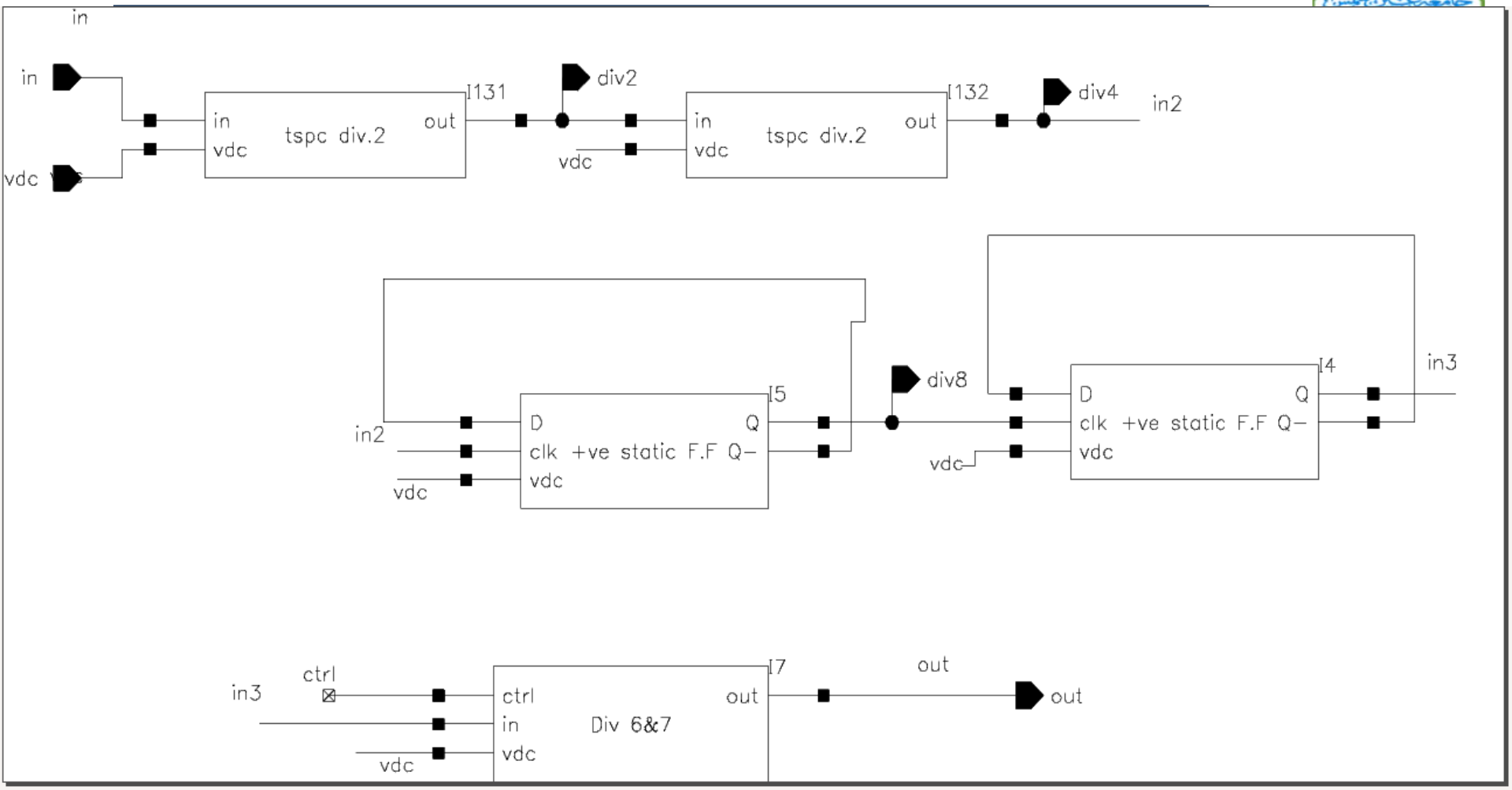
  -Divide by 6
- Simulations & Results

Block Diagram

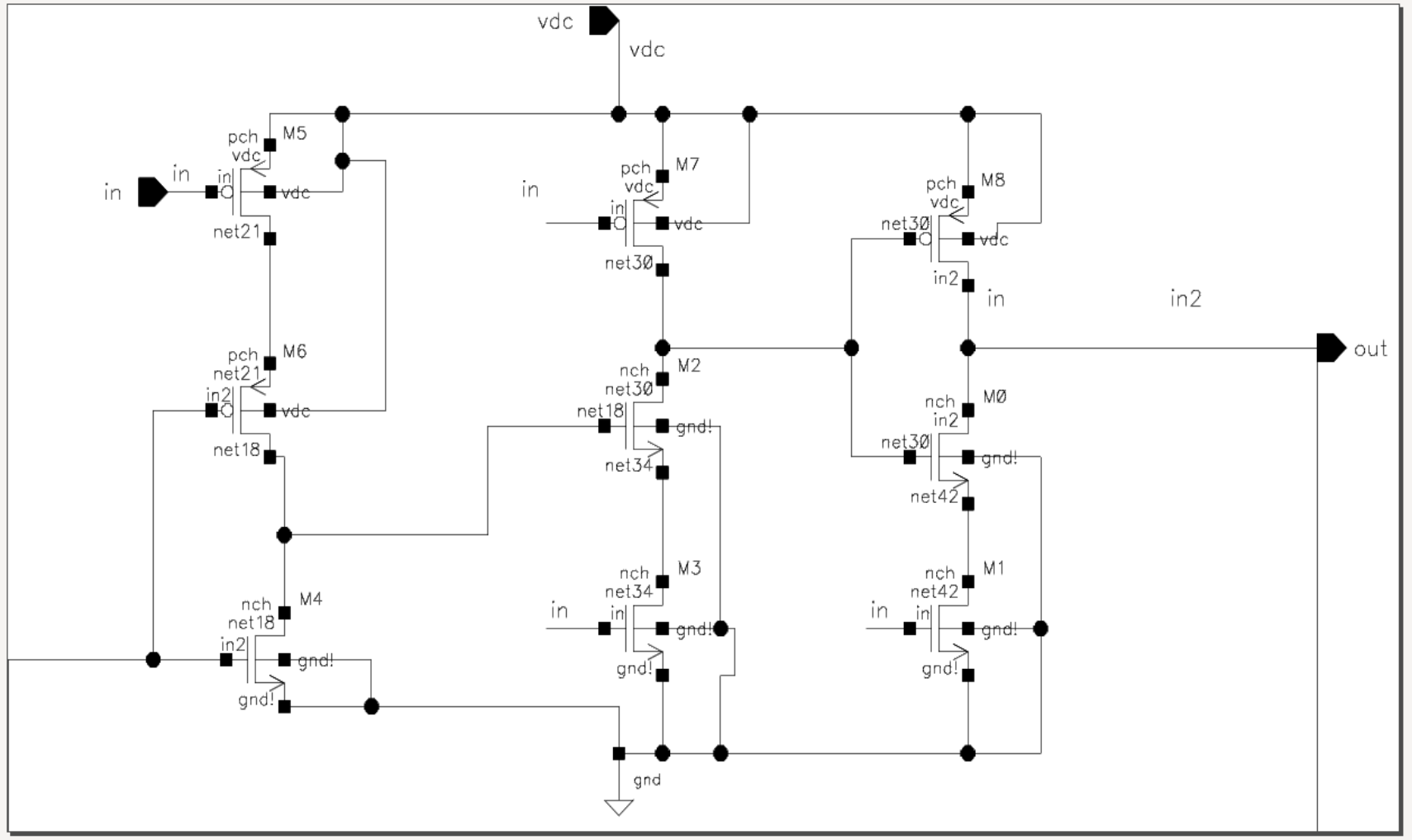


Division ratio =96 or 112

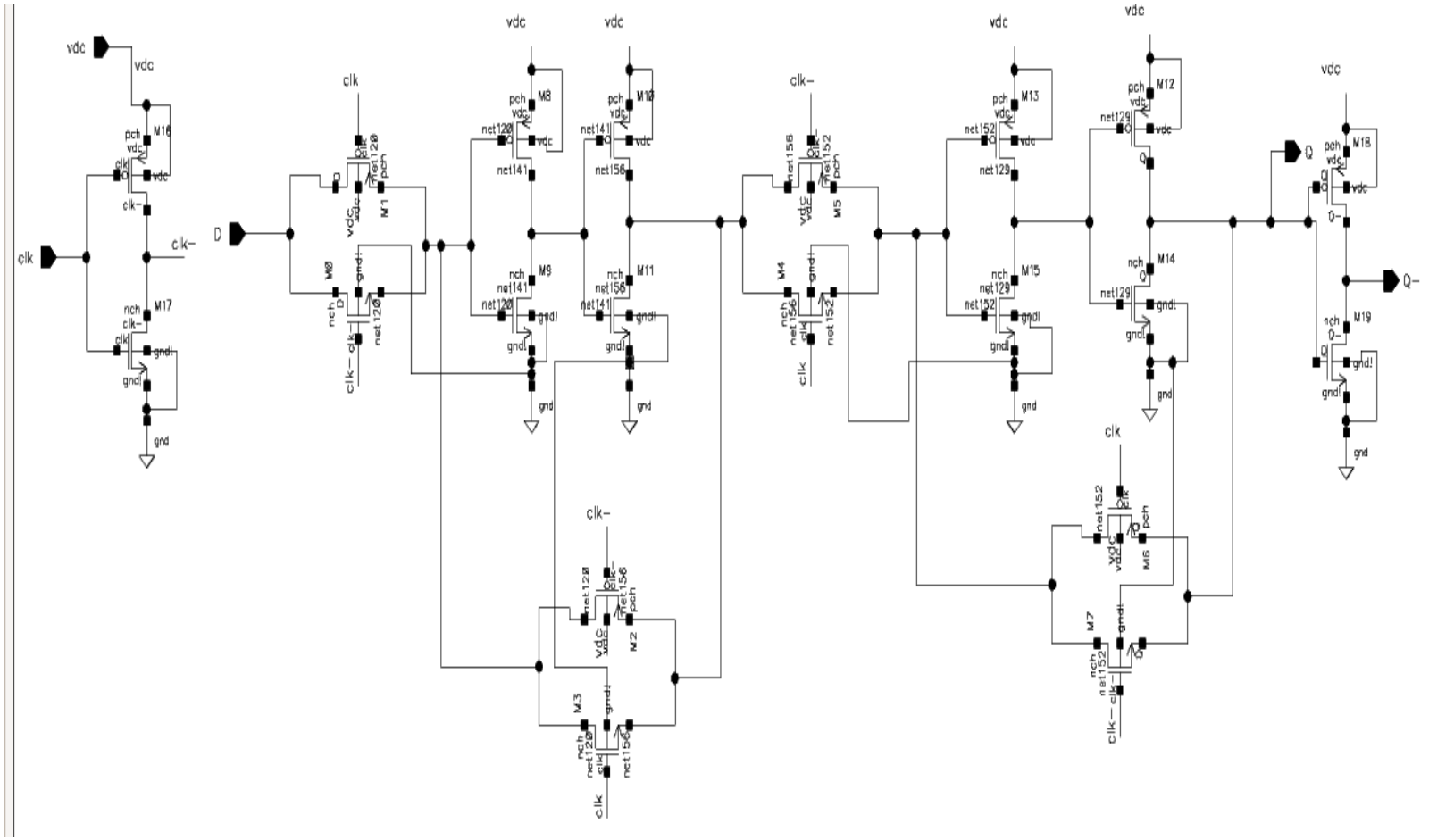
Circuit and schematic



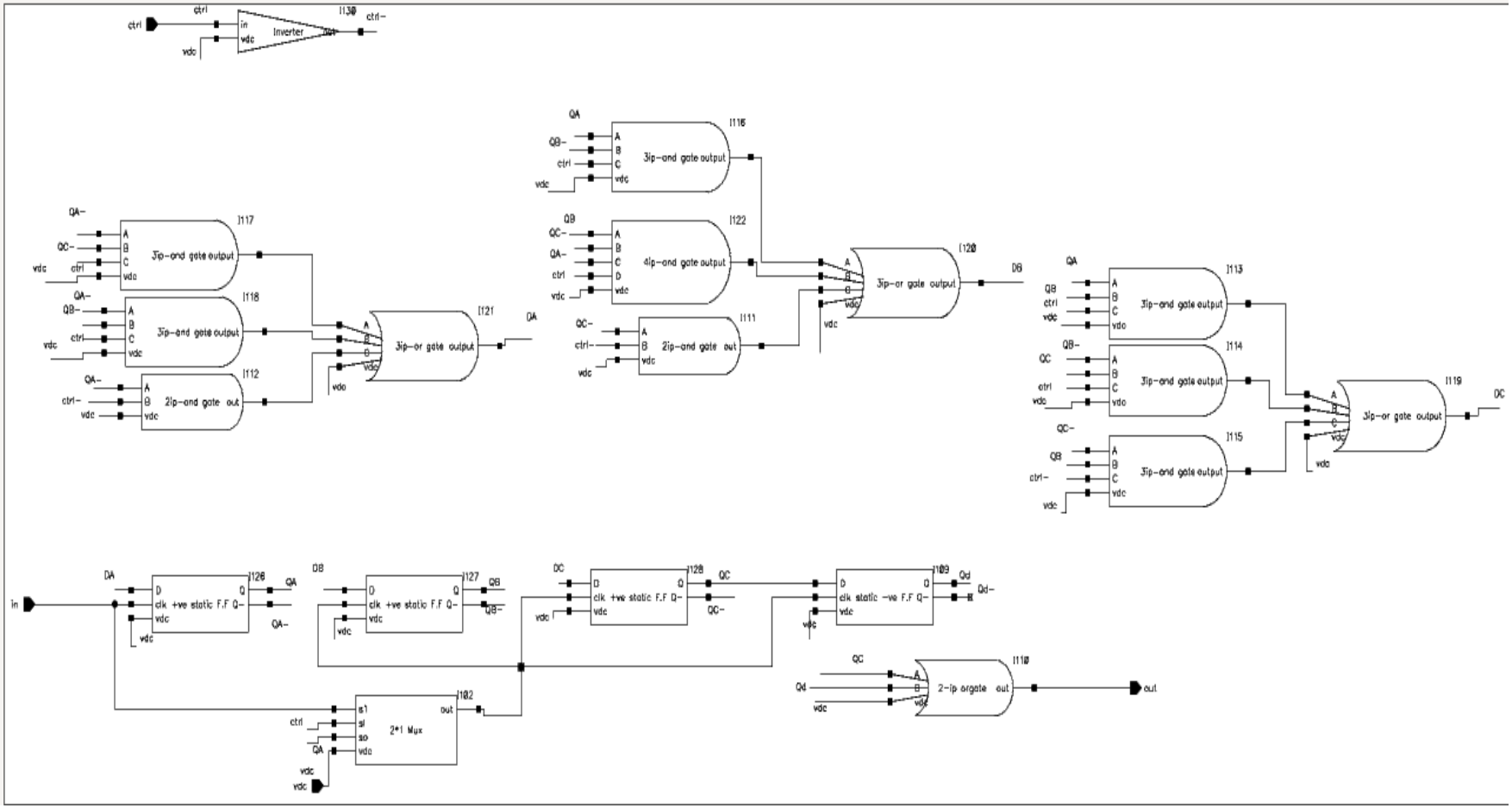
TSPC circuit



Static flip flop circuit

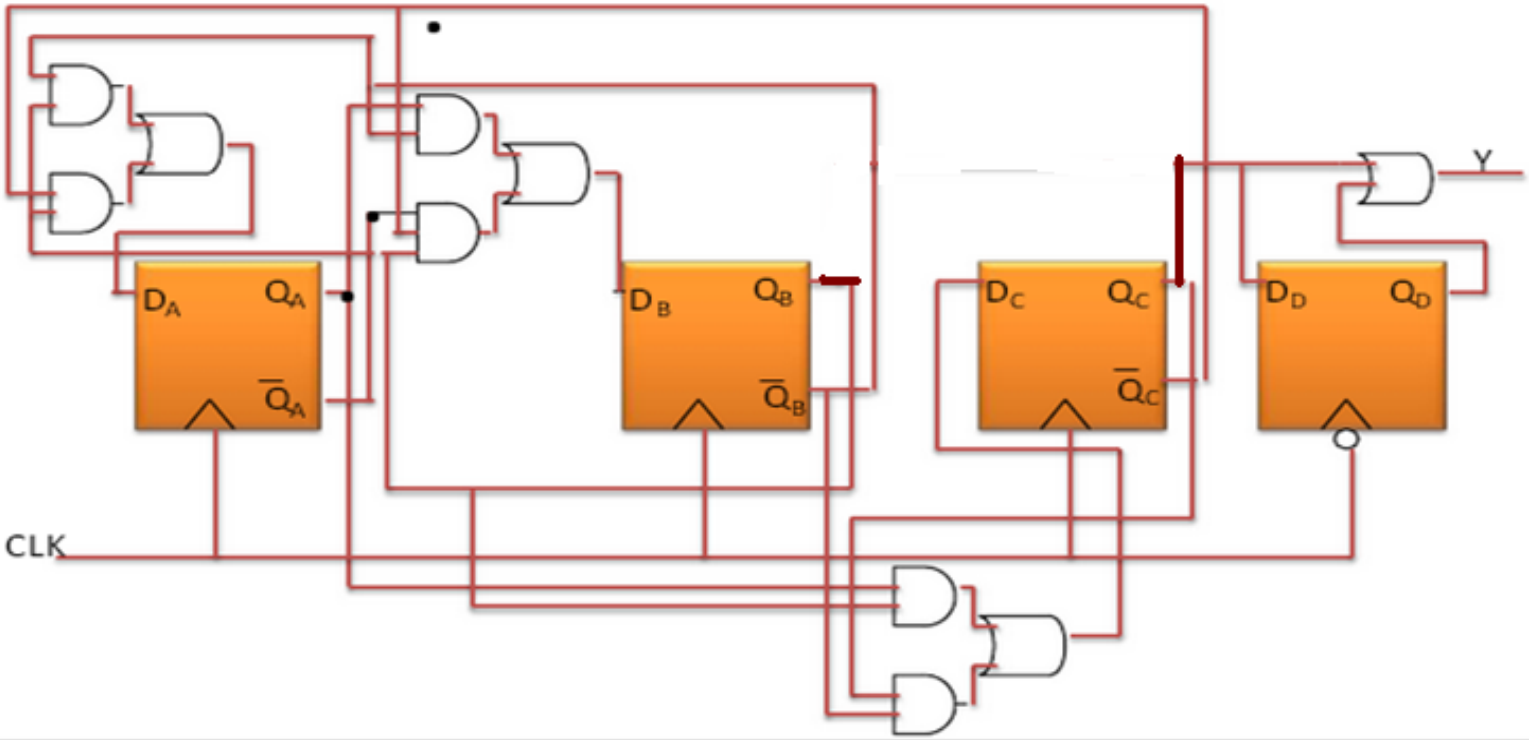


Divide by 6 & 7 circuit

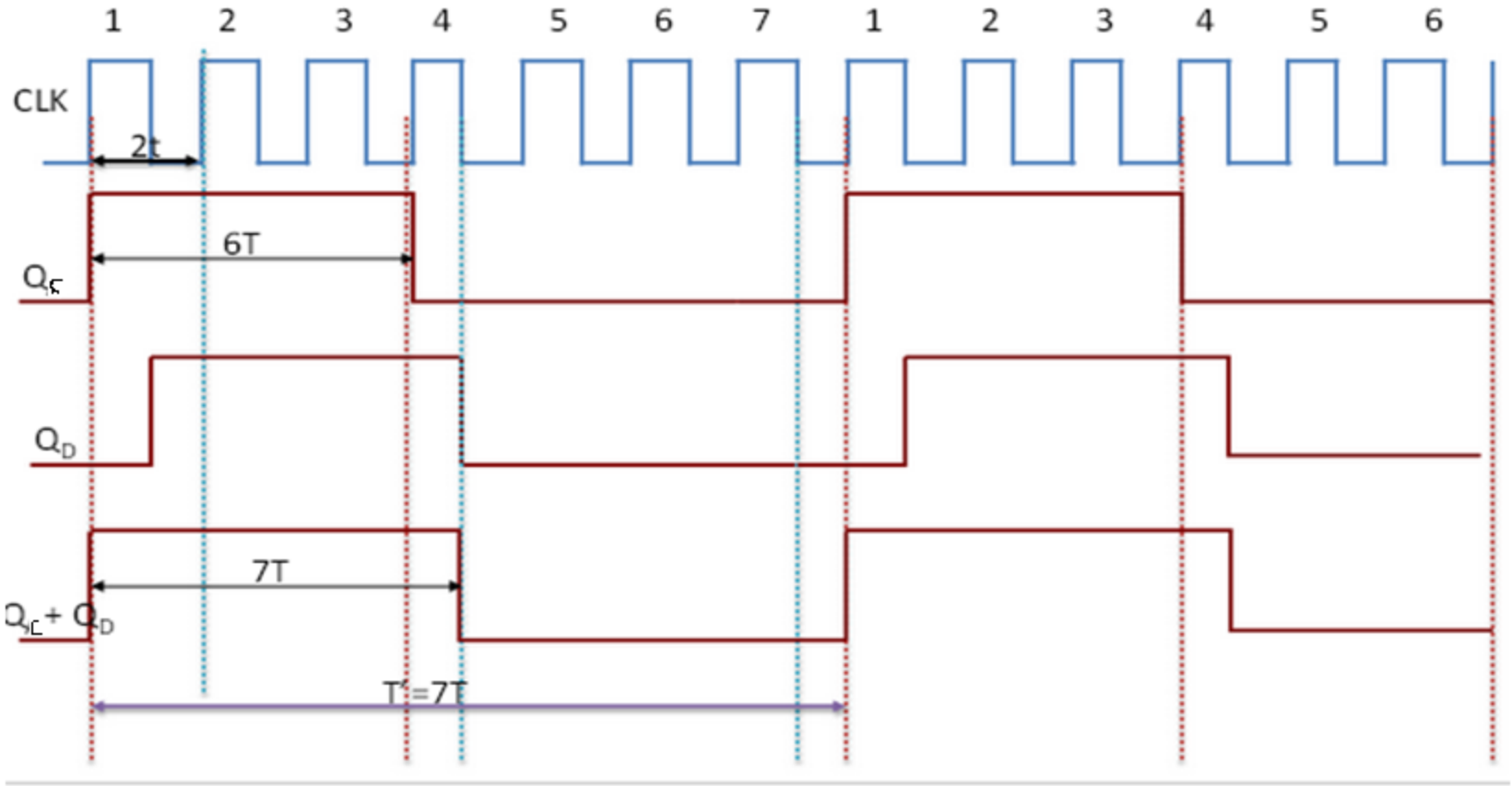


Divide by 7 circuit

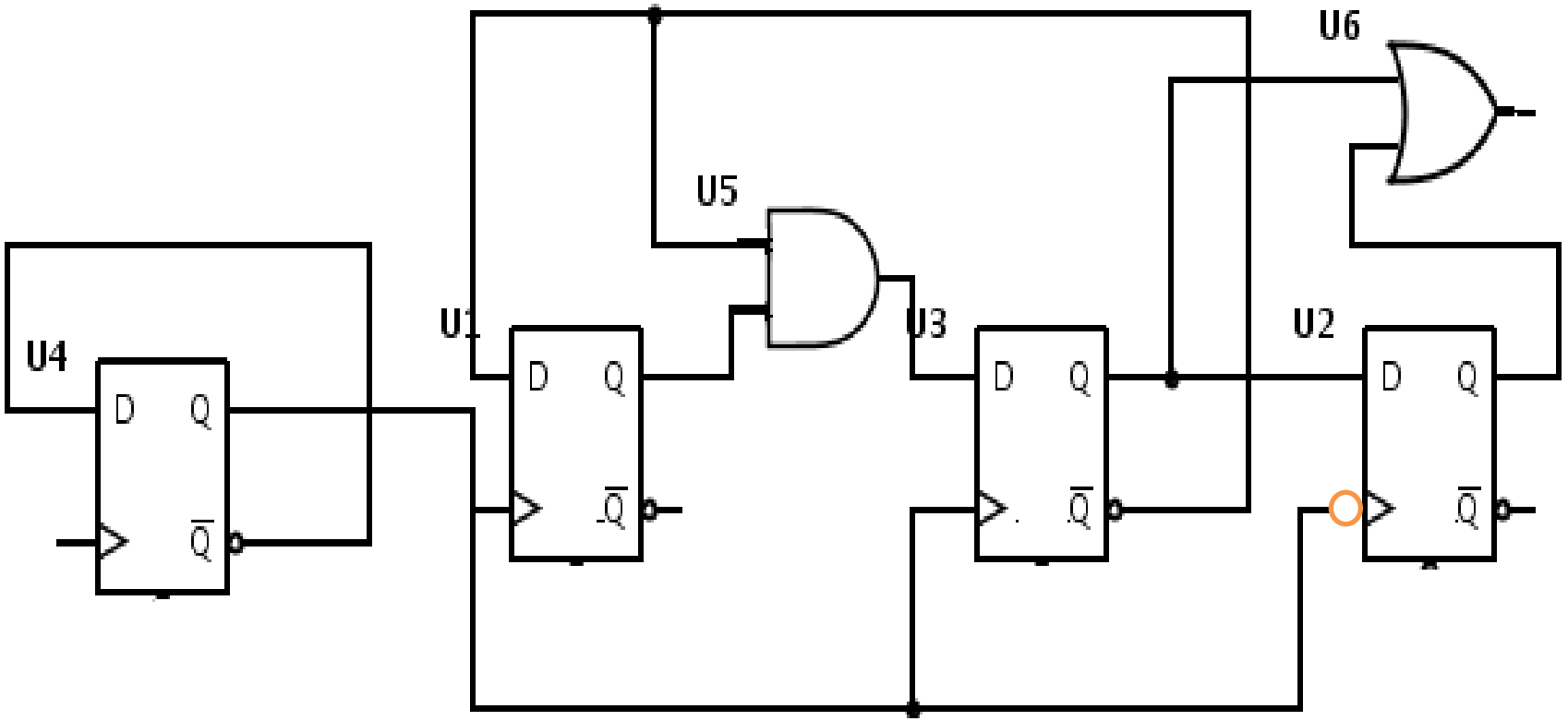
Divide by 7 counter Logic Diagram



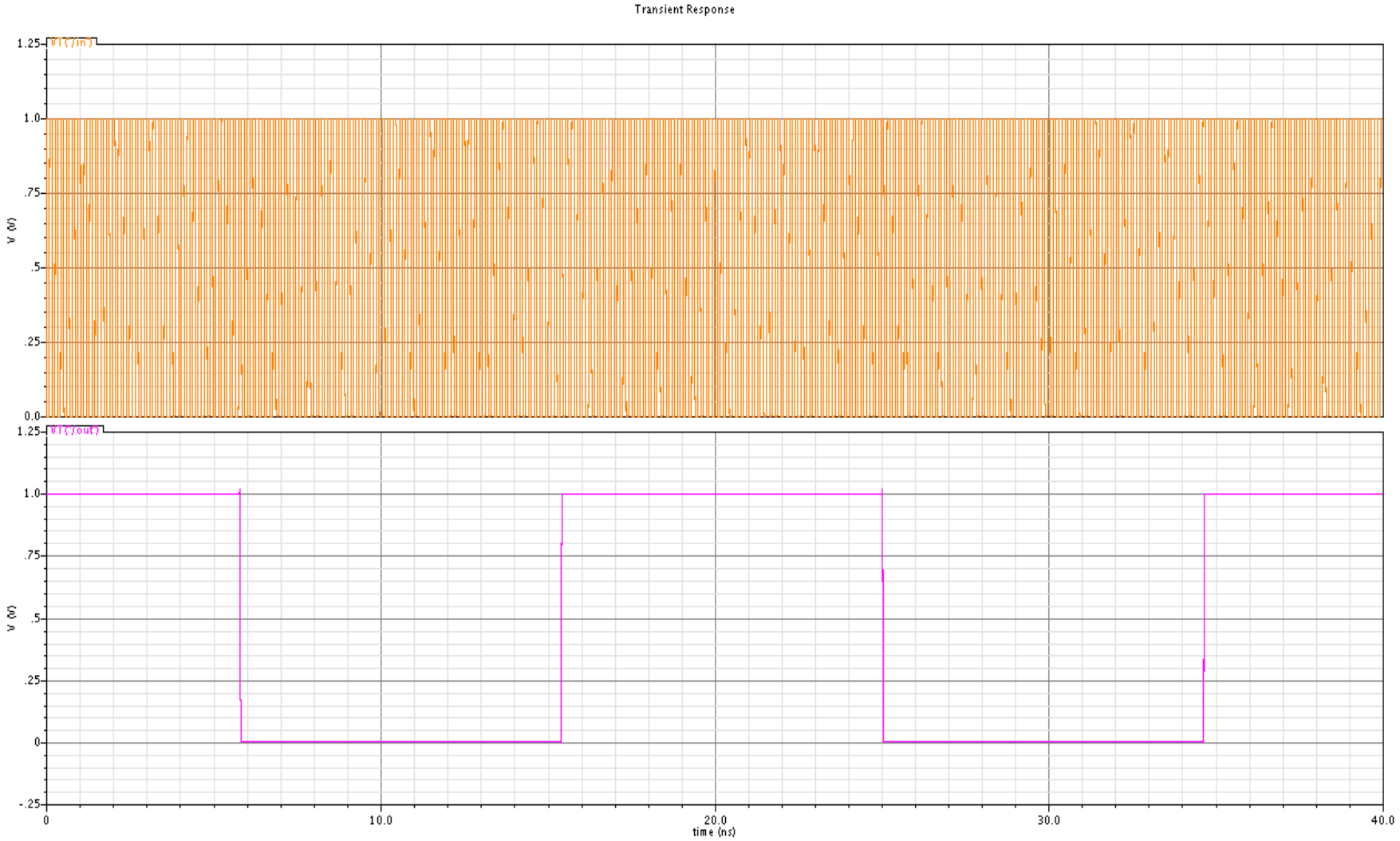
Divide by 7 circuit



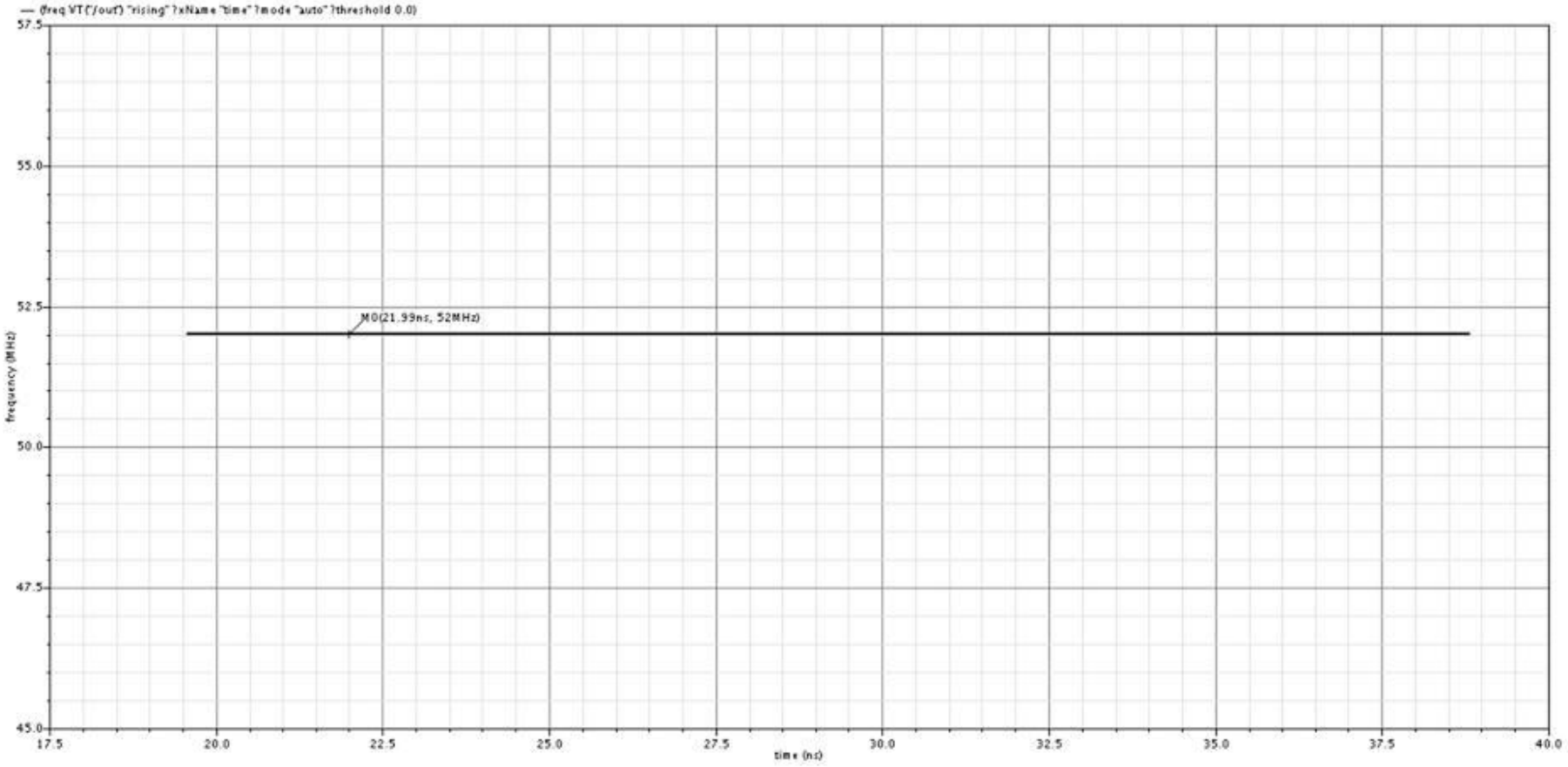
Divide by 6 circuit



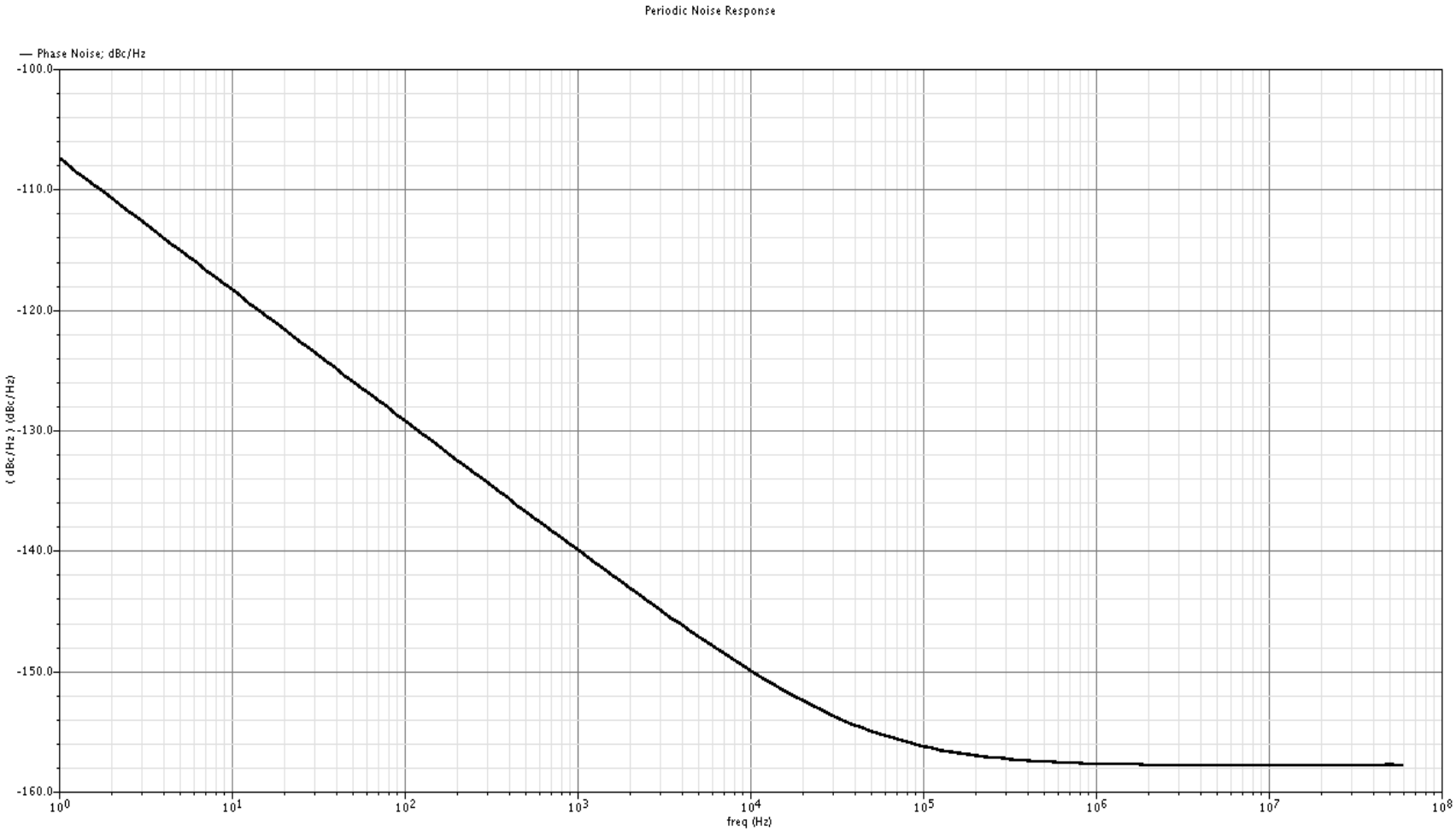
Simulations & results



Simulations & results



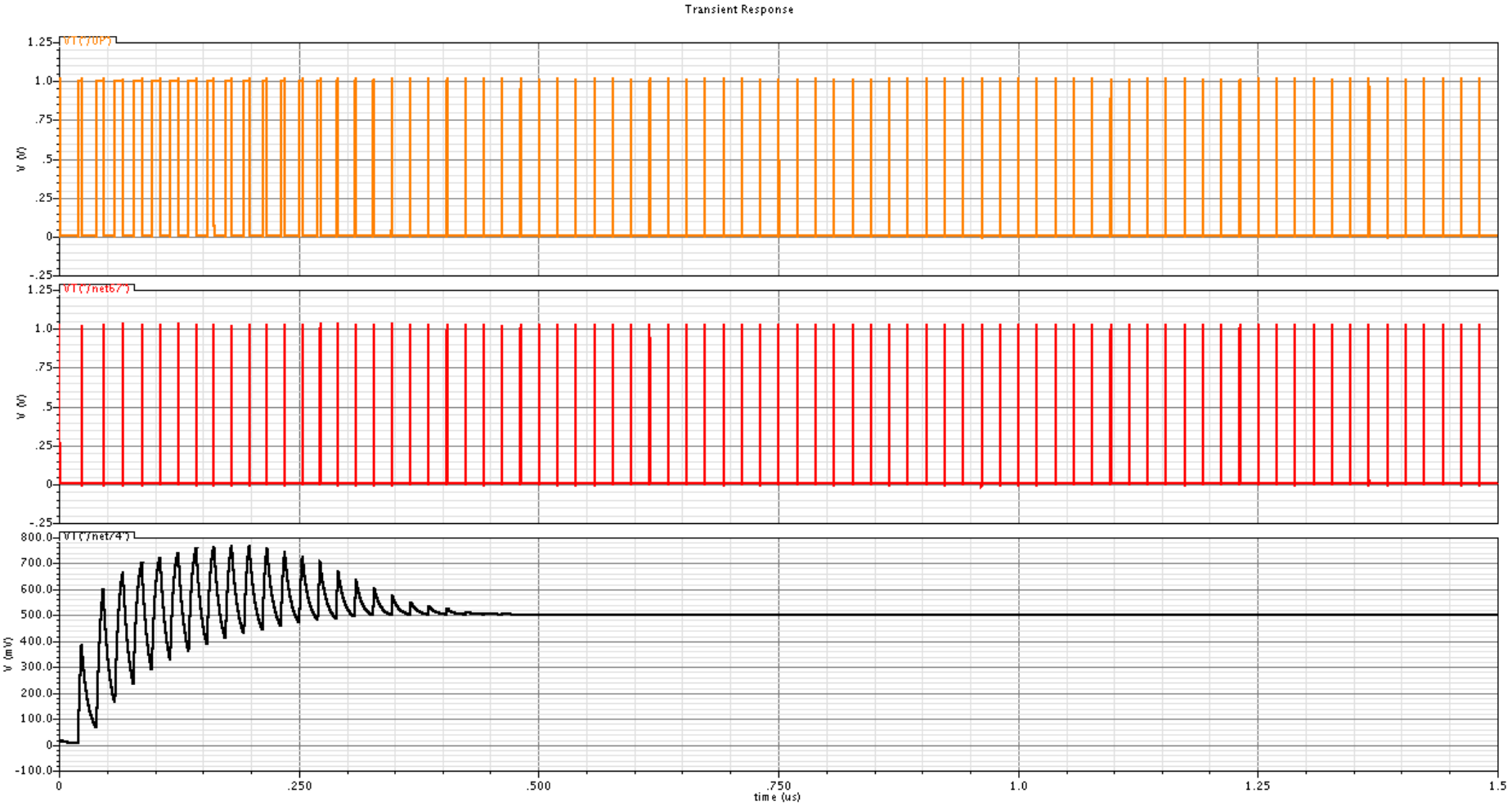
Simulations & results



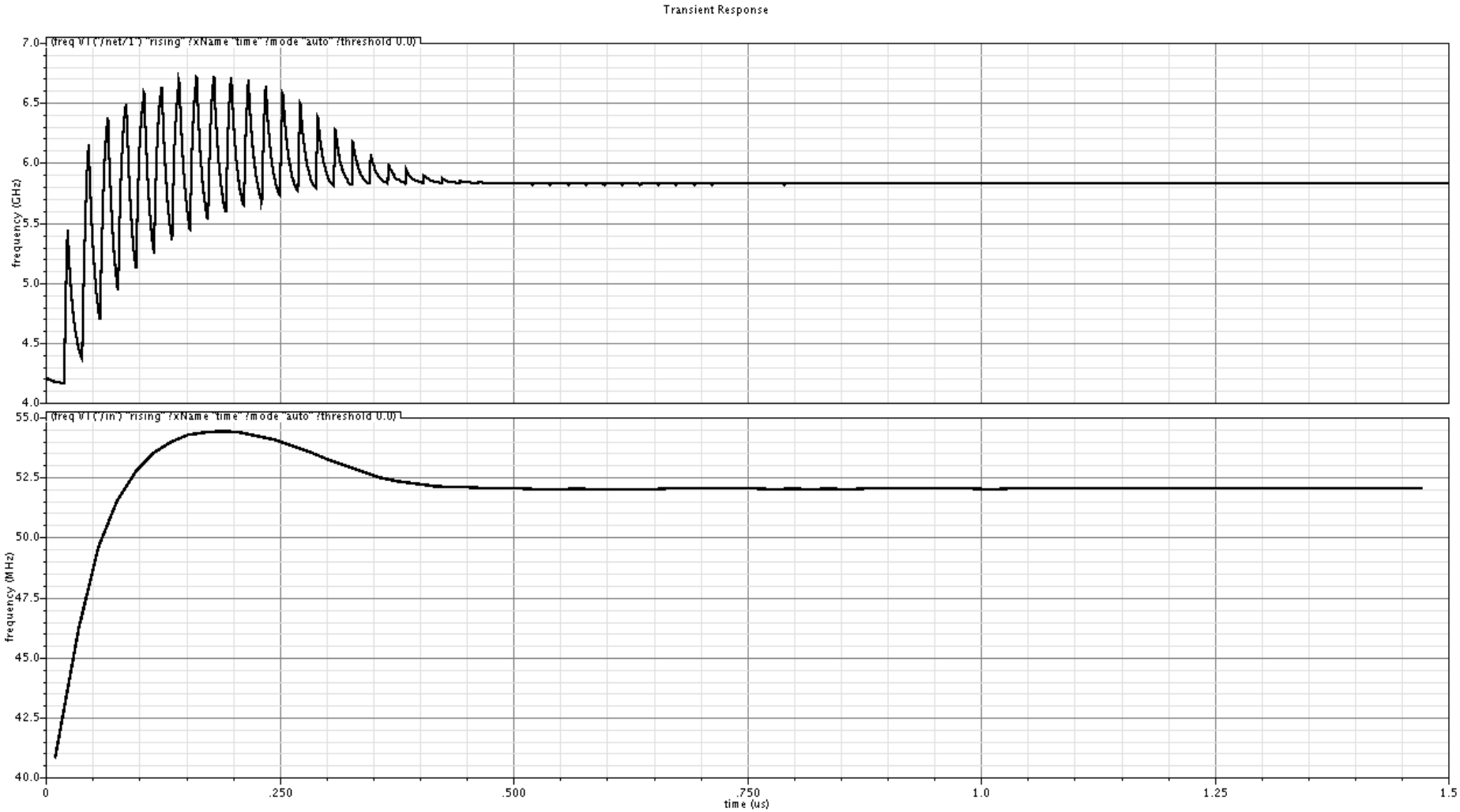
Simulations & results

- Power consumption = 44.7uw.
- Circuit is robust across corners.

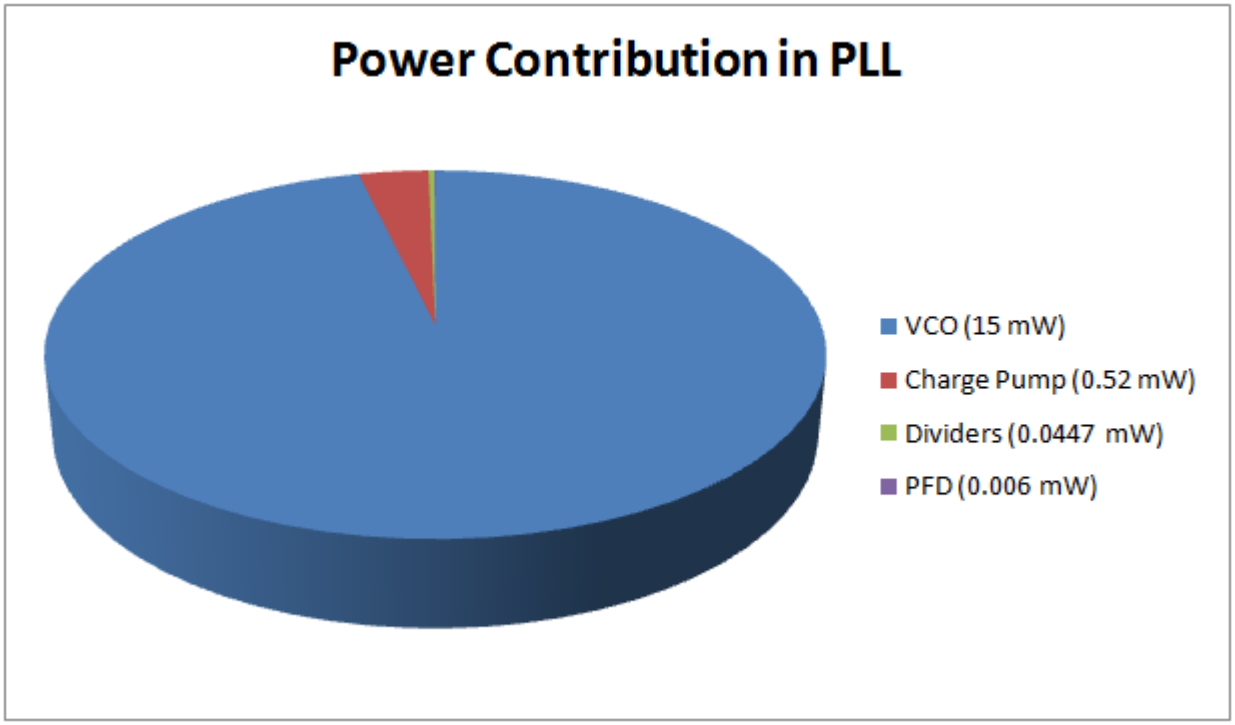
The Locked Loop



The Locked Loop



The Locked Loop



The Locked Loop:
Open Loop