



# MODELING THE PHASE STEP RESPONSE OF BANG-BANG DIGITAL PLLS

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*Moataz Abdelfattah*

**Supervised by:**

**AUC**

Prof. Yehea Ismail  
Dr. Maged Ghoniema

**Intel**

Dr. Mohamed Abdel-moneum  
*(Industry Mentor)*

# Outline

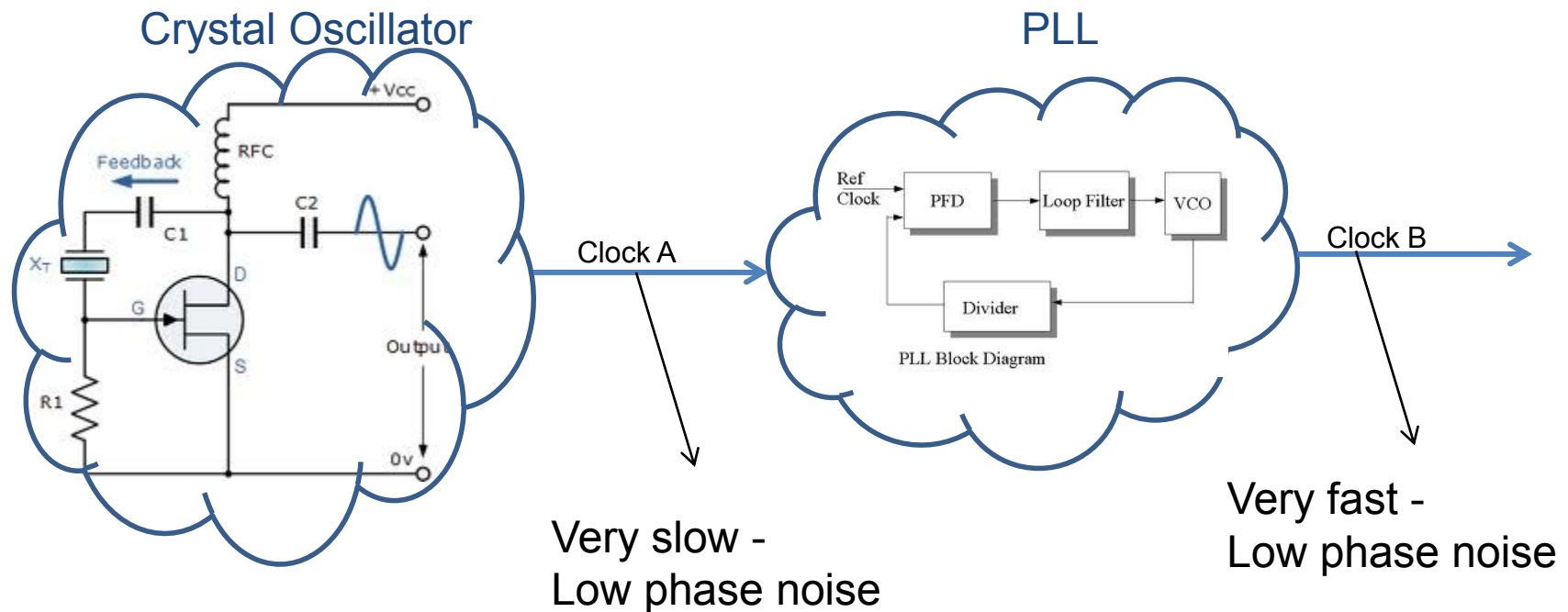
- Introduction
- Proposed Modeling Methodology
- BB-ADPLL System
- Proposed Techniques for Enhanced System Response
- Conclusion & Future Work

# Outline

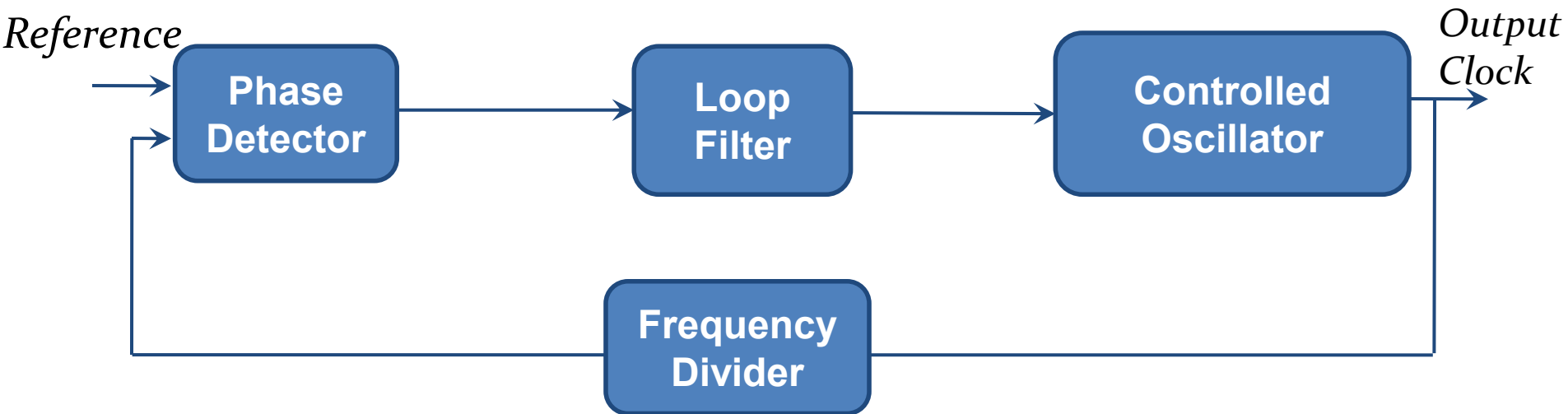
- Introduction
  - **What is BB-PLLs**
  - Motivation
  - Scope of work & Methodology
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# What is a PLL?

- A circuit responsible for **generating clock** signal for electronic devices



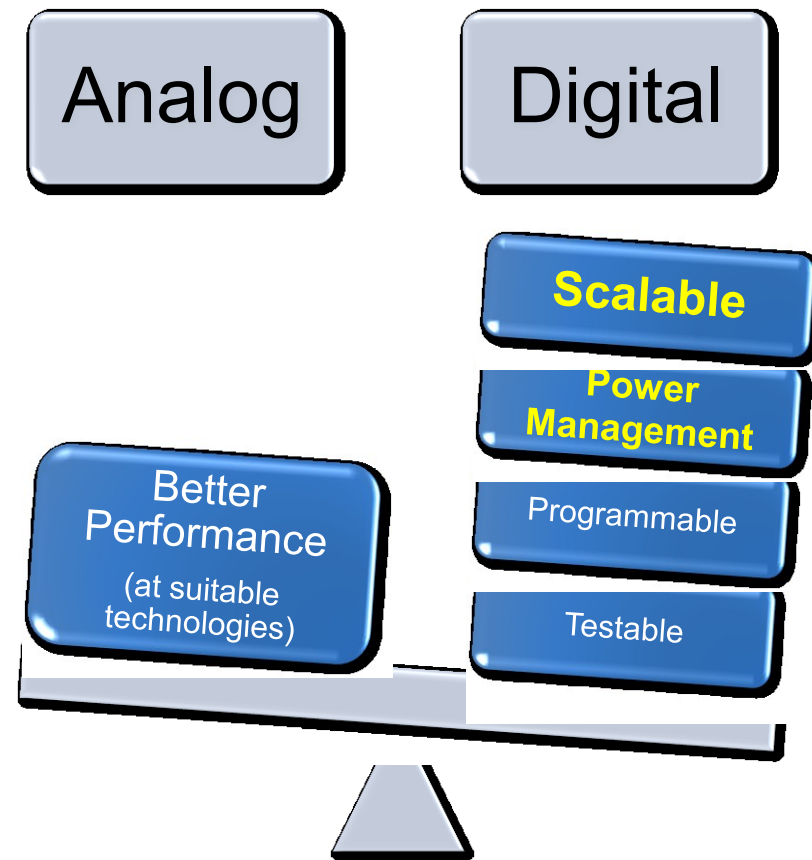
# PLL Operation



- Negative feedback system
- Compares reference to a divided version of output clock
- Guarantees purity through –ve FB

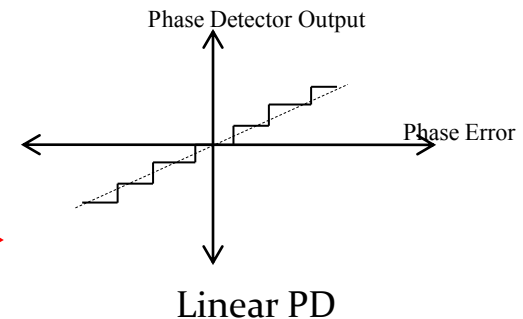
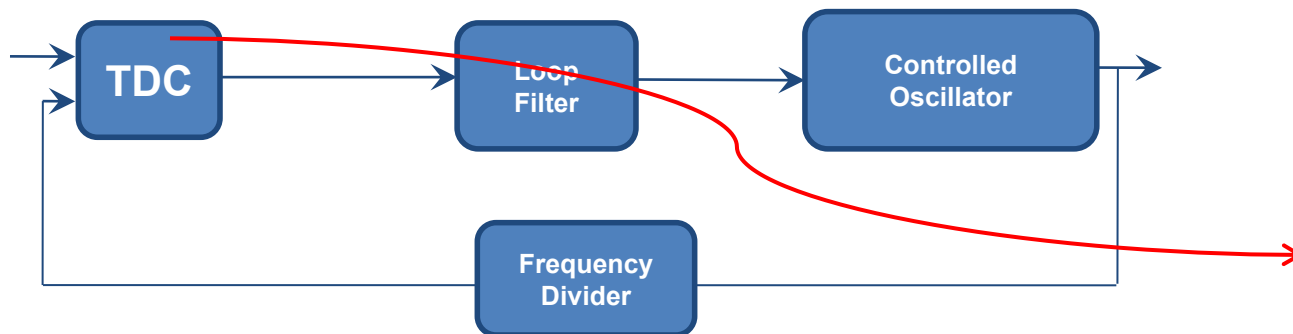
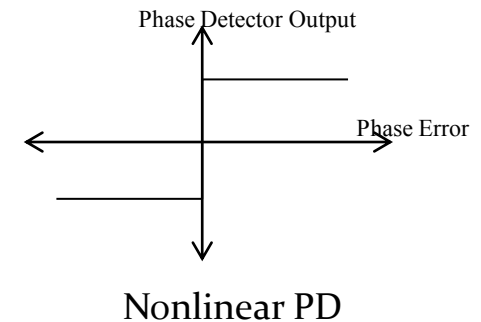
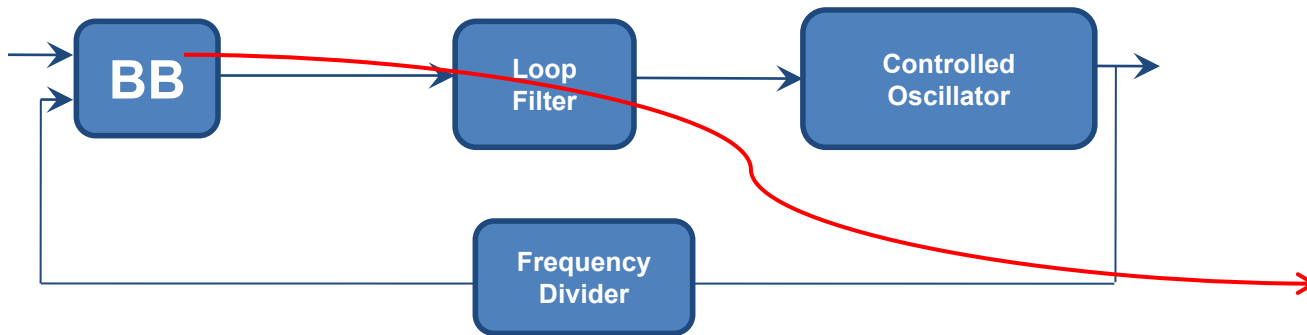
# PLL Types

- Trend:
  - Past – Analog Design
  - Future – Digital Design
- Features:
  - Analog: High Accuracy
  - Digital: Scalable
- Challenges:
  - Technology scales down
  - Analog design – difficult!!



# Digital PLLs

- Digital PLL:
  - **Bang-Bang** – Non linear, low performance, low power
  - **TDC** - linear, good performance, high power



# BB-PLL Pros – Cons – Applications

- Pros
  - **Low Power**
  - Simple Implementation (simple phase detector)
- Cons
  - **Non-linear** loop dynamics (due to non-linear phase detector):
    - No well defined design methodology
    - Unreliable response
- Apps
  - Traditionally: CDR
  - Recently: Microprocessors, Wireless Transceivers, SoCs

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# Thesis Motivation

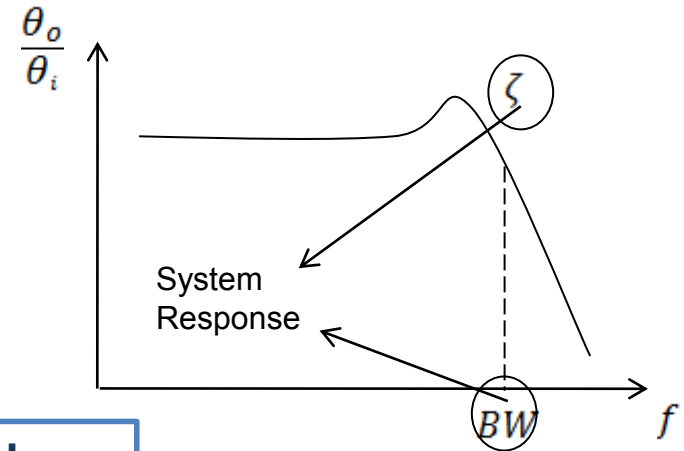
- Recent interest in **low power** designs:
  - Interest in BB-PLLs – use in high performance apps (microprocessors and wireless applications)
- **Non-linearity** of BB-PLLs prevent their use in high performance Apps.:
  - Need to solve problems caused due to non-linearity
- **Not much work in the literature** on solving BB-PLLs problems

# Problems Due to Nonlinearity

1. System Modeling
2. Unreliable Response

# Problem 1 - Modeling

Nonlinear → no TF analysis



## Design Methodology

Linear PLL

BB-PLL

$$H(s) = \frac{K_d \cdot K_0 \cdot \omega_{LPF}}{s^2 + \omega_{LPF} s + K_d \cdot K_0 \cdot \omega_{LPF}}$$

Design Parameters

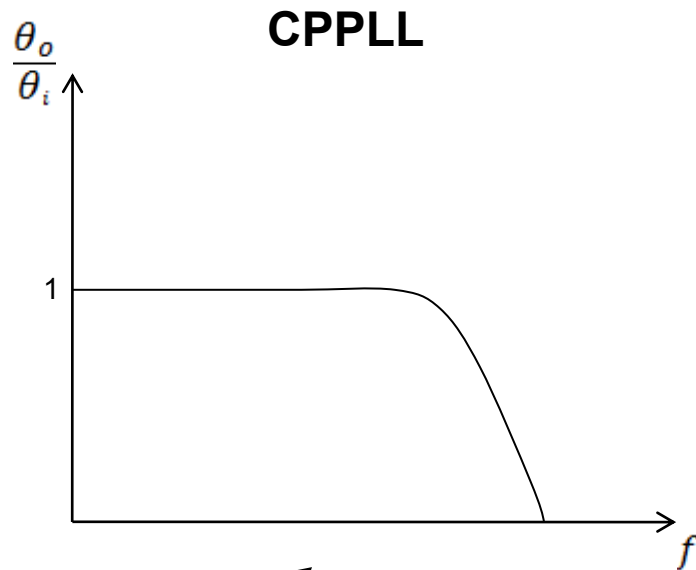
$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Desired Response

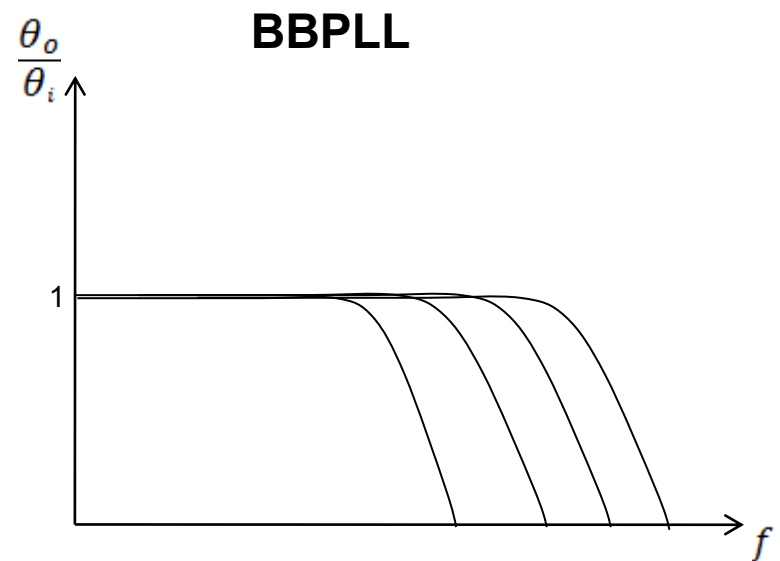
?

# Problem 2 – Nonlinear Response

## BW – Phase error magnitude



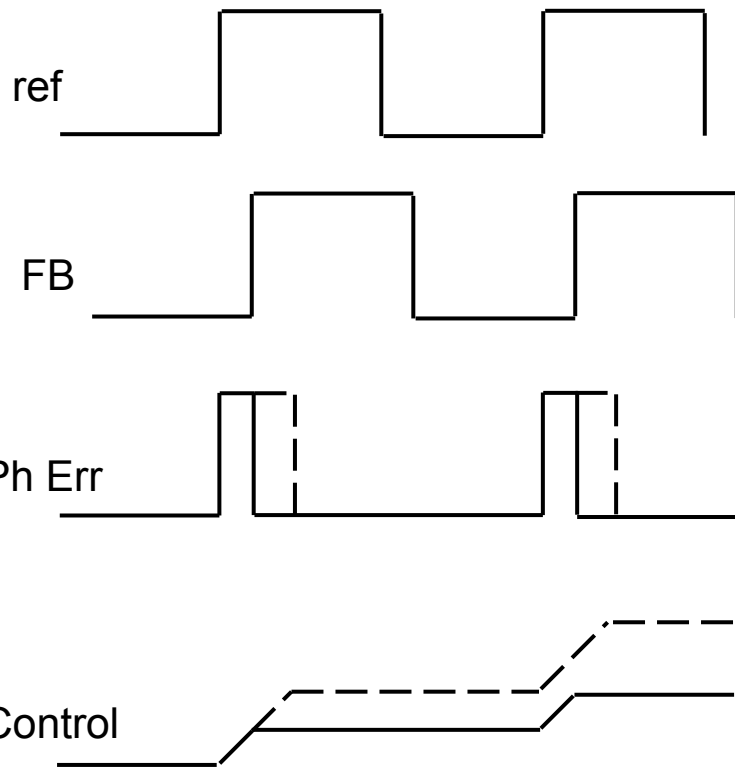
Independent of input phase error



Depending on input phase error

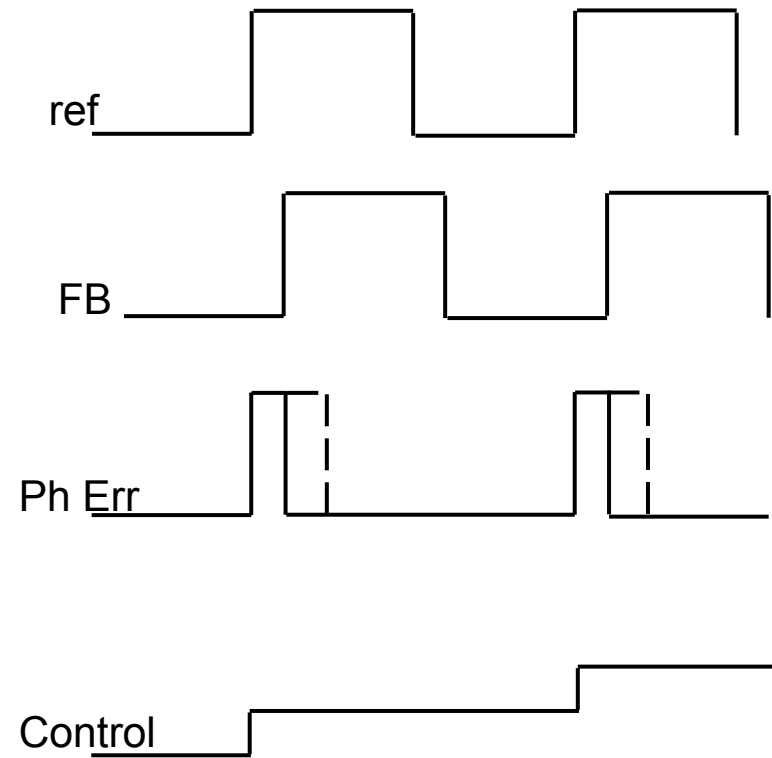
# Problem 2 – Nonlinear Response

## CPPLL



Control Voltage proportional to input error

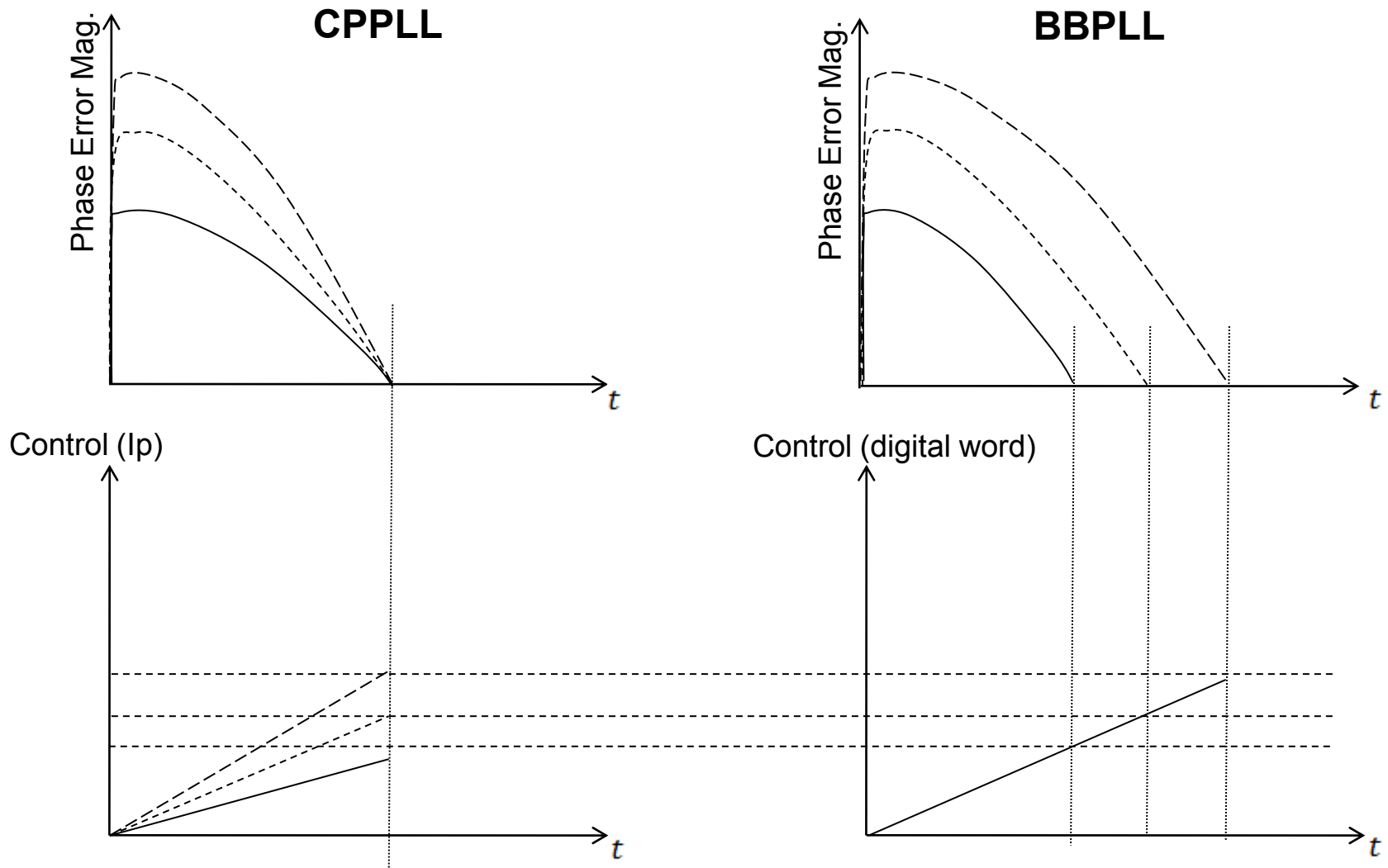
## BBPLL



Control Word not proportional to input error

# Problem 2 – Nonlinear Response

BW – Phase error magnitude



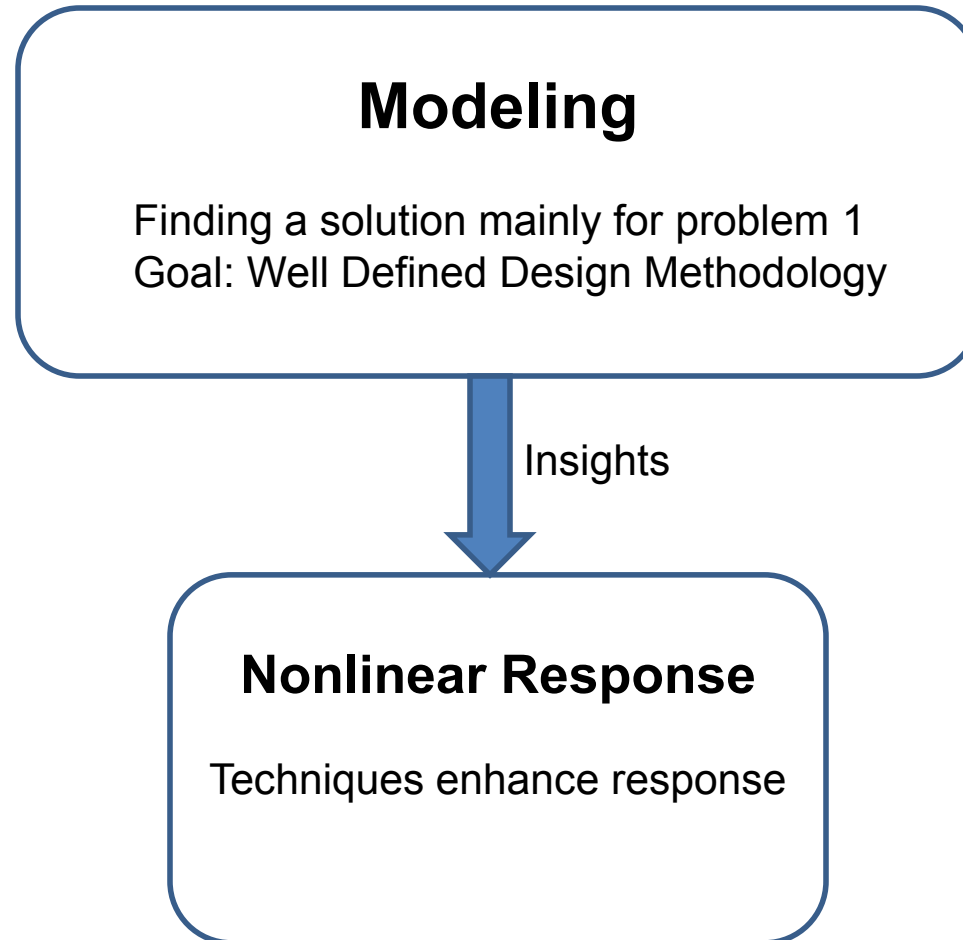
# Literature

- On problem 1 (Modeling):
  - **Only one model** is proposed by Razavi in 2003 [1]
  - Model **valid only for small** Phase Error Magnitudes (PEMs)
  - Model is **specific for error patterns at CDR** applications
- On Problem 2 (Nonlinear Response):
  - Different solutions proposed
  - Circuit techniques to regulate the BW through digital algorithms
- Literature shortage in Modeling → Thesis focus on Modeling

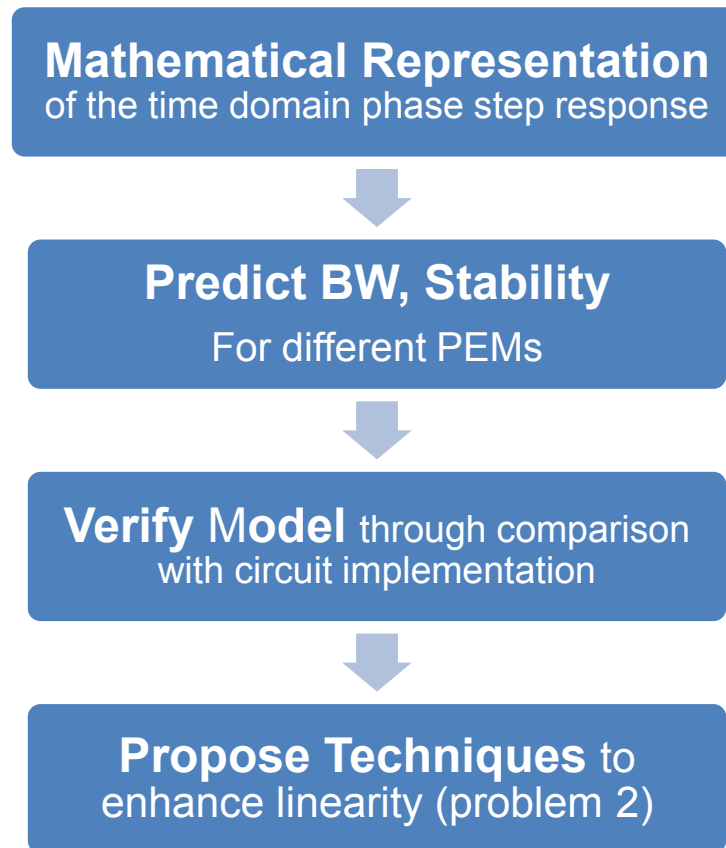
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# Scope of Work



# Methodology

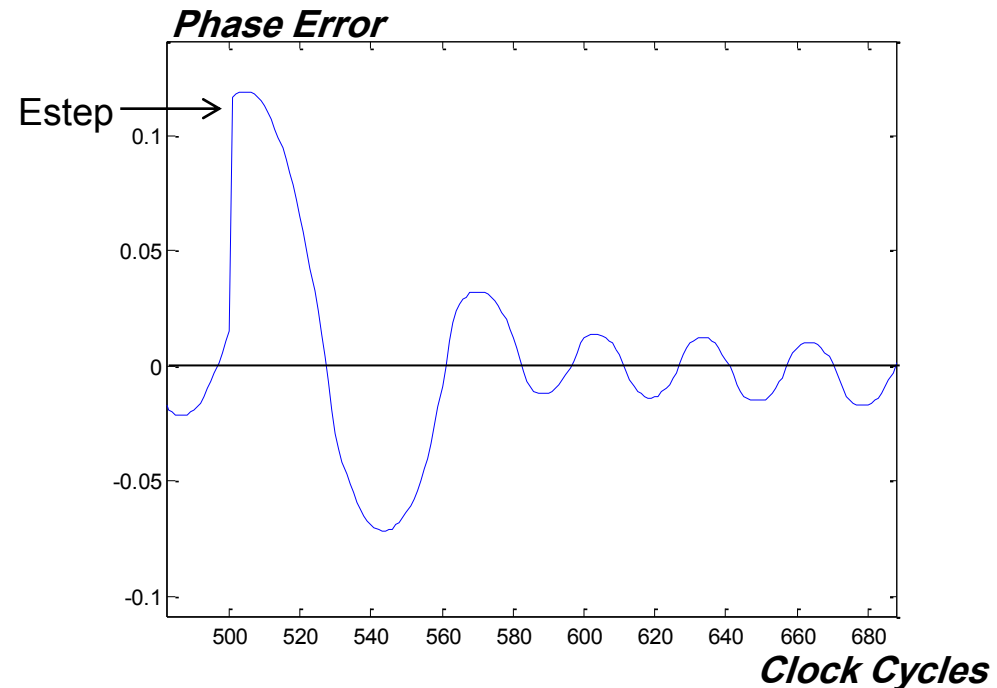


# Outline

- Introduction
- Proposed Modeling Methodology
  - **Model Parameters**
  - Model Derivation
- BB-ADPLL System
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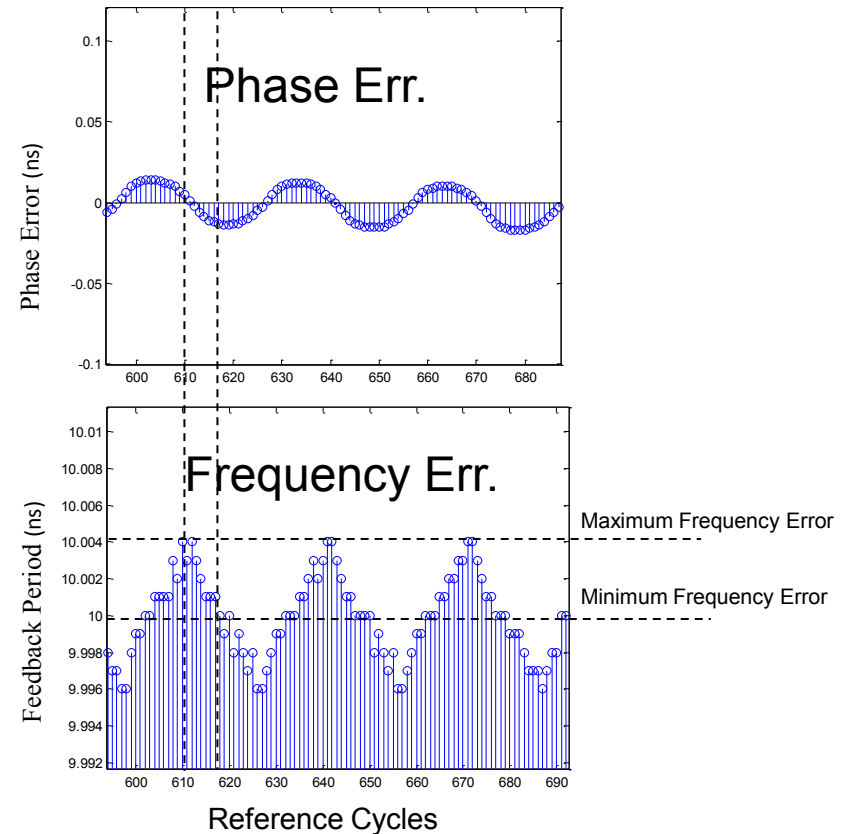
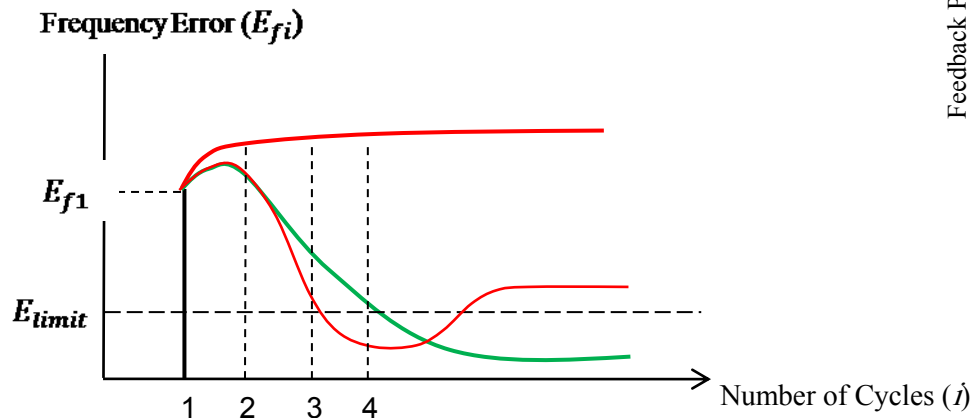
# Modeling (objective? – How?)

- Objective?
  - Predicting **BW**
  - Predicting **Stability**
- How?
  - Phase Step Response
    - Settling  $\rightarrow$  Stability
    - Settling time  $\rightarrow$  BW



# Modeling (How to predict stability?)

- Frequency Error – Phase Error
- $E_{fi}$  at zero crossings
- $E_{fi}$  trajectory – settling – stability
- Predict  $E_{fi} \rightarrow$  stability

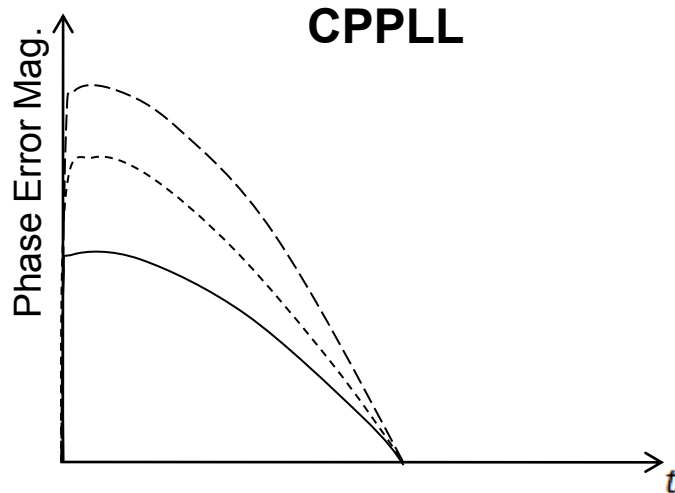


**Stability Limit:  $E_{fi} < E_{limit}$**

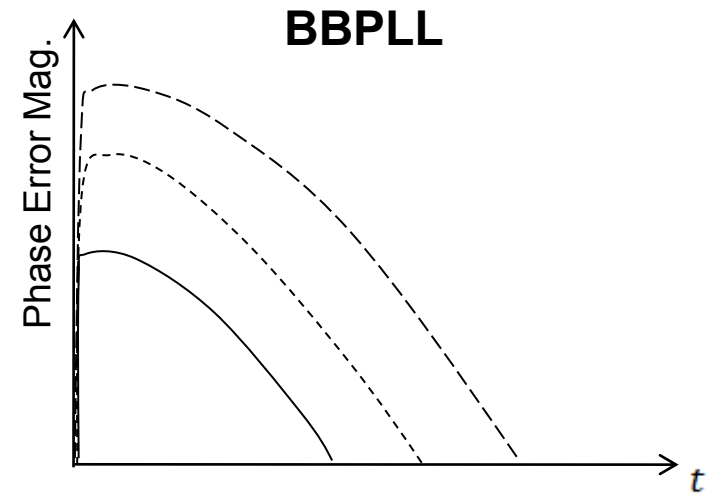
# Modeling (predicting BW – what is BW?)

**BW: How fast PLL can track jitter**

$$BW = \frac{1}{T_{\text{settling}}}$$



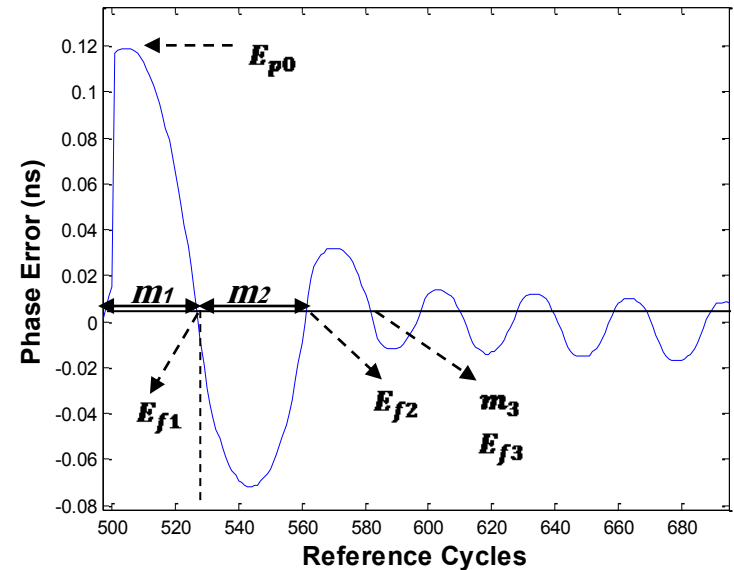
Constant BW



Variable BW

# Modeling (How to predict BW?)

- Phase step response
  - settling time – BW
- $m_i$ : cycles between zero crossings
- Predict  $m_i \rightarrow$  BW

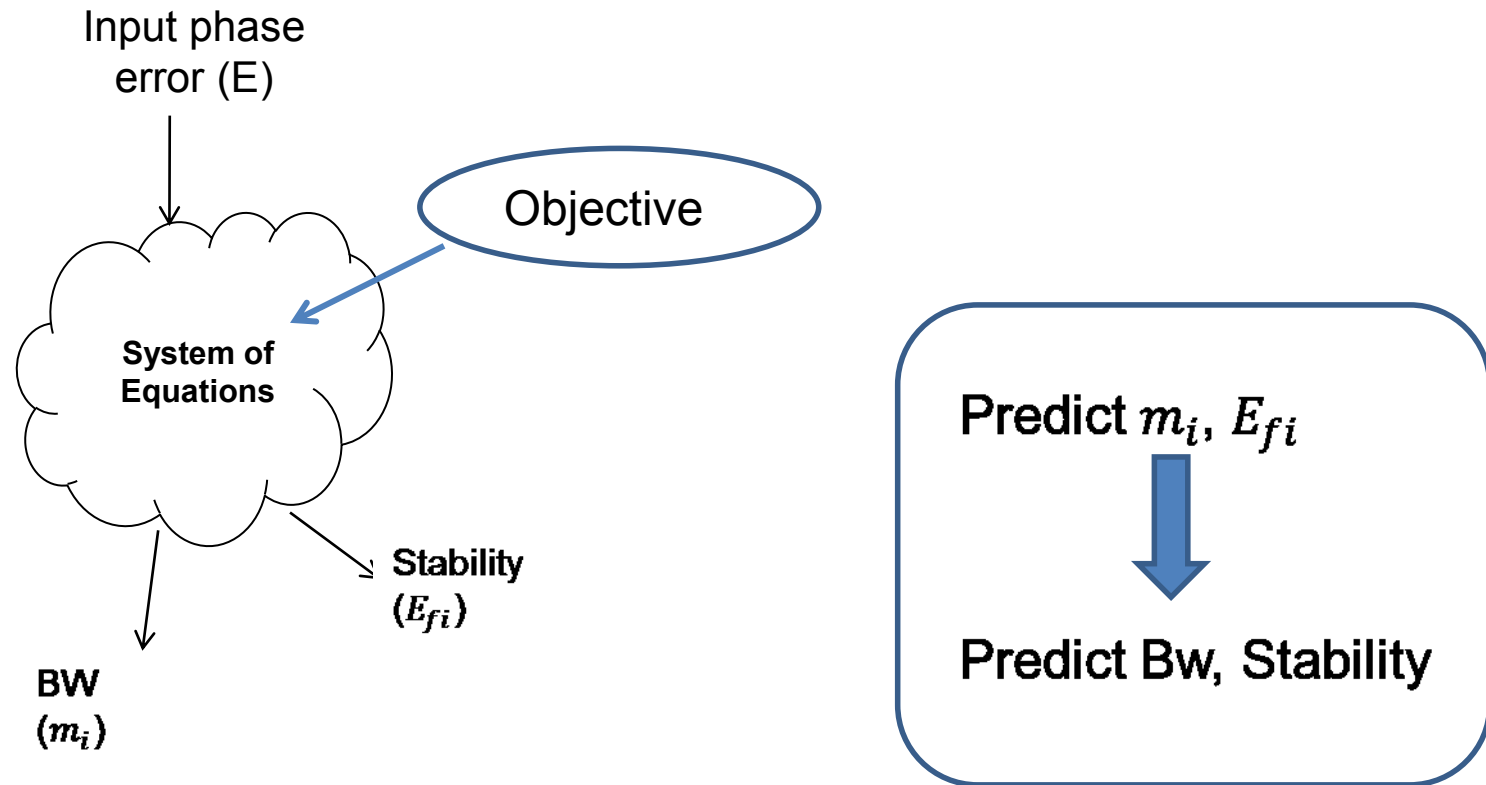


$$T_{\text{settling}} = (m_1 + m_2 + \dots + m_n) T_{\text{clk}}$$

(until  $E_n$  is small enough, less than  $E_{\text{limit}}$ )

- $T_{\text{settling}}$  depends on PEM (BB characteristic)

# Modeling (predicting BW & Stability)



(1) *Stability Limit:  $E_{fi} < E_{limit}$*

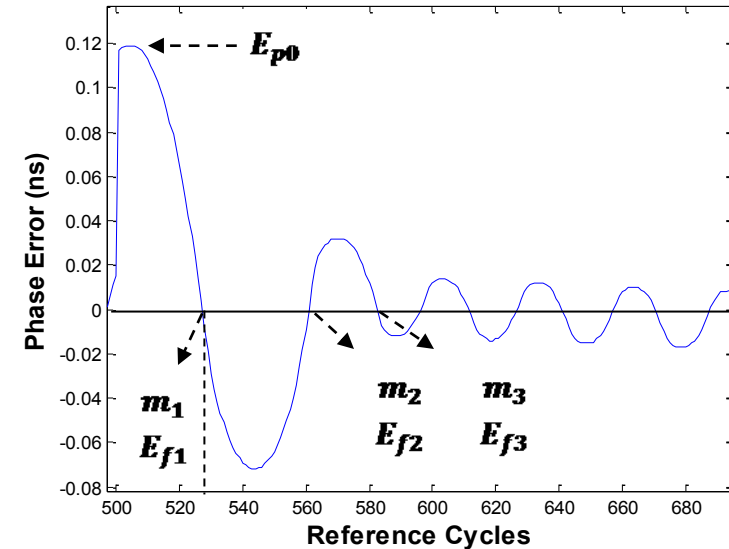
(2)  *$T_{settling} = (m_1 + m_2 + \dots + m_n) T_{clk}$   
(until  $E_n$  is small enough, less than  $E_{limit}$ )*

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# Modeling Methodology

- Phase step error  $\rightarrow$  loop acts to compensate
- Phase at zero crossings equals zero
  - Phase due to step err. = phase due to loop action

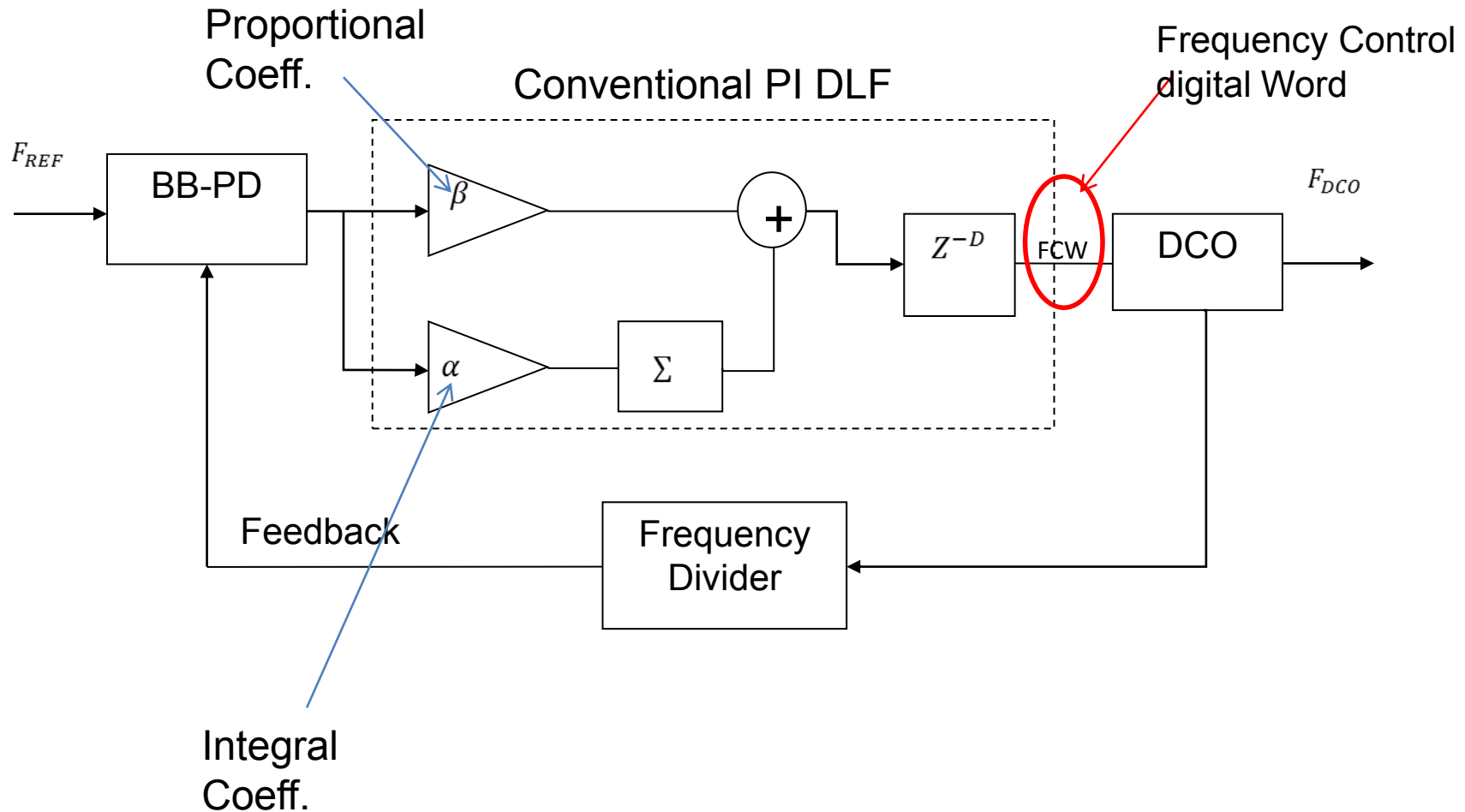


Mathematical Representation  
of both phase components (step &  
loop action)

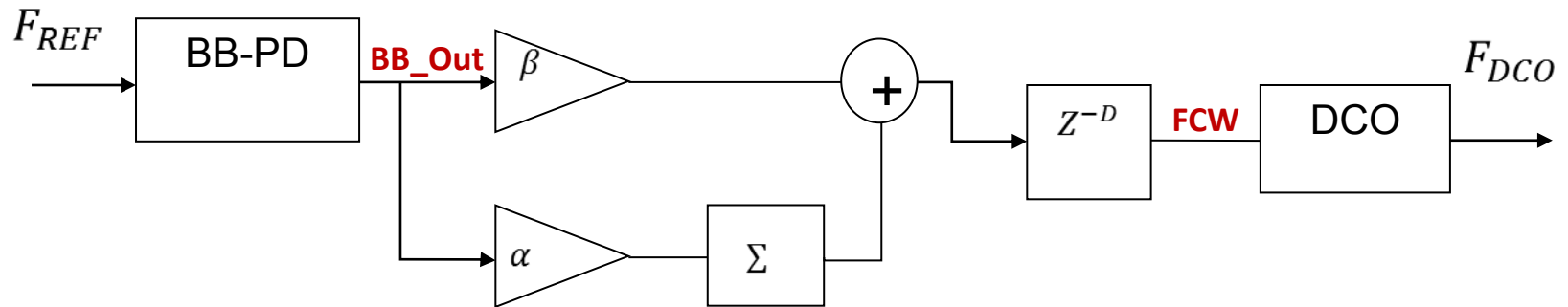
Equate  
at zero crossings

Get values of  
 $(m_i, E_{fi})$

# Modeling (BB-ADPLL Operation)



# Modeling (DLF Operation)



	BB_Out		FCW	
	1	Proportional Contribution Per BB decision	$\beta$	Integral Contribution Per BB decision
	1		$\beta + \alpha$	
	1		$\beta + 2\alpha$	
	1		$\beta + 3\alpha$	
	...		...	
<b>Polarity Change</b>	-1		$-\beta - \alpha$	
	-1		$-\beta - 2\alpha$	

# Modeling Methodology

- Phase due to loop action:
  - Proportional path

$$\phi_{1,due\ to\ proportional} = \beta \Delta\phi m_1$$

Change in frequency control word over  $m_i$

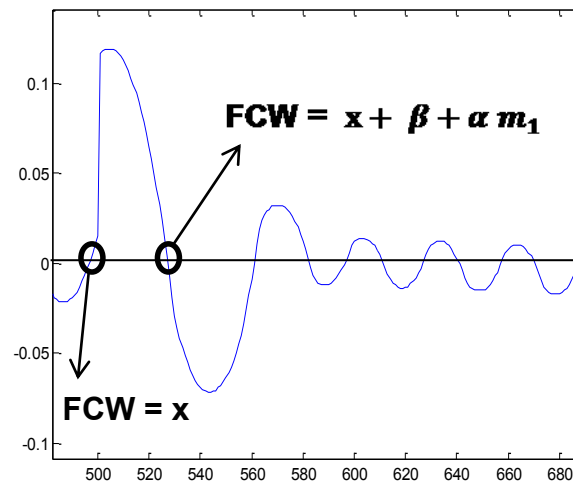
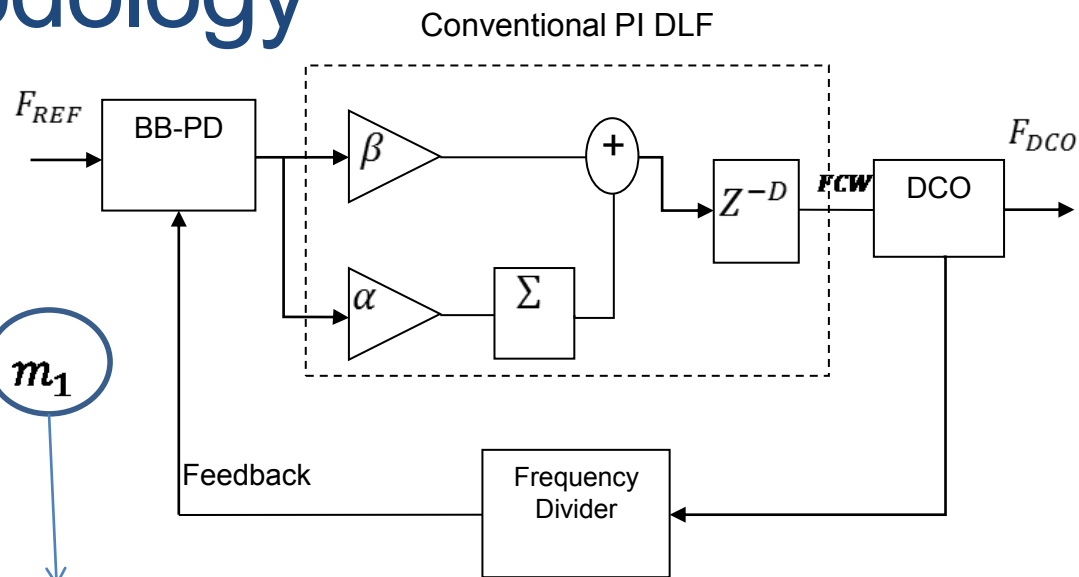
DCO phase change due to one change in the FCW (DCO resolution)

Integration of phase over  $m_1$  due to frequency change

- Integral Path

$$\phi_{1,due\ to\ integral} = \alpha m_1 \Delta\phi + \alpha (m_1 - 1) \Delta\phi + \dots + \alpha \Delta\phi$$

$$\phi_{1,due\ to\ integral} = \alpha \Delta\phi \frac{m_1(m_1 + 1)}{2}$$



# Modeling Methodology

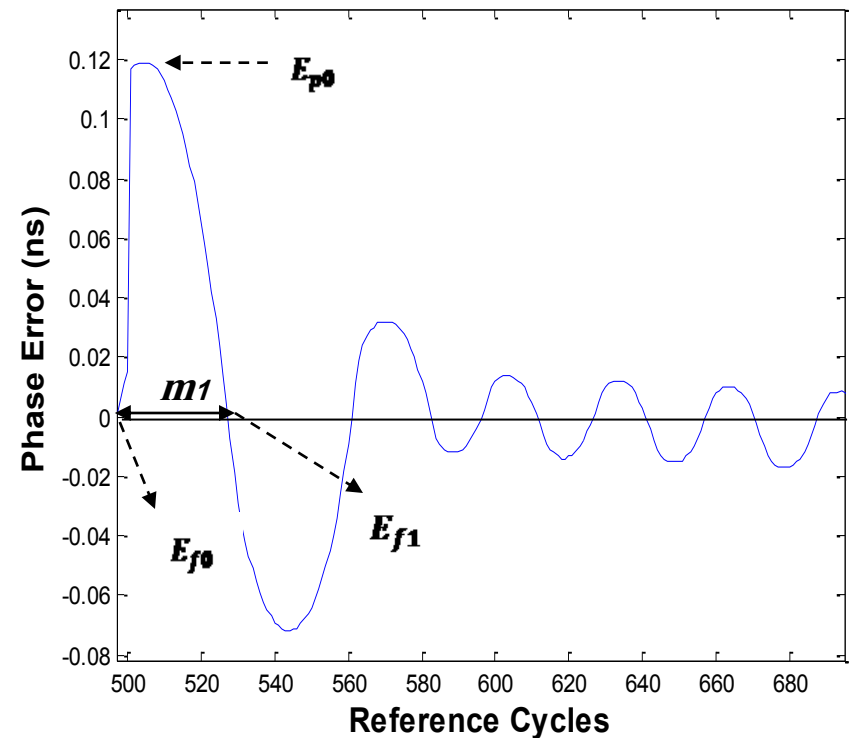
- Phase due to loop action:

$$\phi_1 = \alpha \frac{m_1(m_1 + 1)}{2} \Delta\phi + \beta m_1 \Delta\phi$$

- Phase due to step error:

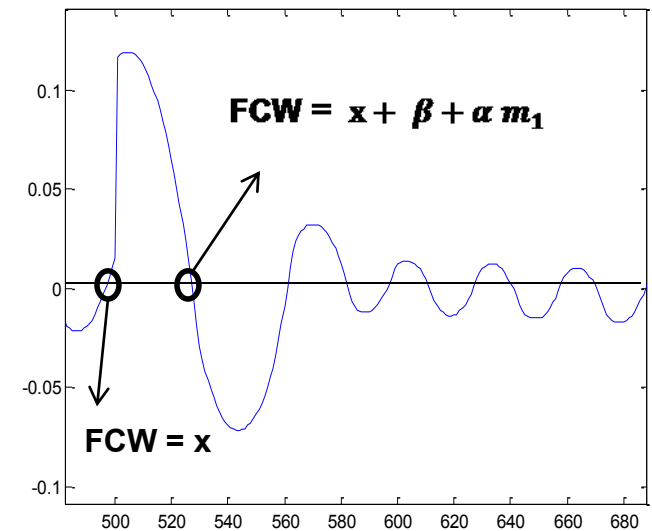
$$\phi_{e1} = E_{p0}$$

- Equate  $\rightarrow$  get  $m_1$



# Modeling Methodology

- 
- Frequency Error  $E_{f1}$  is the change in frequency from the initial state:



$$E_{f1} = (\alpha m_i + \beta)\Delta\phi - E_{f0}$$

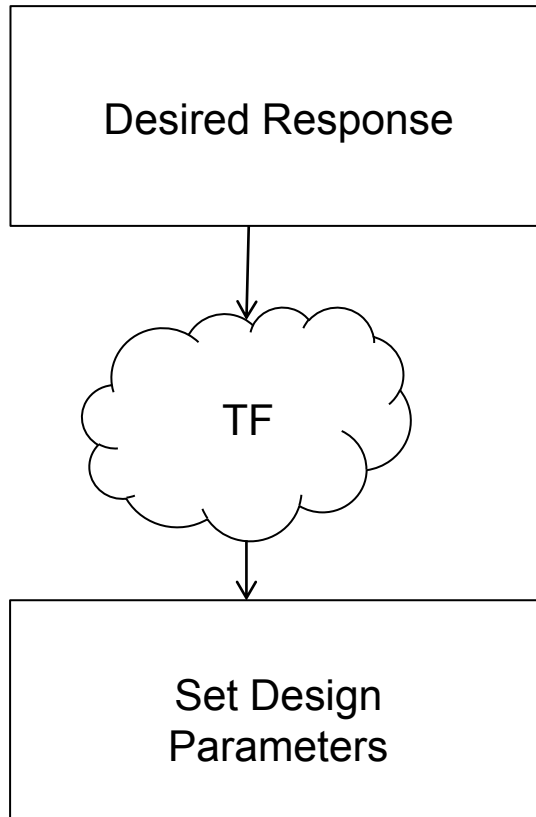
# Modeling Methodology

- Similarly, can get any  $m_i, E_{fi}$
- Thus, Given:
  - PEM (Estep),
  - the DLF parameters ( $\alpha, \beta, D$ )
  - the DCO step ( $\Delta\phi$ )
  - The division ratio N (DCO frequency/reference frequency)  
→ get  $m_i, E_{fi}$  → predict stability and BW

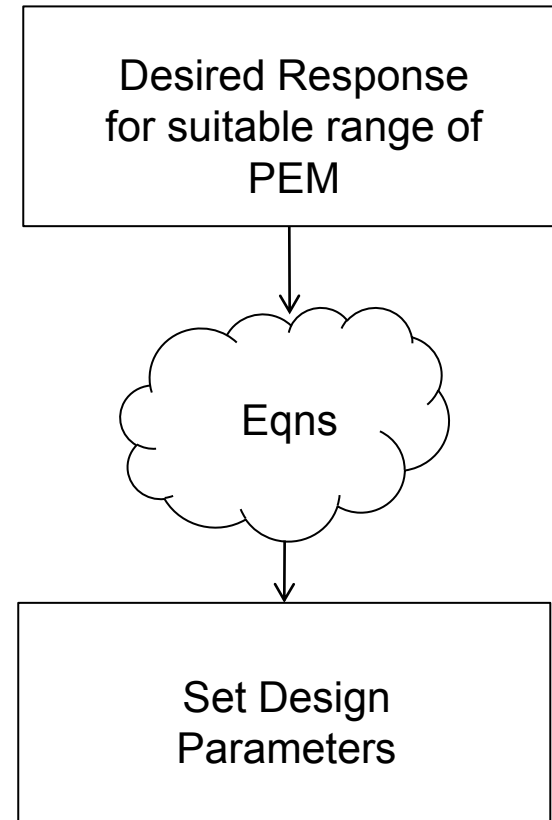
# Modeling (outcome)

## Design Methodology

### CPPLL



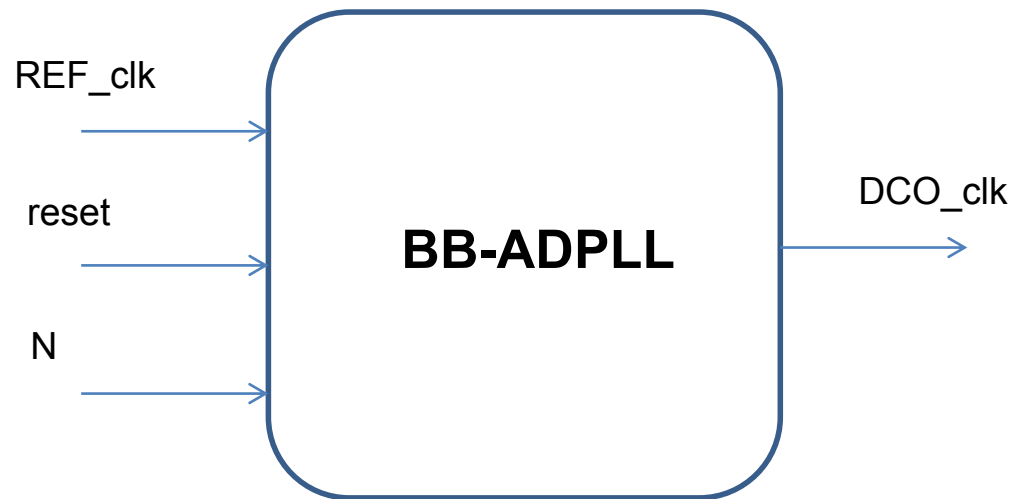
### BBPLL



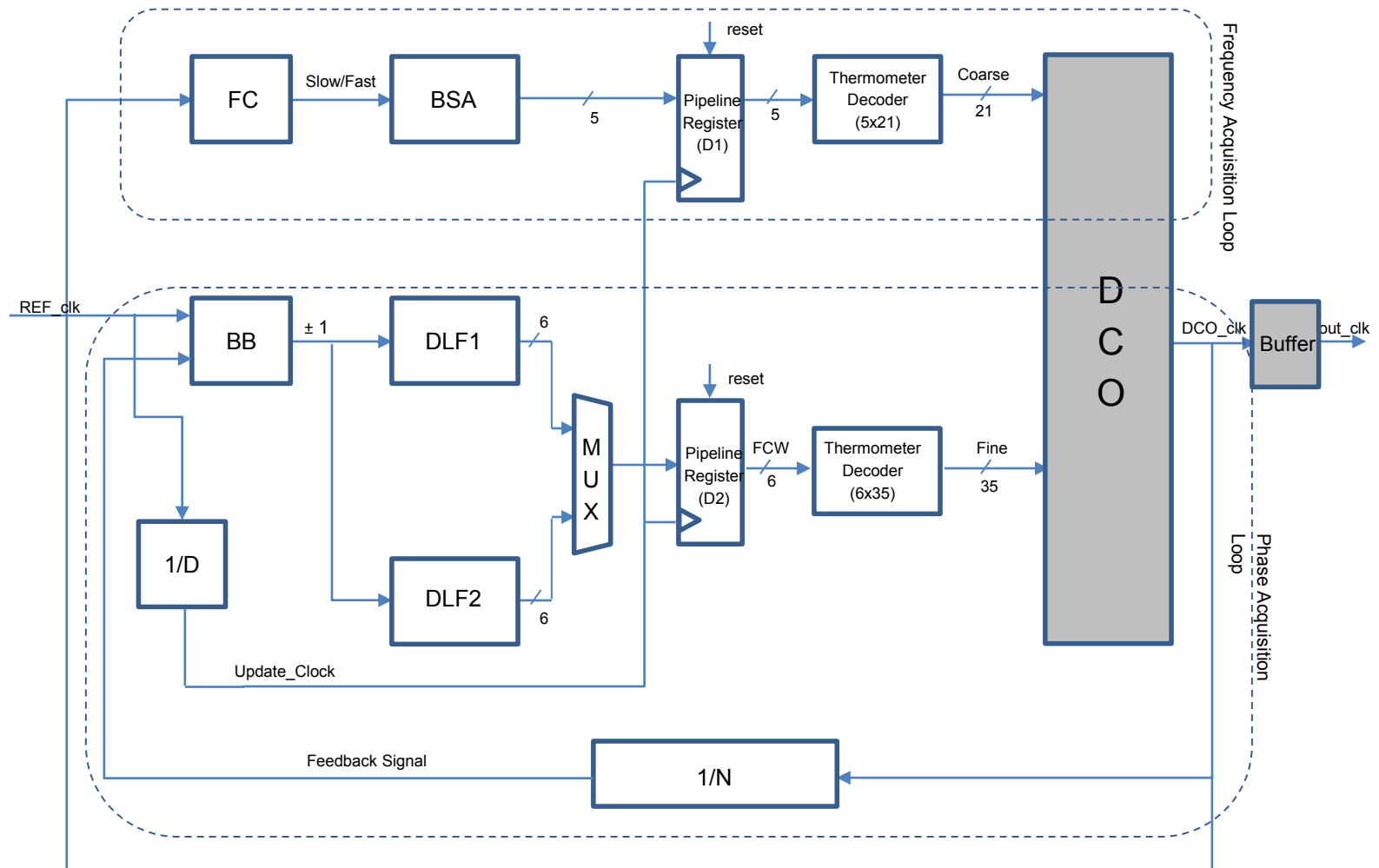
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  - **System Architecture & Performance**
  - Model Verification
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# BB-ADPLL Pin Diagram



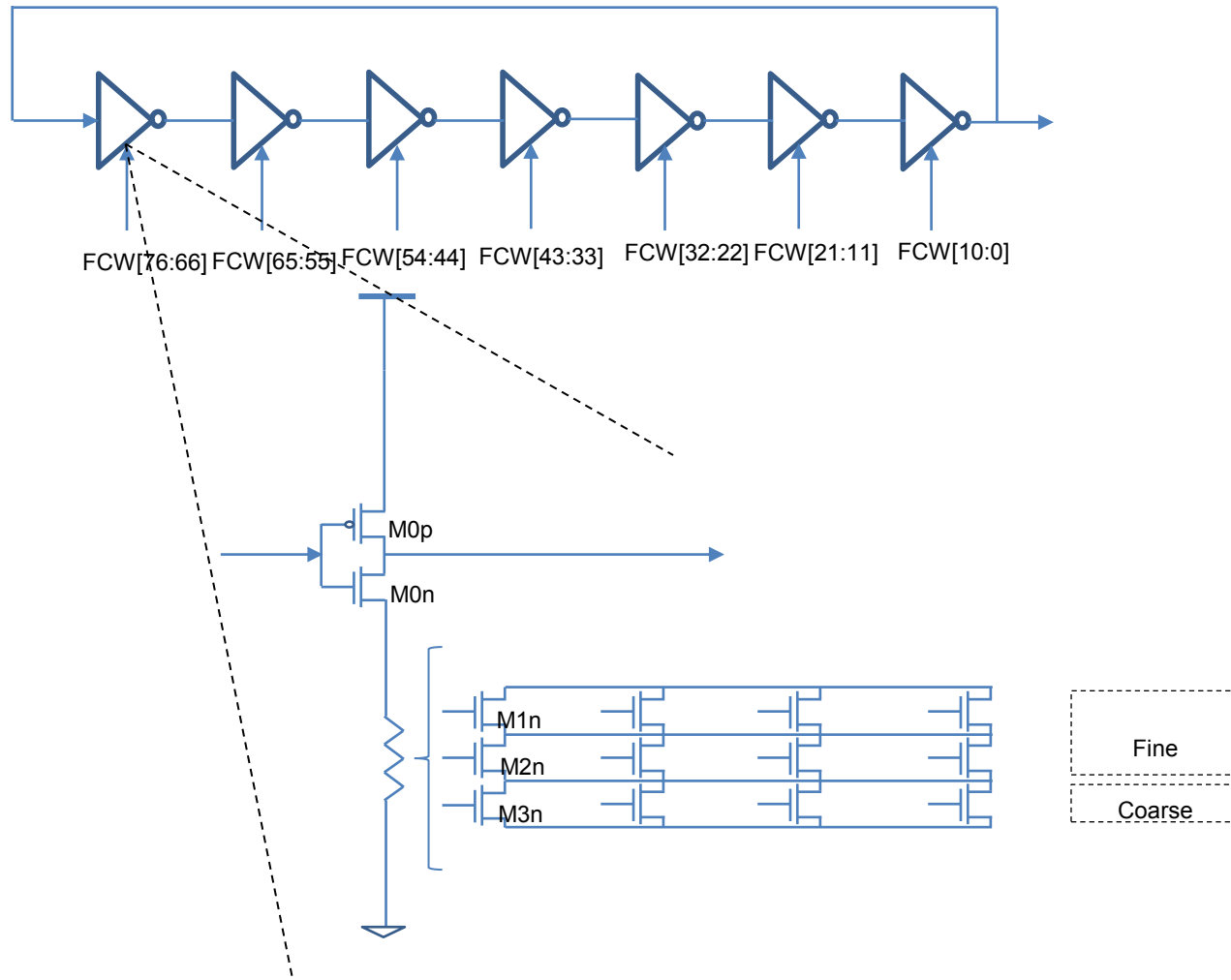
# BB-ADPLL



 Custom Design

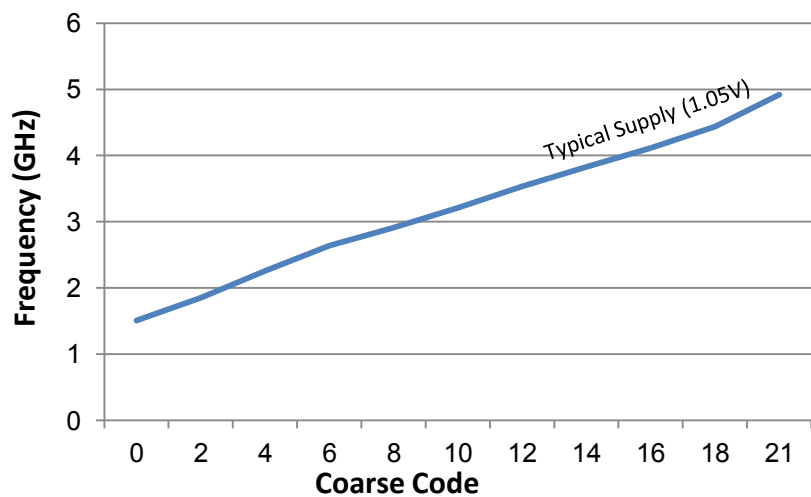
 RTL

# BB-ADPLL (DCO)



# DCO

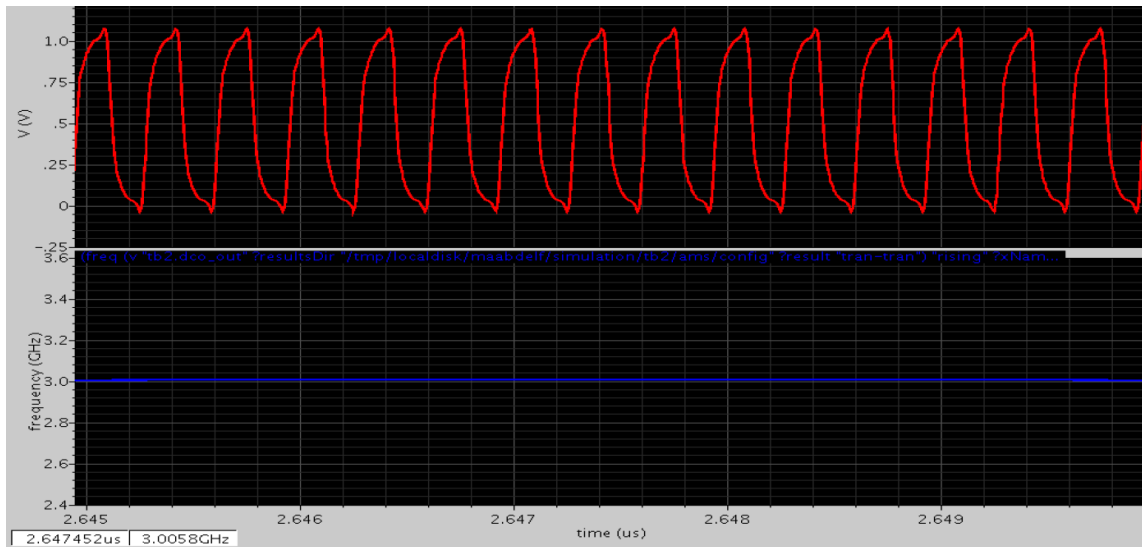
## Frequency Range



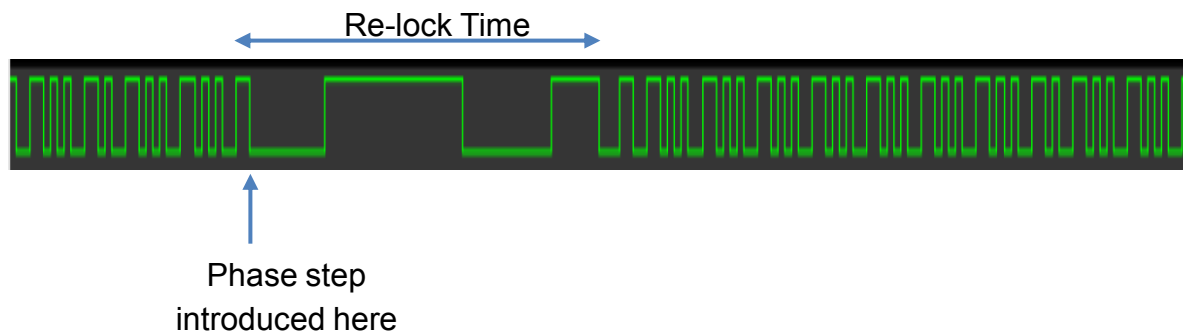
## Frequency Resolution

Frequency (GHz)	Coarse Step (MHz)	Fine Step (MHz)
1.5 (Min)	171.5	0.7
3	149.5	1.45
4.9 (Max)	243	2.5
<b>Average</b>	162.3	<b>1.55</b>

# PLL Results



Locked at 3 GHz



# PLL Results

Frequency	Lock Time (us)	RMS Jitter (ps)	Peak-to-Peak Jitter (ps)
2 GHz	2.5	1.13	4.2
3 GHz	2.2	0.88	3.6
5 GHz	1.6	0.7	3.4

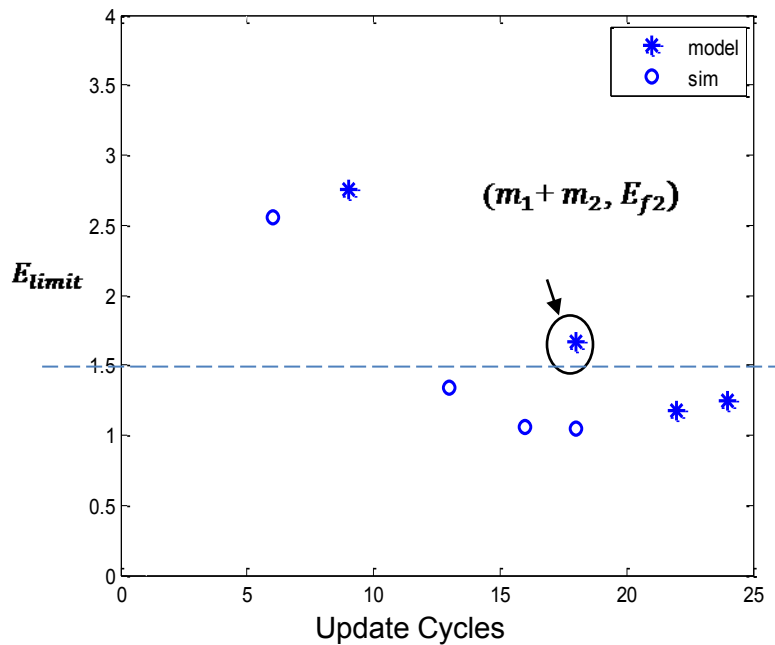
COMPARISON	This Work	ISSCC 2012 [2]
Measurement Frequency	3 GHz	3 GHz
Supply	1.05 V.	0.5 – 1V.
RMS Jitter	0.88 ps	0.8 ps
Silicon	No	Yes

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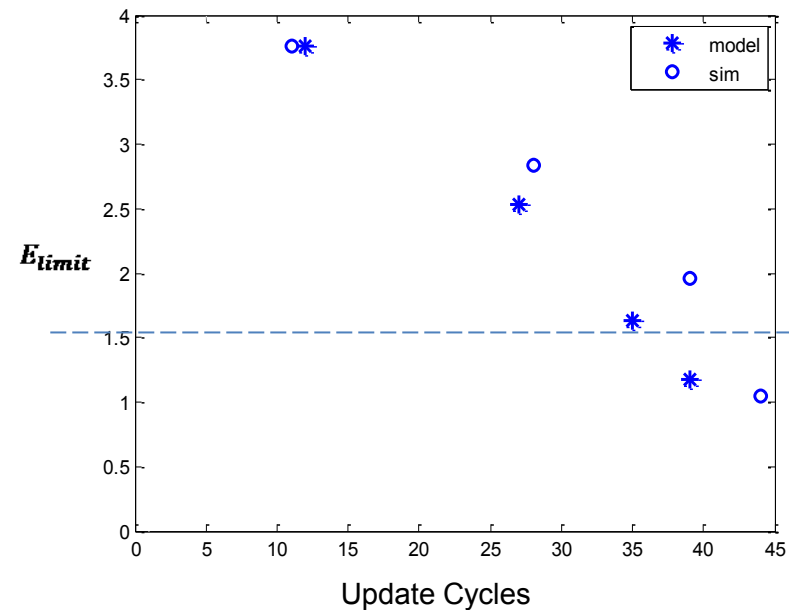
# Model Verification

Frequency Error  $E_{fi}$  (ps)



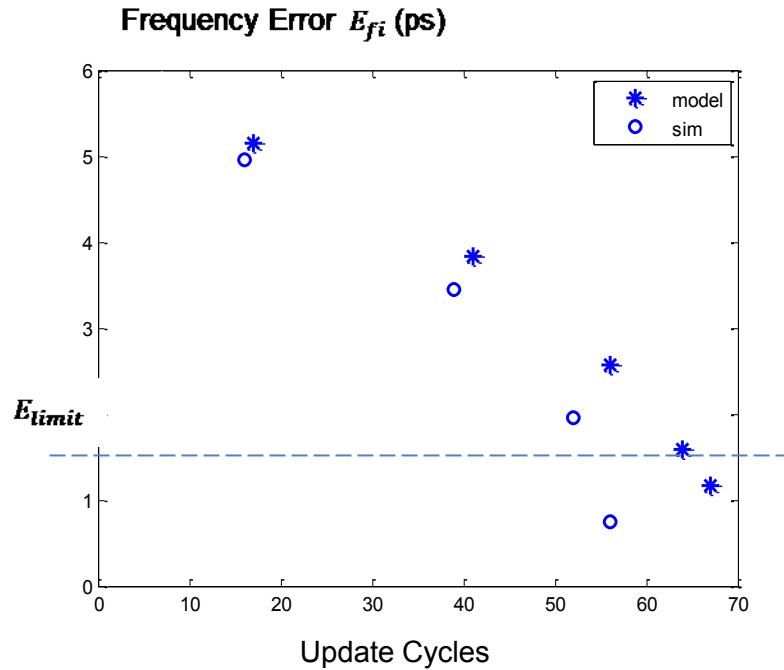
PEM = 600ps

Frequency Error  $E_{fi}$  (ps)

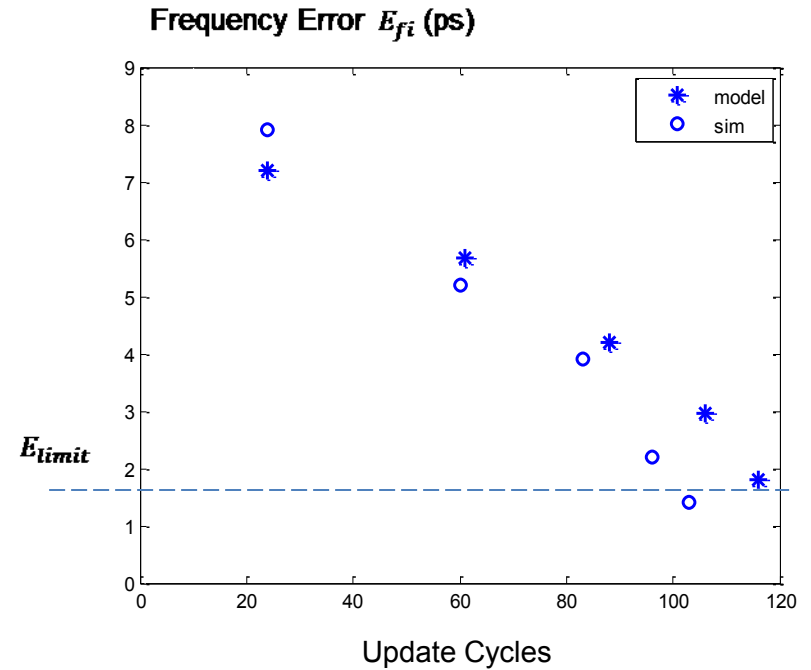


PEM = 1200ps

# Model Verification



PEM = 2400ps



PEM = 5000ps

# Model Verification

PEM (ps)	$T_{settling}$ (model)	$T_{settling}$ (sim.)	Accuracy %
600	480 ns	360 ns	75%
1200	780 ns	880 ns	88.6%
2400	1280 ns	1120 ns	87.5%
5000	2320 ns	2190 ns	94.3%

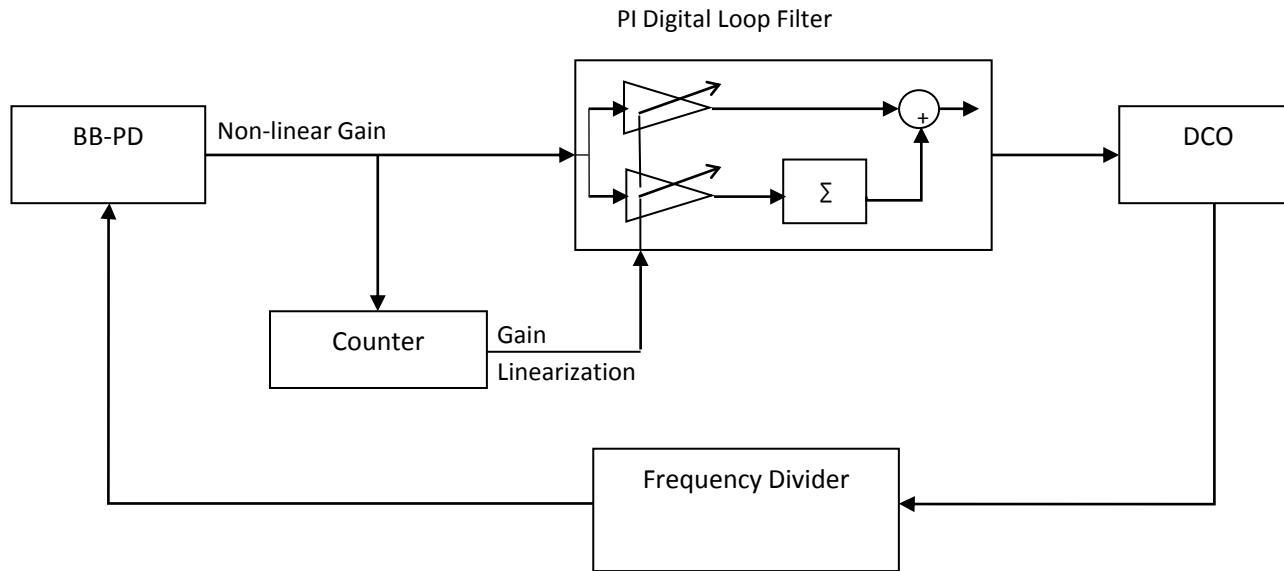
# Model Accuracy

- **Better accuracy can be achieved – less assumptions**
- **Assumptions:**
  - Initial frequency error value ( $E_{f0}$ )
  - Zero crossing points are at integer multiple of reference
  - DCO phase noise neglected

# Outline

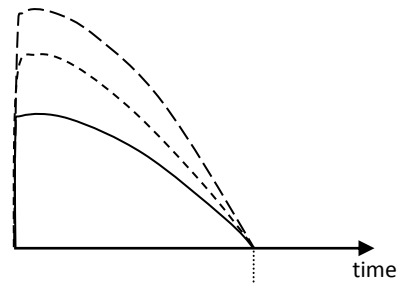
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  - **Technique 1**
  - Technique 2
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# Proposed Technique 1

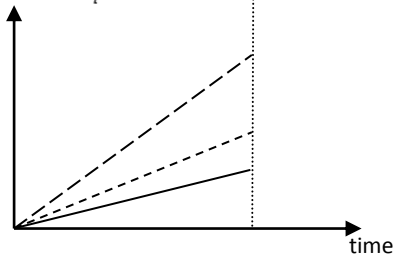


# Proposed Technique 1

Phase Error Magnitude

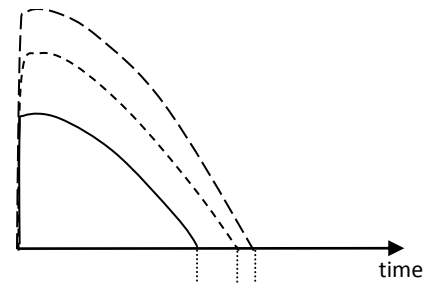


Control Current ( $I_p$ )

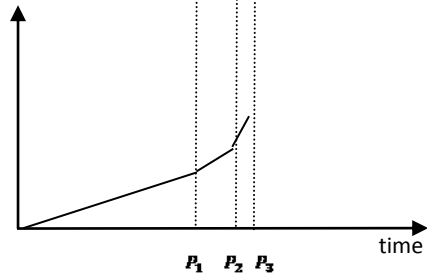


(a)

Phase Error Magnitude



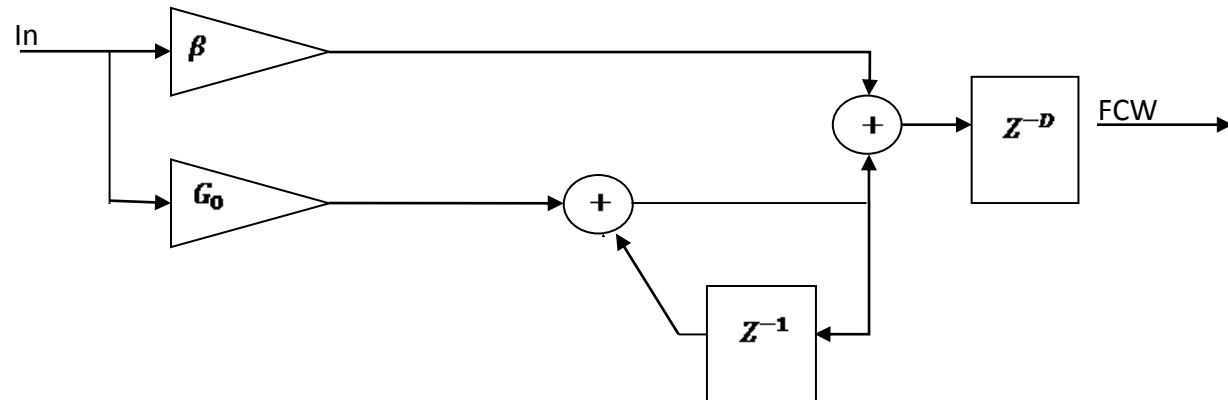
FCW



(b)

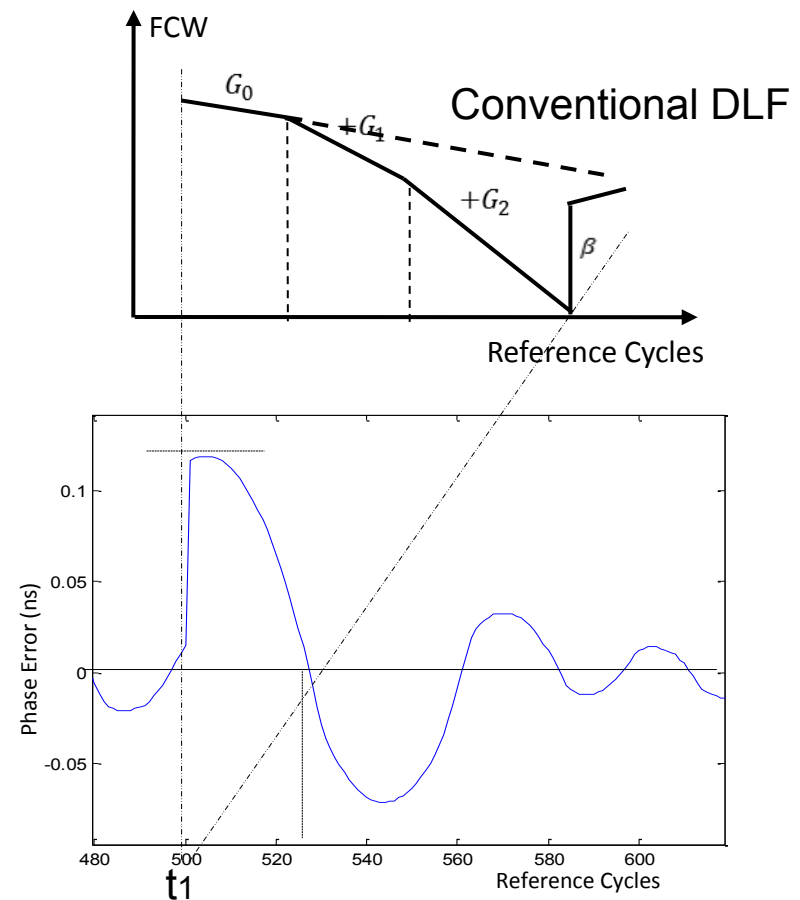
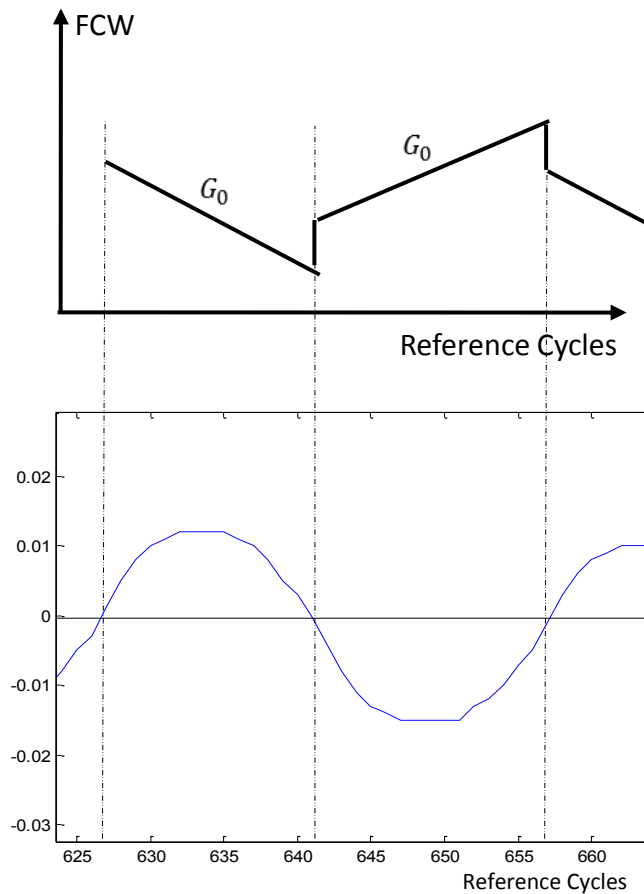
# Proposed Technique 1

- New DLF Architecture

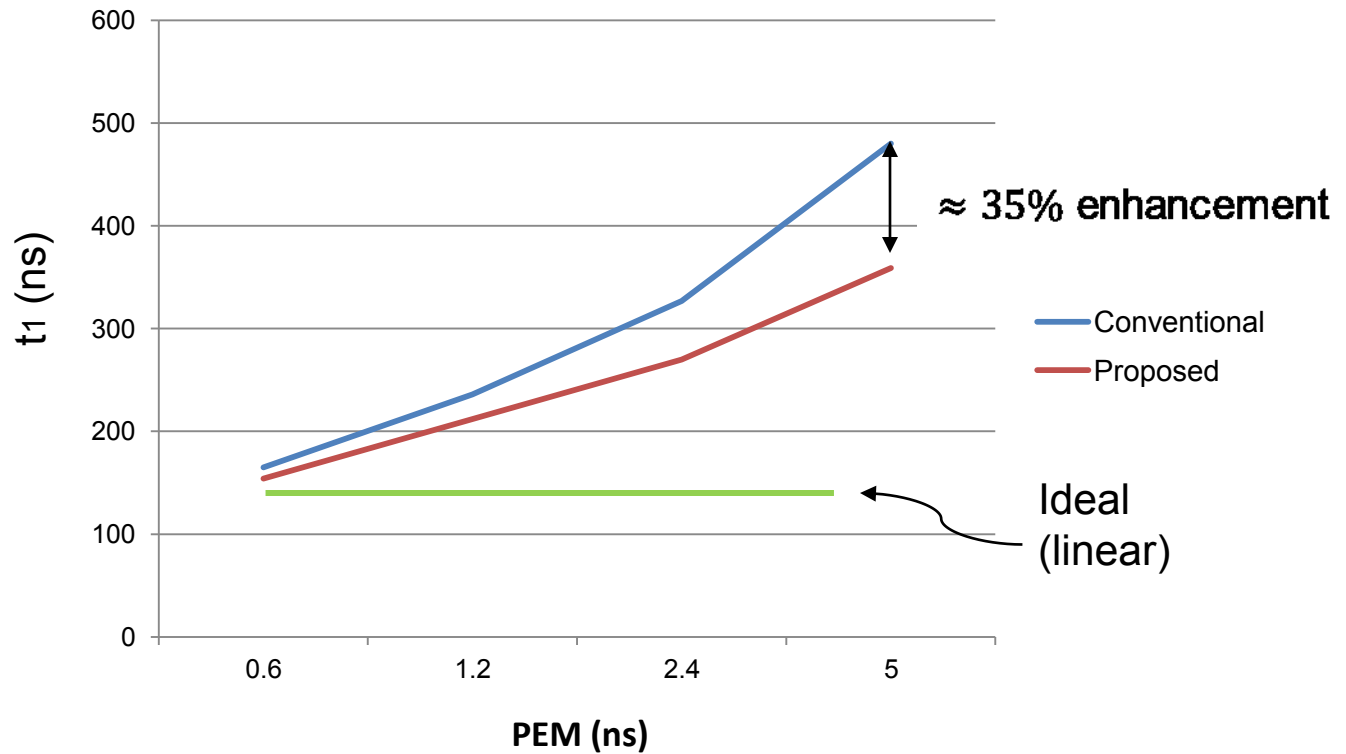


# Proposed Technique 1

- New DLF Operation



# Technique 1 verification



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# Proposed Technique 2

**At first zero crossing:**

Phase Error = 0

Freq. Error =  $E_{f1}$

**Add circuitry to estimate  $E_{f1}$ :**

$$E_{f1} = (\alpha m_1 + \beta)$$

**At first zero crossing:**

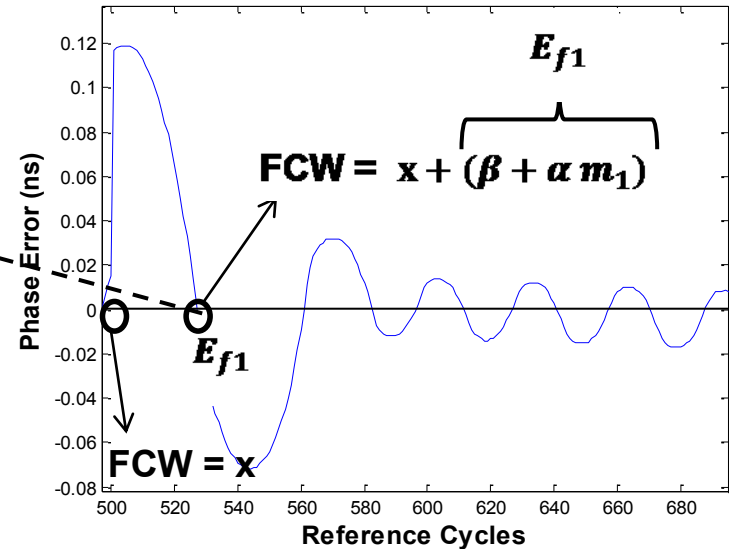
Subtract  $E_{f1}$  from  $FCW$

**At first zero crossing:**

Phase Error = 0

Freq. Error  $\approx 0$

**Relock Time Reduced**



# Technique 2 verification

PEM (ps)	$T_{settling}$ (conventional)	$T_{settling}$ (proposed)	Percentage Reduction
600	480 ns	215 ns	55.2 %
1200	880 ns	406 ns	53.8 %
2400	1120 ns	457 ns	59.1 %

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# Conclusion

- BB-PLL: **low power – nonlinearity**
- Nonlinearity: **modeling problem**
- **Model** predict system response in terms of design parameters – provides **design methodology**
- Model insights → **proposed techniques** to enhance system linearity (**SL enhanced by 35%, Re-lock time enhanced by 55%**)

# Future Work

- **Physical Design** (further verification of model)
- **Enhance accuracy** (Re-develop model with less assumptions)

# References

- [1] J. Lee, K. S. Kundert, and B. Razavi, “Analysis and modeling of bangbang clock and data recovery circuits,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1571–1580, Sep. 2004.
- [2] N. August, H. Lee, M. Vandepas, R. Parker, “A TDC-less ADPLL with 200-to-3200MHz range and 3mW power dissipation for mobile SoC clocking in 22nm CMOS,” *ISSCC Dig. Tech. Papers*, pp. 246-248, Feb., 2012.

# Publications From This Work

- Accepted

- Abdelfattah M., Lotfy A., Abdel-moneum M., Kurd N., Ghoneima M., Taylor G., Ismail Y. “*Modeling the Response of Bang-Bang Digital PLLs to Phase Error Perturbations*”, IEEE in proceedings of **CICC** 2012.
- Abdelfattah M., Lotfy A., Abdelsalam M., Abdel-moneum M., Kurd N., Ghoneima M., Taylor G., Ismail Y. “*A Novel DLF Architecture for Digital Bang-Bang PLLs*” IEEE in proceedings of **SOCC** 2012.

- Under Preparation

- “*A Novel Technique to Reduce the Lock Time of BB-DPLLs*” (Conference)
- Abdelfattah M., Lotfy A., Abdel-moneum M., Kurd N., Ghoneima M., Taylor G., Ismail Y. “*Modeling the Phase Step Response of Bang-Bang Digital PLLs to Phase Error Perturbations*”, submitted to TCAS I.

# QUESTIONS

