ULTRA WIDEBAND RECEIVER FRONT-END

by

AHMAD MAHMOUD SHEREEF HASSAN ELHEMEILY
AHMED MOHAMMED AHMED SAYED

A THESIS

Submitted in partial fulfillment of the requirements for the degree

BACHELOR OF SCIENCE

Electronics and Communications Engineering Department
Faculty of Engineering

AIN SHAMS UNIVERSITY
Cairo, Egypt

Supervised by:

Professor Hani Fikry

July 2013

Abstract

In the last few years, the interest in ultra-wideband technology which uses wireless transmission in the 3.1-10.6 GHz unlicensed band has increased. In this thesis, a non-coherent low-power ultra-wideband receiver front-end is presented. The usage of non-coherent detection greatly simplifies the receiver and hence reduces power consumption. The receiver system is first discussed. Then, the circuit level implementation of the two main receiver blocks, the LNA and the squarer for the 3.1-5.3 GHz band are presented with circuit simulation results on the LF150 technology.

Table of Contents

List of Figures v
List of Tables viii
Acknowledgements ix
Chapter 1 - INTRODUCTION AND SYSTEM ARCHITECTURE 1
1.1 ULTRA-WIDEBAND DEFINITION 2
1.2 ULTRA-WIDEBAND UNIQUE FEATURES 2
1.2.1 Ultra-wideband and Shannon's theorem 2
1.2.2 The coexistence of ultra-wideband and narrowband signals 3
1.2.3 Time resolution 3
1.3 IMPULSE RADIO (IR) ULTRA-WIDEBAND RECEIVER ARCHITECTURES 4
1.3.1 Coherent receivers 4
1.3.2 Non-coherent receivers 4
1.3.2.1 Transmitted Reference receivers (TR) 5
1.3.2.1 Energy detection receivers (ED) 6
1.4 THE IMPLEMENTED RECEIVER ARCHITECTURE 6
1.5 SYSTEM PERFORMANCE AND SPECS 7
Chapter 2 - LOW NOISE AMPLIFIER DESIGN AND SIMULATION 10
2.1 INTRODUCTION 10
2.2 OJECTIVES AND TARGTED SPECIFICATIONS 11
2.3 DIFFERENT LNA TOPOLOGIES 12
2.4 PROPOSED LNA DESIGN 16
2.4.1 Wideband input impedance matching 18
2.4.2 The design for low noise figure 19
2.4.3 The design for flat gain 19
2.4.4 LNA biasing 19
2.4.5 LNA stability 20
2.4.6 LNA figure of merit 20
2.4.7 Output buffer 20
2.5 TSMC13RF DESIGN KIT SIMULATION RESULTS 21

2.5.1 Small signal simulation 21
2.5.2 Large signal simulation 24
2.6 TSMC13RF DESIGN KIT PROCESS CORNERS SIMULATION RESULTS 26
2.6.1 Small signal process corners 26
2.6.2 Large signal process corners 31
2.7 LF15RF DESIGN KIT SIMULATION RESULTS 32
2.7.1 Small signal simulation 32
2.7.2 Large signal simulation 35
2.8 LF15RF DESIGN KIT PROCESS CORNERS SIMULATION RESULTS 37
2.8.1 Small signal process corners 37
2.8.2 Large signal process corners 42
2.9 CIRCUIT LAYOUT 43
2.10 CONCLUSION 44
Chapter 3 - SQUARER 45
3.1 - SQUARER TOPOLOGY 45
3.2 CURRENT MIRRORS 47
3.3 COMMON MODE FEEDBACK 48
3.4 SIMULATION RESULTS 50
3.4.1 Conversion gain 51
3.4.2 Noise simulation 55
3.4.3 Gain compression 56
3.4.4 Common mode feedback circuit 60
References 63
Appendix A – MATLAB CODE 65
TxRx_tb.m 65
UWB_Tx.m 66
UWB_Rx.m 67
integreate_dump.m 68
delay.m 68
Appendix B – Verilog-A CODE 70
Appendix C – OCEAN CODE 71

List of Figures

Figure 1.1: FCC's spectral mask for indoor communications applications. (1; 2) 1
Figure 1.2: A RAKE receive with K fingers (5) 5
Figure 1.3: A non-coherent transmitted reference (TR) receiver structure (5) 5
Figure 1.4: A non-coherent energy detector (ED) receiver structure (5) 6
Figure 1.5: System Block diagram 7
Figure 1.6: BER versus SNR curve for conventional energy detection receiver (CEDR) (14) 8
Figure 2.1: Resistve terminated LNA 13
Figure 2.2: Common gate LNA 13
Figure 2.3: Resistive feedback LNA 14
Figure 2.4: Common source with inductive degeneration LNA 15
Figure 2.5: A graphical illustration of the multi-dimensional optimization problem faced in LNA design 16
Figure 2.6: The proposed LNA with current-reused technique 17
Figure 2.7: Input matching network 18
Figure 2.8: Cascode current mirror for LNA biasing 19
Figure 2.9: The output buffer 20
Figure 2.10: The input reflection coefficient S_{11} 21
Figure 2.11: Noise Figure 22
Figure 2.12 The power gain S_{21} 22
Figure 2.13: Revere isolation S_{12} 23
Figure 2.14: Stability factor K_f 23
Figure 2.15: Alternative stability factor B_{1f} 24
Figure 2.16: 1dB compression point 24
Figure 2.17: The input refered IP3 at 4 GHz 25
Figure 2.18: S_{11} process corners results 26
Figure 2.19: S_{11} worst case corner 26
Figure 2.20: S_{21} process corners results 27
Figure 2.21: S_{21} worst case corners 27
Figure 2.22: NF process corners results 28

Figure 2.23: NF worst case corner 28
Figure 2.24: S_{12} Process corners results 29
Figure 2.25: S_{12} worst case corner 29
Figure 2.26: K_f process corners results 30
Figure 2.27: B_{1f} process corners results 30
Figure 2.28: P_{1dB} worst case corner 31
Figure 2.29: The input reflection coefficient S_{11} 32
Figure 2.30: Noise Figure 33
Figure 2.31: The power gain S_{21} 33
Figure 2.32: Reverse isolation S_{12} 34
Figure 2.33: Stability factor K_f 34
Figure 2.34: Alternative stability factor B_{1f} 35
Figure 2.35: 1dB compression point 35
Figure 2.36: The input referred IP3 at 4 GHz 36
Figure 2.37: S_{11} process corners results 37
Figure 2.38: S_{11} worst case corner 37
Figure 2.39: S_{21} process corners results 38
Figure 2.40: S_{21} worst case corners 38
Figure 2.41: NF process corners results 39
Figure 2.42: NF worst case corner 39
Figure 2.43: S_{12} process corners results 40
Figure 2.44: S_{12} worst case corner 40
Figure 2.45: K_f process corners results 41
Figure 2.46: B_{1f} process corners results 41
Figure 2.47: IIP_3 worst case corner 42
Figure 2.48: Circuit layout 43
Figure 3.1: A conventional Gilbert cell 45
Figure 3.2: Schematic diagram of the squarer 46
Figure 3.3: Schematic diagram of the current mirrors 48
Figure 3.4: Schematic diagram of the CMFB circuit 49
Figure 3.5: Schematic diagram of a resistive divider circuit 50

Figure 3.6: Schematic diagram of the pulse model 52
Figure 3.7: Ultra-wideband pulse waveform 52
Figure 3.8: Squarer output waveform 53
Figure 3.9: Squarer output waveform across corners 54
Figure 3.10: Squarer input power versus output power 57
Figure 3.11: 1 dB compression for highest gain corner 58
Figure 3.12: 1 dB compression for lowest gain corner 58
Figure 3.13: Conversion gain (dB) versus squarer input power (dBm) for the typical case 59
Figure 3.14: Conversion gain (dB) versus squarer input power (dBm) for the max case 59
Figure 3.15: Conversion gain (dB) versus squarer input power (dBm) for the min case 60
Figure 3.16: AC response of the CMFB circuit 61
Figure 3.17: Loop gain of the CMFB circuit 61

List of Tables

Table 1.1: System specs 8
Table 1.2: Spec results summary 9
Table 2.1 :Packages that were used from the Cadence Virtuoso Software Suite and their functionality 11
Table 2.2: Desired LNA Specifications 12
Table 2.3: Comparison between various LNA topologies 16
Table 2.4: Transistors sizing and components values for TSMC13RF design kit 21
Table 2.5: Achieved results using TSMC13RF design kit 25
Table 2.6: Summary of the process corners performance of the LNA 31
Table 2.7: Transistors sizing and components values for LF15RF design kit 32
Table 2.8: The achieved results using LF15RF design kit 36
Table 2.9: Summary of the process corners performance of the LNA 42
Table 2.10: The main positive and negative points of the two design kits 44
Table 3.1: Squarer Best and worst corners 55
Table 3.2: Summary of squarer corners 55
Table 3.3: Summary of squarer noise results 56
Table 3.4: Summary of squarer achieved specs 62

Acknowledgements

We would like to thank Prof. Hani Fikry, our project supervisor for all help and support. Great thanks to Eng. Joseph Riad for greatly helping us throughout the year, maintaining the design tools and kits and giving us advice during circuit design. Thanks to Dr. Mohammed El Nozahi for helping us getting the design kits. Thanks to Eng. Samer Bahr for helping us during the circuit design.

Chapter 1 - INTRODUCTION AND SYSTEM ARCHITECTURE

The need for low-power communication has been increasing more and more in the last few years. The increasing popularity of portable devices enhances this need. The low transmitted power in addition to the system simplicity make ultra-wideband to be a promising technology that can be used to achieve superior power performance over regular narrowband receiver in short-range communications.

In April 2002, after extensive commentary from industry, the FCC issued its first report and order on ultra-wideband technology, thereby providing regulations to support deployment of ultra-wideband radio systems. This FCC action was a major change in the approach to the regulation of RF emissions, allowing a significant portion of the RF spectrum, originally allocated in many smaller bands exclusively for specific uses, to be effectively shared with low-power UWB radios. (1)

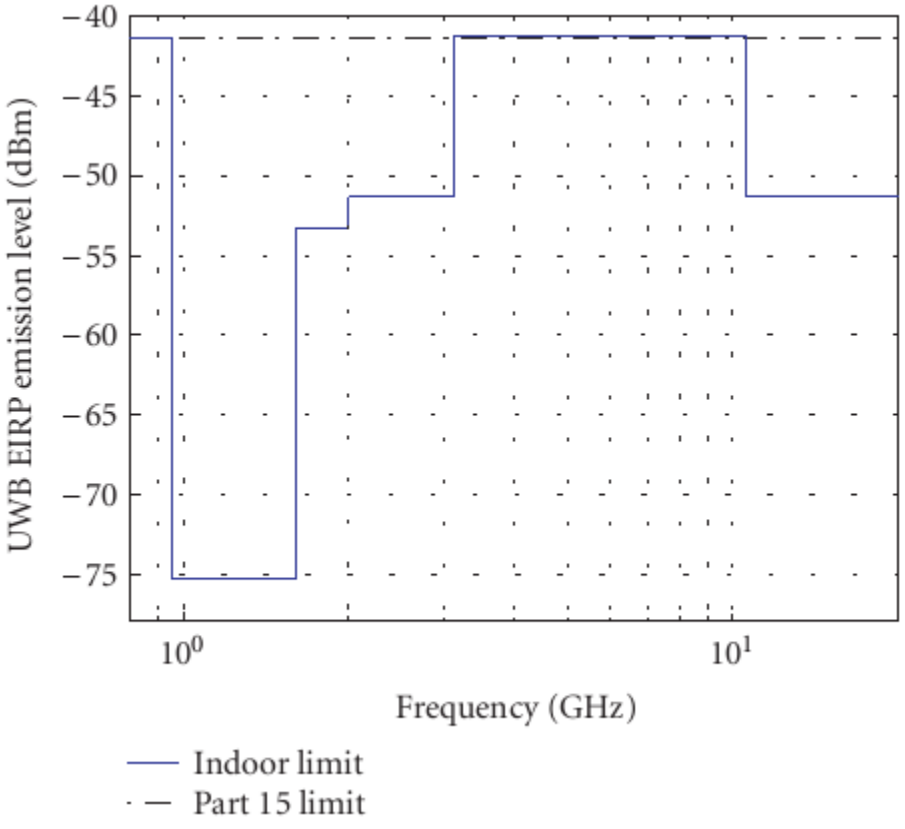

Figure 1.1: FCC's spectral mask for indoor communications applications. (1; 2)

The FCC limits the EIRP emission level in the 3.1-10.3 GHz to -41.3 dBm/MHz, which is a very low level compared to common narrowband standards.

The usage of ultra-wideband in receiver involves on of two main methods:

- Impulse radio (IR): In which a very short pulse in time domain is sent taking a large bandwidth in frequency domain. This whole bandwidth is treated as one channel. Many modulation schemes may be used in this case such as pulse amplitude modulation (PAM), pulse position modulation (PPM) or on-off keying (OOK).
- OFDM: In which the large bandwidth is divided into a number of channels, each channel is carried over a different subcarrier. This enables taking this large bandwidth with easier combat for multipath fading.

1.1 ULTRA-WIDEBAND DEFINITION

For a radiator to be considered UWB, the 10dB bandwidth $f_H - f_L$ must be at least 500MHz, and the fractional bandwidth B_f must be at least 0.2 (1). The fractional bandwidth is defined as:

$$\boldsymbol{B_f = 2\frac{f_H - f_L}{f_H + f_L} = \frac{f_H - f_L}{\left(\frac{f_H + f_L}{2}\right)} = \frac{Bandwidth}{Center\ Frequency}} \qquad \textbf{(1.1)}$$

where f_H and f_L are the -10 dB power points. So for an ultra-wideband signal:

$$\boldsymbol{2\frac{f_H - f_L}{f_H + f_L} > 0.2} \qquad \textbf{(1.2)}$$

1.2 ULTRA-WIDEBAND UNIQUE FEATURES

1.2.1 Ultra-wideband and Shannon's theorem

According to Shannon's theory the channel capacity C, meaning the theoretical tightest upper bound on the information rate (excluding error correcting codes) of clean (or arbitrarily low bit error rate) data that can be sent with a given average signal power S through an analog communication channel subject to additive white Gaussian noise of power N, is (3):

$$\boldsymbol{C = Blog_2(1 + SNR)} \qquad \textbf{(1.3)}$$

where B is the bandwidth of the channel, SNR is the signal-to-noise ratio.

Shannon's theory shows that the channel capacity increases linearly with the channel bandwidth and increases with log of the SNR. This means that a for a low-data-rate transmission, the SNR required to receive the signal with a suitable BER is greatly reduced for the case of

ultra-wideband transmission. This enables receiving the signal despite the low limit that the FCC puts on the power transmitted from ultra-wideband systems.

On the other hand, Shannon's theory also means that ultra-wideband systems may be used to transmit a very large data rate at a reasonable SNR, enabling the use of ultra-wideband systems in short-range very high data rate systems.

1.2.2 The coexistence of ultra-wideband and narrowband signals

The frequency band dedicated by the FCC for ultra-wideband transmission is also allocated for many other standards that should transmit on the same band at the same time. However, the narrowband and ultra-wideband signals can coexist without interfering with each other.

Due to the very low power spectral density limit on the ultra-wideband signals, multiplying this low PSD with the narrow bandwidth of the narrowband signals results in narrowband receivers taking just a very small amount of power and hence the narrowband receiver finds a small rise in its noise floor without affecting its operation as it only took a very small portion of the wideband pulse.

On the other hand, the ultra-wideband receiver detects pulses present in the large bandwidth without being affected much by narrowband signals that have no pulses.

1.2.3 Time resolution

The time resolution T_{res} of a matched receiver generally is on the order of the reciprocal of the RF Gabor (RMS) bandwidth B_{RF} (1):

$$\boldsymbol{T_{res} \cong \frac{1}{B_{RF}}} \qquad \textbf{(1.4)}$$

This gives a corresponding range resolution in positioning systems on the order of $\frac{c}{B_{RF}}$, where c is the speed of light. This time-resolution measure is well known in radar circles as a measure of the width of the peak of a matched-filter response to a waveform of RMS bandwidth B_{RF}. Although. (1)

1.3 IMPULSE RADIO (IR) ULTRA-WIDEBAND RECEIVER ARCHITECTURES

In this section, we represent an overview on different receiver architectures that are used for ultra-wideband signal detection. For IR-UWB systems, coherent and non-coherent receivers implemented either in digital or analog domain can be used for detection of distorted and noisy received signal. The implementation of all-digital receiver requires high-sampling frequency ADCs, and its high-data-rate solutions also need large memory and high processing speeds, which makes it expensive to implement (4). Alternatively, a fully analog implementation of IR-UWB receiver can provide a simple and low-cost receiver. The coherent and non-coherent IR-UWB receivers are discussed briefly in the following subsections. (5)

1.3.1 Coherent receivers

The coherent receivers correlate the received signal with a locally generated reference (LGR) template (6). However, to correlate the received UWB signal with LGR template, the receiver needs to achieve the pulse-level synchronization with accuracy on the order of tens of picoseconds (7).

The coherent RAKE receivers take advantage of the time-diversity provided by multipath channel. This scheme was invented by Price and Green (8) in 1958. It consists of a bank of matched filters (also called fingers) with each finger matched to a different replica of the same transmitted signal, as shown in Figure 1.2. The outputs of the fingers are appropriately weighted and combined to reap the benefits of multipath diversity (6). The coherent RAKE receivers require accurate synchronization and the knowledge of channel impulse response.

1.3.2 Non-coherent receivers

The non-coherent receivers do not require channel estimation and have low complexity implementation at the expense of performance loss. The sub-optimal non-coherent receivers are suitable for low power and low-cost scenarios such as wireless sensor networks. Transmitted reference (TR) receiver and energy detector (ED) are two popular non-coherent detection schemes for IR-UWB signals. (5)

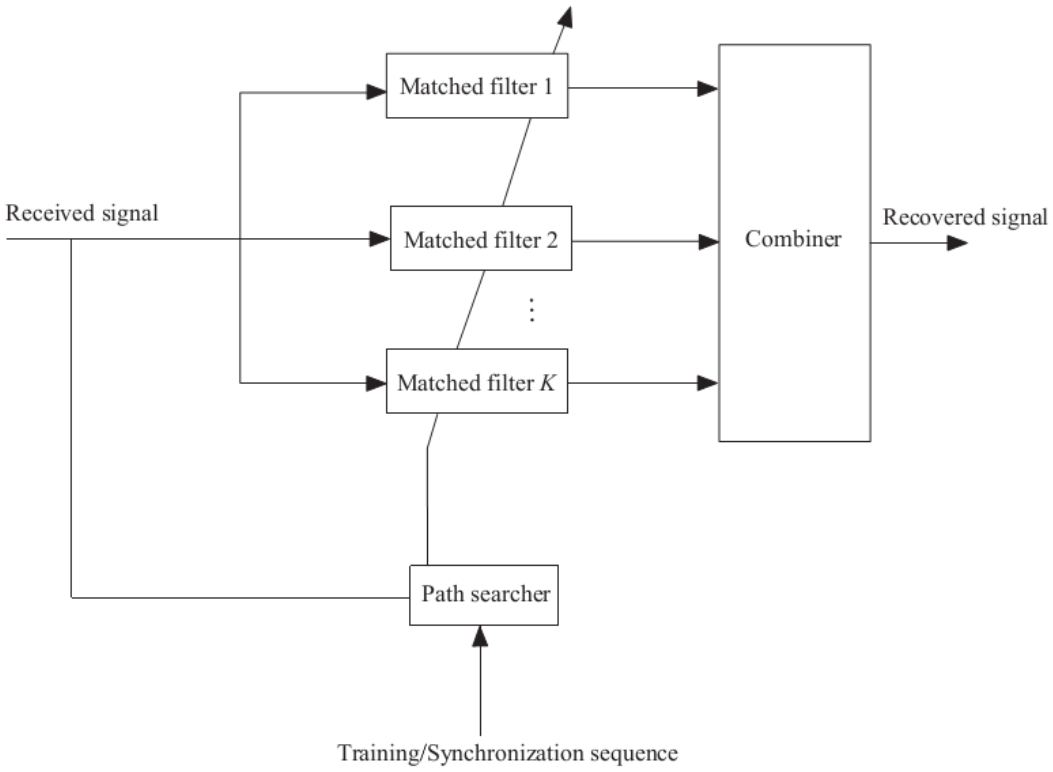

Figure 1.2: A RAKE receive with K fingers (5)

1.3.2.1 Transmitted Reference receivers (TR)

The non-coherent transmitted reference receiver shown in Figure 1.3 is used to demodulate the signal transmitted using TR modulation. TR receiver delays the reference signal and correlates it with data-modulated signal in each frame. The decision statistic is acquired by adding the correlations over N_f frames. TR receivers exploit multipath diversity inherent in the environment without the need for stringent acquisition and channel estimation (9). On the other hand, TR receiver suffers a 3 dB penalty because half of the pulses are unmodulated (10).

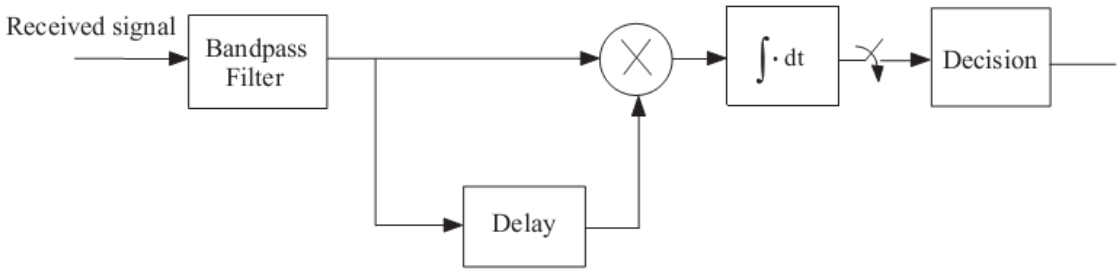

Figure 1.3: A non-coherent transmitted reference (TR) receiver structure (5)

1.3.2.1 Energy detection receivers (ED)

Energy detector is a non-coherent approach for UWB signal reception, as shown in Figure 1.4, where low complexity receivers can be achieved at the expense of some performance degradation (11), (12). On-off keying (OOK) is one of the most popular non-coherent modulation options that has been considered for energy detectors (13). OOK based implementation of energy detectors is achieved by passing the signal through a square law device followed by an integrator and a decision mechanism, where the decisions are made by comparing the outputs of the integrator with a threshold (13). Pulse position modulation (PPM) can also be used for non-coherent energy detector (ED) receiver (5).

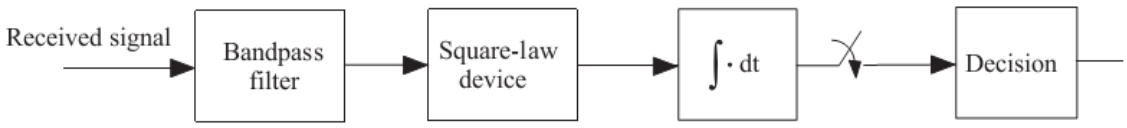

Figure 1.4: A non-coherent energy detector (ED) receiver structure (5)

1.4 THE IMPLEMENTED RECEIVER ARCHITECTURE

The Energy detection receiver architecture was chosen to be implemented in this project. This is mainly due to the relatively simple receiver and transmitter circuits. In addition to low area and cost, choosing this simple architecture greatly reduces the power consumption of the receiver. On-off keying (OOK) modulation scheme was chosen for its simplicity.

The receiver block diagram is shown in Figure 1.5. The received signal from the antenna passes first through an LNA to get some gain without adding much noise as the received signal from the antenna has a very small amplitude and any added noise significantly degrades the SNR.

Then a VGA block is added after the LNA for two reasons. First, the gain of the wideband LNA has large variation across corners. Second, the squarer gain is function of its input power due to the inherent squaring action and hence adjusting the power of the squarer input to a known value for all received powers is highly recommended.

After the VGA, a squarer circuit multiplies the received pulse by itself; this causes the wideband received signal to have a component around the DC and a component around twice the center frequency. The component around twice the center frequency is filtered by the output pole

of the squarer circuit. The resulting signal is integrated and when the integrator output reaches a certain threshold value a dump signal is sent to the integrator and the output of the receiver goes high indicating receiving a pulse and the OOK signal is received.

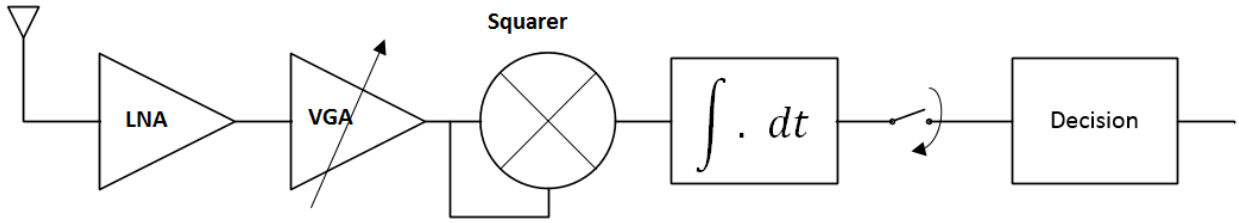

Figure 1.5: System Block diagram

The receiver system was simulated using MATLAB code, which is included in Appendix A.

1.5 SYSTEM PERFORMANCE AND SPECS

In the IEEE 802.15.6 standard for local and metropolitan area networks, it is stated that for on-off modulation of an ultra-wideband receiver the receiver sensitivity should be equal to -88 dBm at a data rate of 0.7897 Mbps and -85 dBm at a data rate of 1.579 Mbps. Since the desired data rate is 1 Mbps, the receiver sensitivity is about -87.2 dBm.

To achieve a receiver sensitivity of -87.2 dBm at a data rate of 1 Mbps. The receiver sensitivity is given by:

$$\boldsymbol{P_{sens} = -174\ dbm + 10\log(BW) + NF + SNR_{min}} \qquad \textbf{(1.5)}$$

where BW is the signal bandwidth, NF is the total receiver noise figure and SNR_{min} is the minimum SNR that must be achieved at the receiver output to achieve the maximum acceptable bit error rate (BER). For impulse ultra-wideband radio, the maximum acceptable BER is usually taken to be 10^{-3}. To get the SNR_{min} corresponding to 10^{-3} BER, we use the BER versus SNR curve corresponding to this receiver as shown in Figure 1.6 (14). It is seen from the figure that the $\frac{E_b}{N_0}$ corresponding to 10^{-3} BER for a conventional energy detection receiver (CEDR) is about 18 dB. The SNR_{min} of the received signal is given by:

$$SNR_{min} = \frac{E_b R_b}{N_o BW} = 10^{\frac{18}{10}} * \frac{1*10^6}{2*10^9} = 0.0315 = -15 \text{ dB}$$

where the chosen signal bandwidth is 2 GHz in the range 3.1-5.3 GHz.

The total noise figure of the receiver is hence found to be:

$$NF = P_{sens} + 174\ dbm - 10\log(BW) - SNR_{min}$$
$$= -87.2 + 174 - 10\log(2 * 10^9) + 15 = 8.8\ dB$$

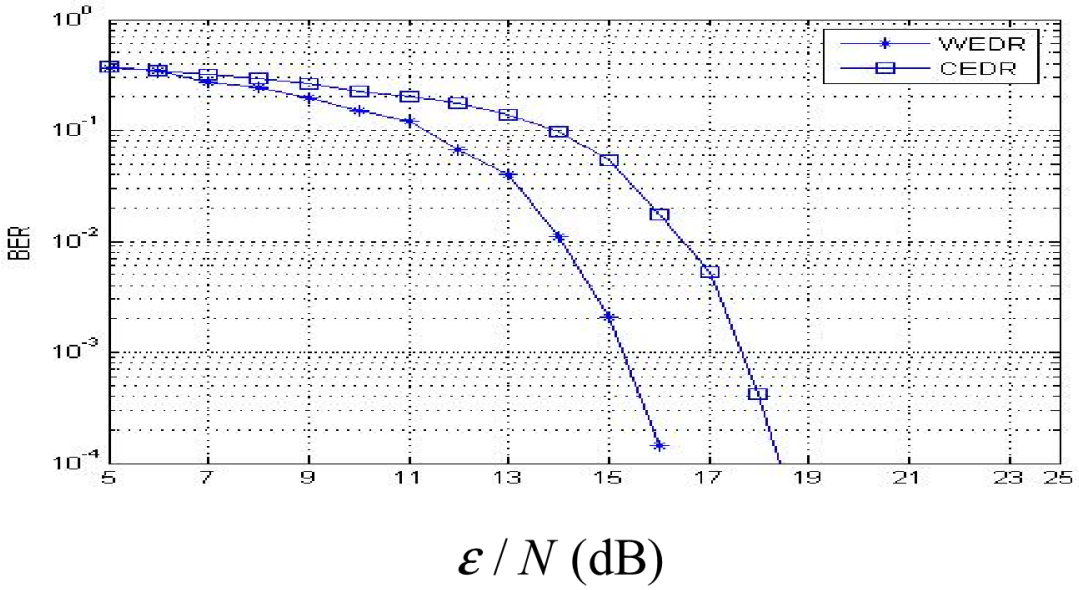

Figure 1.6: BER versus SNR curve for conventional energy detection receiver (CEDR) (14)

This noise figure as well as the gain should be distributed on the receiver chain. The noise figure spec should be harder on the first stages and should be relieved for subsequent stages where the signal is larger and noise contribution become negligible compared to the signal. The proposed system specs are as shown in Table 1.1:

Block	Min Gain (dB)	Max NF (dB)
LNA	7	5.5
VGA	33 (max)	12
Squarer	0	30
Integrate and Dump	5	35

Table 1.1: System specs

The implemented blocks at circuit level of this system were the LNA and the squarer. The desired specs versus the achieved specs for these two blocks are shown in Table 1.2:

Spec	Required	Achieved at Worst Corner
LNA Gain	> 7 dB	7.6 dB
LNA NF	< 5.5 dB	5.4 dB
Squarer Gain	> 0 dB	0.9 dB
Squarer NF	< 30 dB	28.4 dB

Table 1.2: Spec results summary

The squarer worst case Gain is based on the fact that at a sensitivity of -87.2 dBm, the worst case corner input power to the squarer is equal to -87.2+7.6+35 = -44.6 dBm.

Chapter 2 - LOW NOISE AMPLIFIER DESIGN AND SIMULATION

2.1 INTRODUCTION

The LNA (Low Noise Amplifier) is a critical component in the receiver architectures and presents a considerable challenge for its simultaneous requirements to achieve high gain, low noise and excellent input matching, unconditionally stability and low power consumption. Also, a large signal or blocker can occur at the input of LNA. The circuits should be sufficiently linear in order to have a reasonable signal reception. The problem becomes more severe at high frequencies due to the parasitics that become effective at high frequency of operation.

The LNA is designed for the operation over the 3.1 GHz to 5.3 GHz range. The configuration was simulated using Spectre with two different design kits. An optimized design is presented using TSMC13RF (Taiwan Semiconductor Manufacturing Company 130 nm for RF Design) and this design is migrated to LF15RF (LFoundry 150 nm for RF Design) due to the relative low cost of the latter one. The difference in performance between the two design kits and the design tradeoffs between them is reported. Also, a final conclusion is presented with the main positive and negative points of each design kit.

The circuit topology is also a crucial consideration as it determines the minimum and maximum performance boundaries and the consequential tradeoffs in order to release the LNA in such a high and large operating frequency range. The current reused configuration (15) is chosen based on its ability to provide two of the most important parameters in LNA design: high gain and relatively low power compared to other topologies. Also, the cascode configuration is added to the current reused configuration to get the advantages of the suppression of the Miller effect, high gain that reduces the input referred noise and stability improvement due to the high reverse isolation characteristics. Two disadvantages of the chosen configuration are the higher voltage headroom required due to the stacked transistors and reduction of linearity due to reduced output swing.

The schematic entry, simulations and layout were done using Cadence Virtuoso version IC6.1.5.500.132. Details on the packages that were used are provided in Table 2.1

Package name	Functionality
Virtuoso Schematic Editor	Graphical user interface for schematic entry
Analog Design Environment (ADE) and Spectre version IC6.1.5.500.132.	ADE is graphical user interface that can be used to compile the simulator input file for various IC simulators, such as Spectre.
Virtuoso Layout Editor	Graphical user interface for drawing circuit layouts
Assura	Design rule check (DRC) Layout versus schematic check (LVS)

Table 2.1 :Packages that were used from the Cadence Virtuoso Software Suite and their functionality

The MOSFET transistor model used in the simulations of both design kits TSMC13RF and LF15RF is BSIM3V3. Simulations were done with temperature specified at 27 ºC which is frequently assumed as room temperature. All simulations were done using parameterized cells which includes all device parasitics.

Small-signal simulations were used to find the input return loss, the forward gain, noise figure (NF) and the reverse isolation of the LNA. Process corners simulations were performed to find the variation of performance measures with process, supply voltage and temperature changes. Large signal analysis was used to determine the IIP3 and P_{1dB} of the LNA.

2.2 OJECTIVES AND TARGTED SPECIFICATIONS

One of the major challenges for both UWB systems is the design of a wideband low noise amplifier (LNA). As the first active component in the receiver chain, the LNA should provide sufficient gain and sufficiently low noise to keep the overall receiver noise figure (NF) as low as possible. In most applications, obtaining wideband input matching, good linearity, and low power consumption is desirable. In addition, gain flatness over the entire frequency range of interest is necessary to meet design specifications.

There are two main objectives of this part of the project; the first objective is to design an optimized LNA using TSMC13RF design kit fulfilling the system requirements and specifications as shown in Table 2.2.

Parameter	Specifications
Bandwidth	3.1 GHz to 5.3GHz
Input Reflection Coefficient (S_{11})	< -10 dB
Noise Figure (NF)	< 4dB
Gain (S_{21})	14 dB to16 dB
Power	Lowest possible
IIP_3	> -15 dBm

Table 2.2: Desired LNA Specifications

The second objective is to migrate this design to another technology using different design kit which is LF15RF for fabrication purposes and to report the deviation in performance between the two designs and the main positive and negative points of the two design kits.

2.3 DIFFERENT LNA TOPOLOGIES

The LNA usually involves one or two transistors and sometimes three to achieve low noise operation and high gain at low power. The performance of the LNA circuits is very dependent on process technology. CMOS technologies are the best choice to design an LNA because they offer high speed operation, simplicity in fabrication, and low power consumption. The following discussion presents several popular LNA structures possible in a CMOS integrated circuit. The LNA input is directly connected to a filter for impedance and noise matching. Therefore, different LNA structures have different methods to achieve impedance matching.

The structure shown in Figure 2.1 achieves input impedance matching by directly placing a 50 Ω resistor (R_s) in parallel with the gate of transistor M_1. This is the most straightforward method but the noise figure will be exceptionally high.

The lower bound of the LNA noise figure is given by:

$$NF \geq 2 + \frac{4\gamma}{g_{m_1} R_s}$$

The noise figure is readily larger than 4 dB. The primary contribution of noise comes from the termination resistor R_s and the drain of the transistor M_1. Due to the noise performance limitations this LNA structure is rarely used.

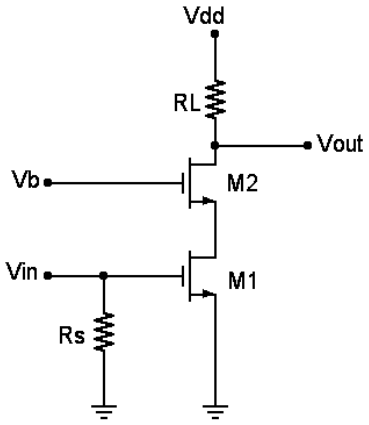

Figure 2.1: Resistve terminated LNA

A common gate amplifier structure, shown in Figure 2.2, has better input impedance than a common source structure. For the first order approximation, the essential part of input impedance is just l/gm.

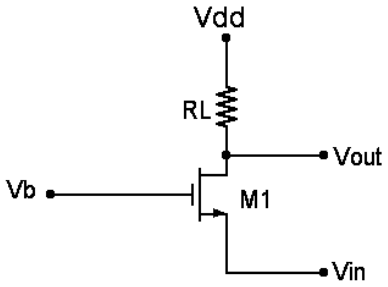

Figure 2.2: Common gate LNA

By carefully choosing the size of the transistor and biasing conditions, the 50 Ω impedance matching can be easily obtained. Ignoring the gate current noise, a lower bound of noise figure for this topology is represented by: $NF \geq 1+\gamma$ .This minimum noise factor is about 4 dB for short channel device. The gate current noise will make the noise factor larger, but the drain noise will still be the dominant factor.

The resistive feedback LNA, shown in Figure 2.3, uses negative shunt feedback to modify the input impedance of a common source stage. Its input impedance under matching condition can be calculated by: $Z_{in} = \frac{R_F}{A_v}$ where A_v is the voltage gain and it's approximately equals to $g_{m1}R_F$.

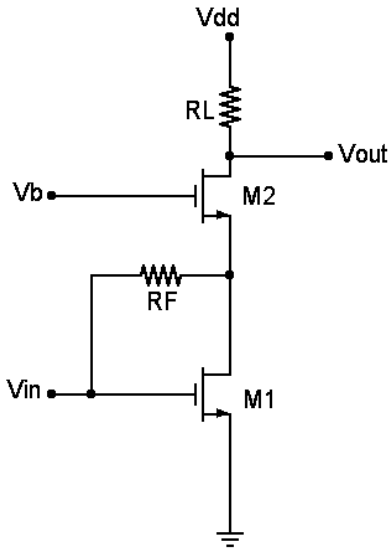

Figure 2.3: Resistive feedback LNA

The noise figure of this structure is given by: $NF \geq 1+\gamma$ It is better than that of the resistively terminated LNA structure but it is still too high to use in applications such as a UWB receiver. Also, this topology is limited by the frequency of operation it can't be used at high frequencies due to the presence of feedback.

Figure 2.4 shows one of the most interesting and important structures of the LNA. Common source with inductive degeneration LNA is one of the topologies that can be used to obtain a very low noise figure that can reach 1 dB at resonance frequency ω_o that not exceed 1 GHz but unfortunately it's a narrow band configuration. The resonance frequency is given by:

$$\omega_o = \frac{1}{(L_g + L_s)C_{gs}}$$

The input impedance is given by:

$$Z_{in} = \frac{1}{sC_{gs1}} + sL_s + \frac{g_{m1}L_s}{C_{gs1}}$$

$$Z_{in} = \frac{1}{sC_{gs1}} + sL_s + \omega_\tau L_s$$

The noise figure at resonance frequency and under matching conditions is given by:

$$NF = 1 + g_{m1} R_s \gamma \left(\frac{\omega_o}{\omega_\tau} \right)^2$$

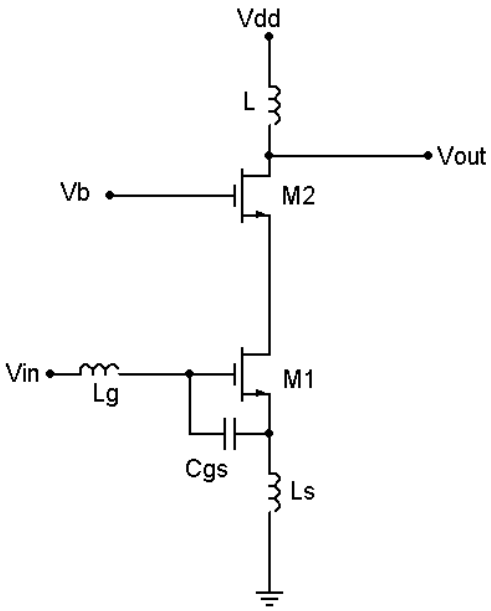

Figure 2.4: Common source with inductive degeneration LNA

Table 2.3 compares all the topologies discussed before. As shown in Table 2.3 it can be proven that common source with inductive degeneration LNA has a good narrowband matching and a very small noise figure. Good input matching and low noise figure are essential requirements for any UWB LNA design. Since UWB is such a low power technology, one cannot afford to add too much noise into the system. Research has shown that the source degeneration is the best suitable topology for the UWB related LNA. The next section discusses the design and simulations for the proposed LNA that employs inductive degeneration technique as one of the main techniques used to achieve low noise and good input matching in addition to other techniques used to achieve high gain, stability and low power consumption. These techniques are discussed in the next section.

Topology	Plus Point	Minus Point
Resistive termination	Good input matching (Wideband)	Huge NF and low gain
Common gate	Good input matching (Wideband)	Large NF and low gain
Resistive feedback	Good input matching (Wideband)	Operation at low frequencies, low gain and stability issues
Common source with inductive degeneration	Good narrow band matching, small noise figure at resonance frequency	Large area due to inductor L_g It can be off chip but this will increase the cost

Table 2.3: Comparison between various LNA topologies

2.4 PROPOSED LNA DESIGN

The key performance requirements for LNAs are power gain, NF, linearity, stability, impedance matching, power dissipation bandwidth and design robustness with respect to process, voltage and temperature variations. Typically these requirements are universal making LNA design a multi-dimensional optimization problem. The requirements are graphically illustrated in Figure 2.5.

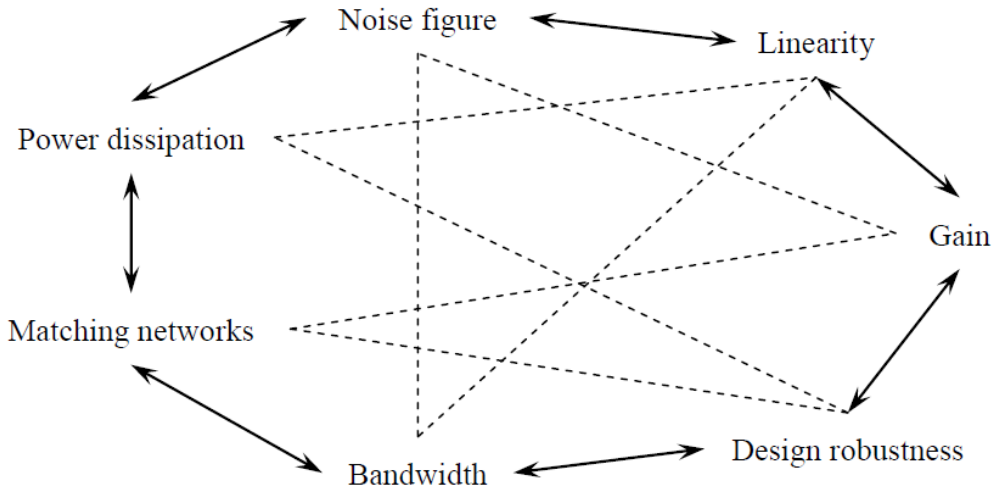

Figure 2.5: A graphical illustration of the multi-dimensional optimization problem faced in LNA design

After the discussion of the main LNA topologies in the previous section it become clear that in order to fulfill the targeted specification mentioned previously a new topology should be introduced, the proposed topology is shown in Figure 2.6. This topology employs the current-reused technique. The current-reused configuration can be considered as a two stage cascade amplifier (AC cascade DC cascode), where the first stage is the common-source amplifier M_1 and the second stage is the cascode amplifier M_2 and M_3. The two amplifying stages are placed on the top of the other. Note that M_3 is a common-gate stage which is used to eliminate the Miller effect and provides a better isolation from the output return signal. The signal amplified by M_1 is coupled to the gate of M_2 by using the inter-stage technique through the coupling capacitor C_g while the source of M_2 is bypassed to ac ground by C_b. The circuit thus saves power through the reuse of the bias current. With this approach, higher gain has been obtained due to the increase in the transconductance ($g_{m1}+g_{m2}$) without both, usage of the cascade configuration and increase in power consumption as two amplifying stages have the same bias current $P_{disp.} = V_{dd} I$ .L_d is used to perform high impedance path for the signal to block it in the desired band and it should exceed a specific value for proper performance of the circuit. As a result the signal flows in the low impedance path of C_g and it is amplified twice under the concurrent structure. To enhance the gain in the desired bandwidth and to compensate the roll of (gain variation) in the upper band L_{pk} is used to perform the inductive peaking.

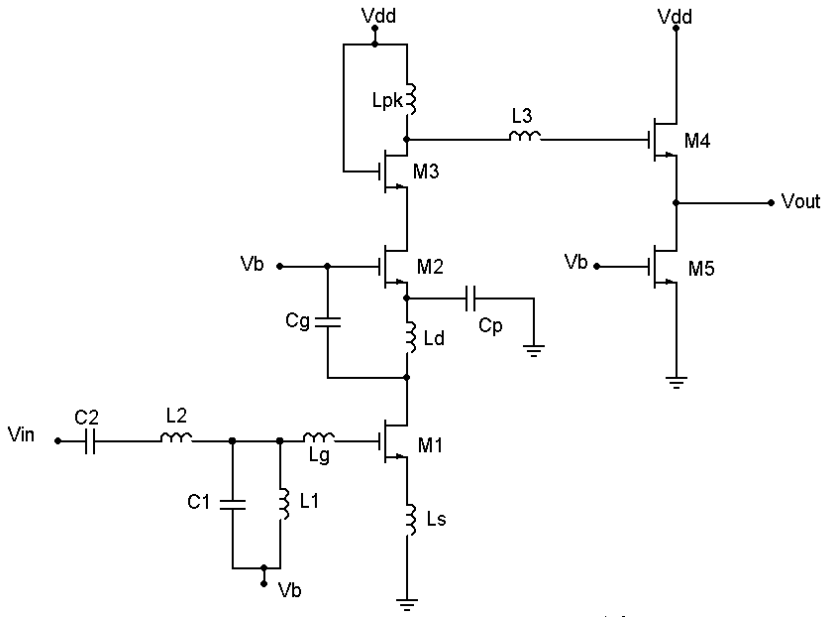

Figure 2.6: The proposed LNA with current-reused technique

2.4.1 Wideband input impedance matching

Input matching to 50 Ω is one of the most challenging issues in the design of wide band LNAs as to achieve S_{11} below 10 dB a third order passive Chebychev band pass filter is used. The input impedance of the amplifier can be approximately given by:

$$Z_{in} = sL_2 + \frac{1}{sC_2} + (sL_1 \| \frac{1}{sC_1} \| Z_g)$$

$$Z_g = \frac{1}{sC_{gs1}} + s(L_s + L_g) + \frac{g_{m1}L_s}{C_{gs1}}$$

The proposed solution expands the basic inductively degenerated common source amplifier by inserting an input multi section reactive network (Chebychev band pass filter), so that the overall reactance can be resonated over a wider bandwidth. This input matching network is shown in Figure 2.7. An inductor (L_g) is placed in series with a capacitor (C_{gs1}) to add flexibility to the design. Different values of L_g and C_{gs1}would give different matching conditions.

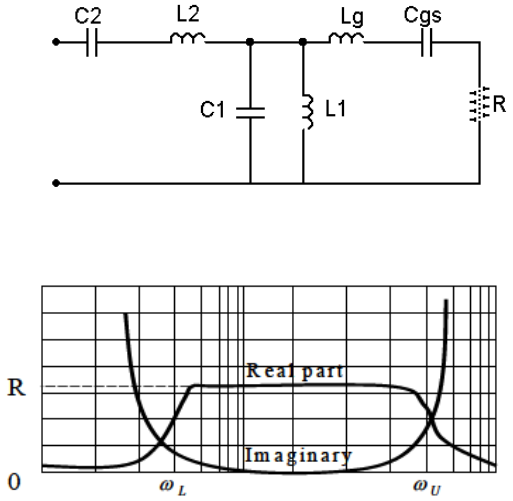

Figure 2.7: Input matching network

$$\omega_L \approx \frac{R}{L_1} \approx \frac{1}{RC_2}$$

$$\omega_U \approx \frac{R}{L_2} \approx \frac{1}{RC_1}$$

Where R is equal to 50 Ω and f_L and f_U are equal to 3.1 GHz and 5.3 GHz respectively.

2.4.2 The design for low noise figure

The current-reused amplifier functions as a two-stage cascade amplifier. The NF of the second stage contributed from both the MOSFETs (M_2 and M_3) and the inductor (L_d) can be reduced by the gain of the first stage (M_1). In addition, the NF originated from (L_{pk}) and the output buffer is reduced twice by the gains of the first and second stages. With this design technique, not only can a high gain be obtained, but a low NF can also be achieved simultaneously. The noise figure can be approximated to be equal to that of the common source with inductive degeneration at a resonance frequency chosen to be 4 GHz at the center of the desired band but it will be slightly higher due to the series resistances of the inductors in the matching network also, the quality factor of the inductors will affect the noise figure at higher frequencies.

2.4.3 The design for flat gain

The load L_{pk} is designed to get flat gain over the whole bandwidth. The value of L_{pk} has a tradeoff between large gain and resonance frequency. The goal is to get a large enough gain over the entire frequency range. Also, L_3 and C_{gs4} resonate at 5.3 GHz to get a flat gain over the whole bandwidth with variations less than 1 dB.

2.4.4 LNA biasing

A simple cascode current mirror Figure 2.8 is used to bias transistors M_1 and M_2. M_3 is directly connected to Vdd. C_B represents a low pass filter that filters the noise coming from the cascode current mirror so as not to affect the noise figure of the LNA (16).

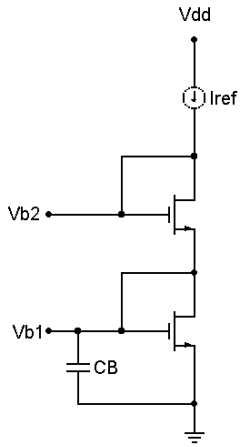

Figure 2.8: Cascode current mirror for LNA biasing

2.4.5 LNA stability

Unconditional stability refers to the situation where the amplifier remains stable throughout the entire domain of the Smith Chart at the selected frequency and bias conditions. Condition can be expressed in terms of the stability factor K_f and the alternative stability factor B_{1f} as shown below:

$$K_f = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{11}||S_{12}|} > 1$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$B_{1f} = 1+|S_{11}|^2-|S_{22}|^2-2|\Delta|^2 > 0$$

2.4.6 LNA figure of merit

The LNA figure of merit (FOM) is given by the equation:

$$FOM = \frac{Gain_{\max dB} BW_{3dBGHz}}{NF_{\min dB} P_{dmW}}$$

2.4.7 Output buffer

The buffer stage (M_4 and M_5) Figure 2.9 must drive a 50 Ω load. Both transistors are required to be in saturation for the chosen biased current.

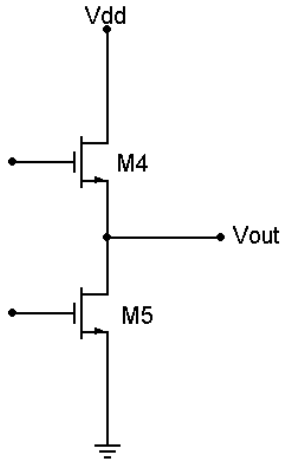

Figure 2.9: The output buffer

2.5 TSMC13RF DESIGN KIT SIMULATION RESULTS

The transistors sizing and the components values of the above design kit is presented in Table 2.4.

Transistors width	M_1 = 210µ, M_2 and M_3 = 190µ, M_4 = 36µ and M_5 = 110µ
Transistors length	130 nm for all transistors
Capacitors	C_1 = 600fF, C_2 = 6pF, C_g = 3pF, C_b = 7pF and C_B = 3pF
Inductors	L_1 = 1.5nH, L_2 = 2nH, L_g = 1.8nH , L_s = 540pH L_d = 3.6nH and L_{pk} and L_3 =1.8nH
Supply voltage	1.2 V
Power dissipation	3.6 mW

Table 2.4: Transistors sizing and components values for TSMC13RF design kit

2.5.1 Small signal simulation

The small signal simulations are performed to evaluate the S-parameters, noise figure and stability parameters.

Figure 2.10 the input reflection coefficient S_{11} is less than -15 dB.

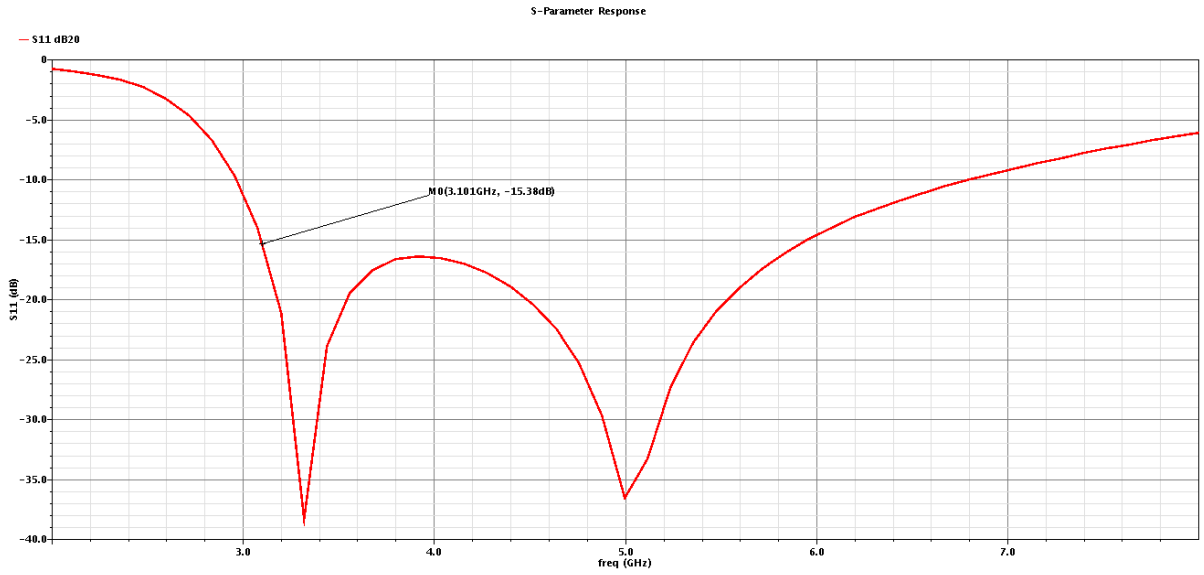

Figure 2.10: The input reflection coefficient S_{11}

Figure 2.11 the noise figure is of maximum value 4 dB at 5.3 GHz and minimum value 3.6 dB at 4 GHz which is the resonance frequency of the inductive degeneration part.

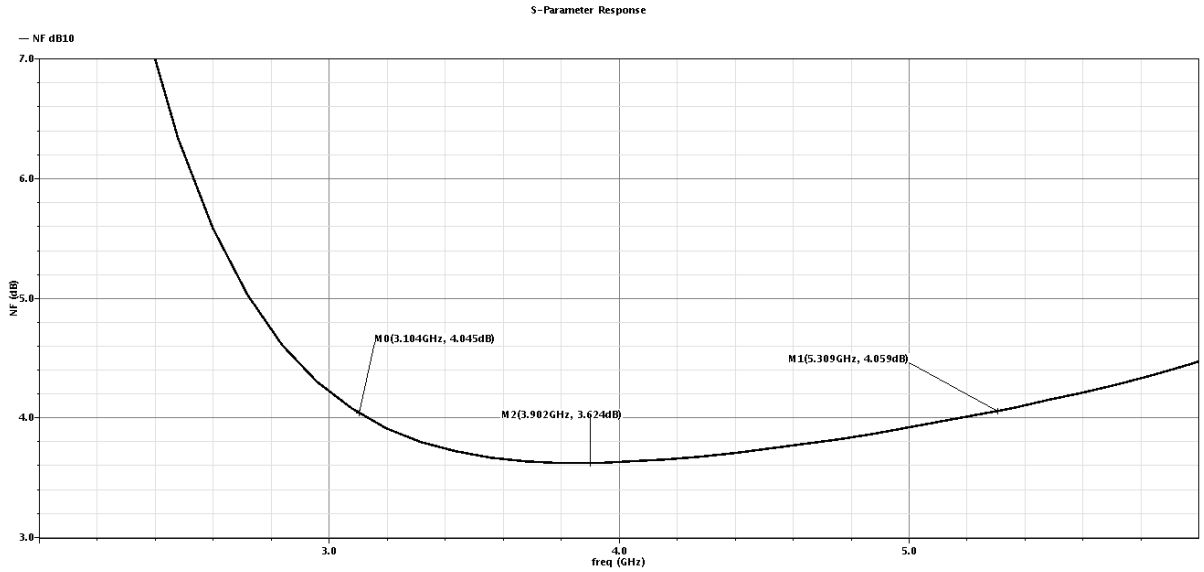

Figure 2.11: Noise Figure

Figure 2.12 the power gain S_{21} of value 15 dB with variations less than 1 dB across the desired band width.

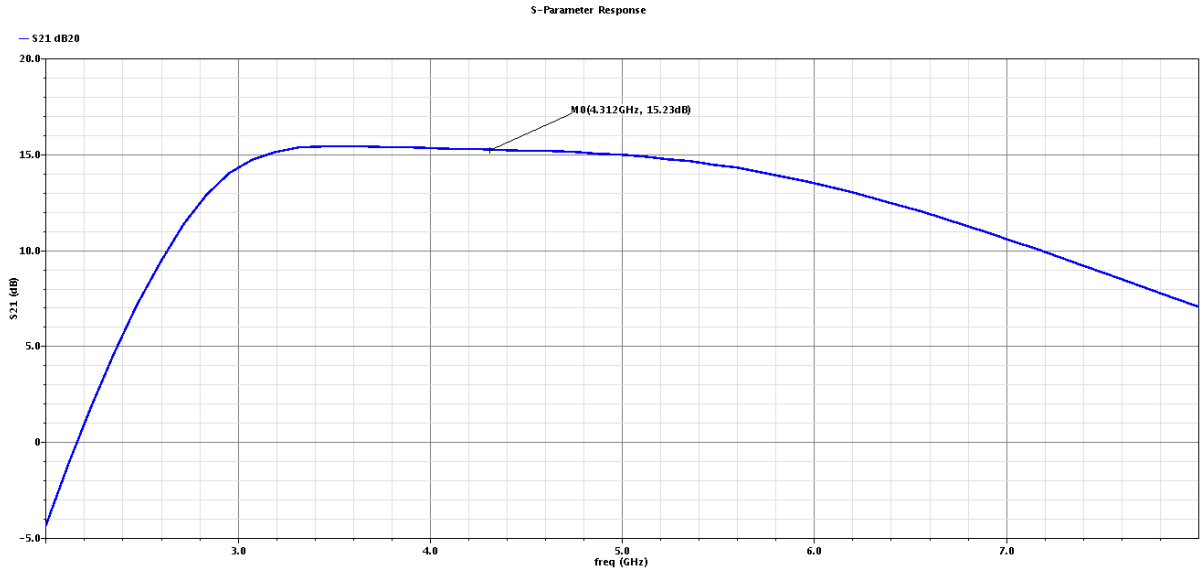

Figure 2.12 The power gain S_{21}

Figure 2.13 the reverse isolation is less than -51dB.

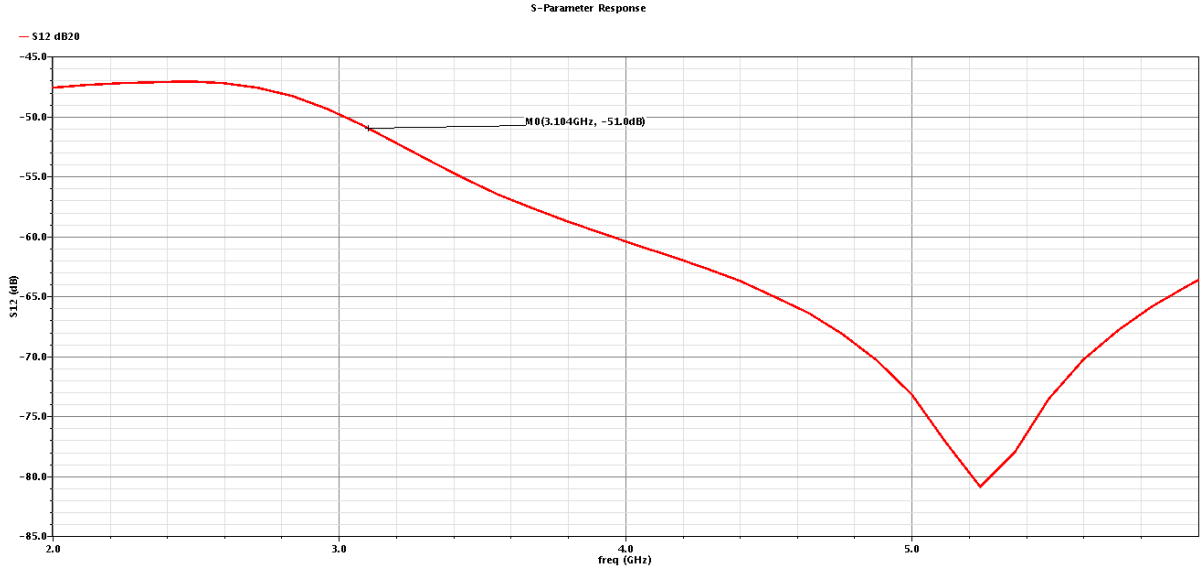

Figure 2.13: Revere isolation S_{12}

Figure 2.14 the stability factor K_f is greater than one across all frequencies.

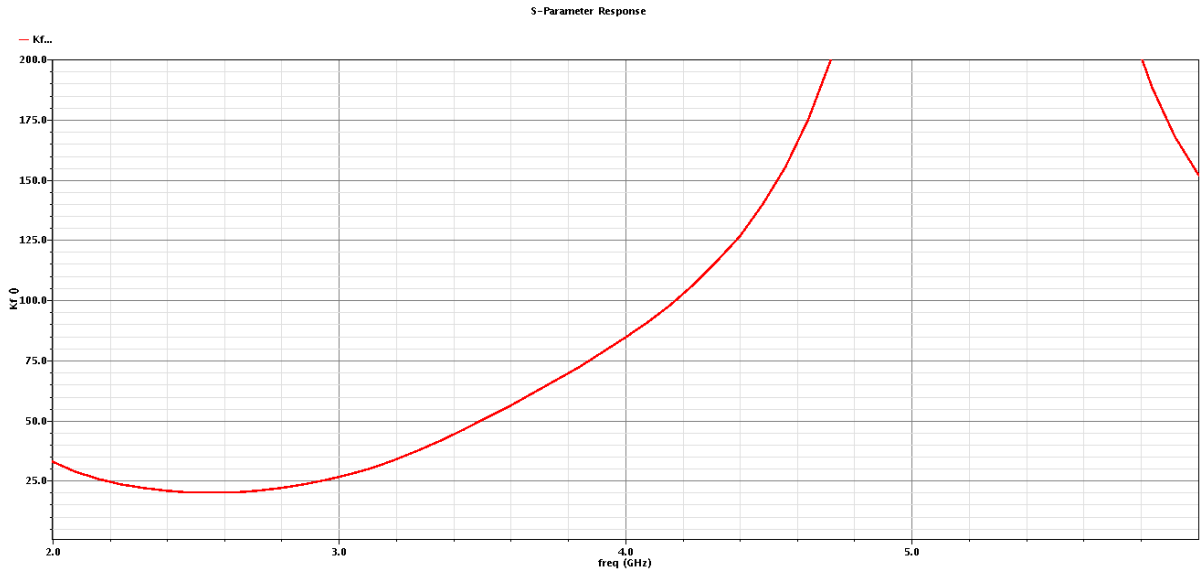

Figure 2.14: Stability factor K_f

Figure 2.15 the alternative stability factor B_{1f} is greater than zero across all frequencies therefore the LNA is unconditionally stable.

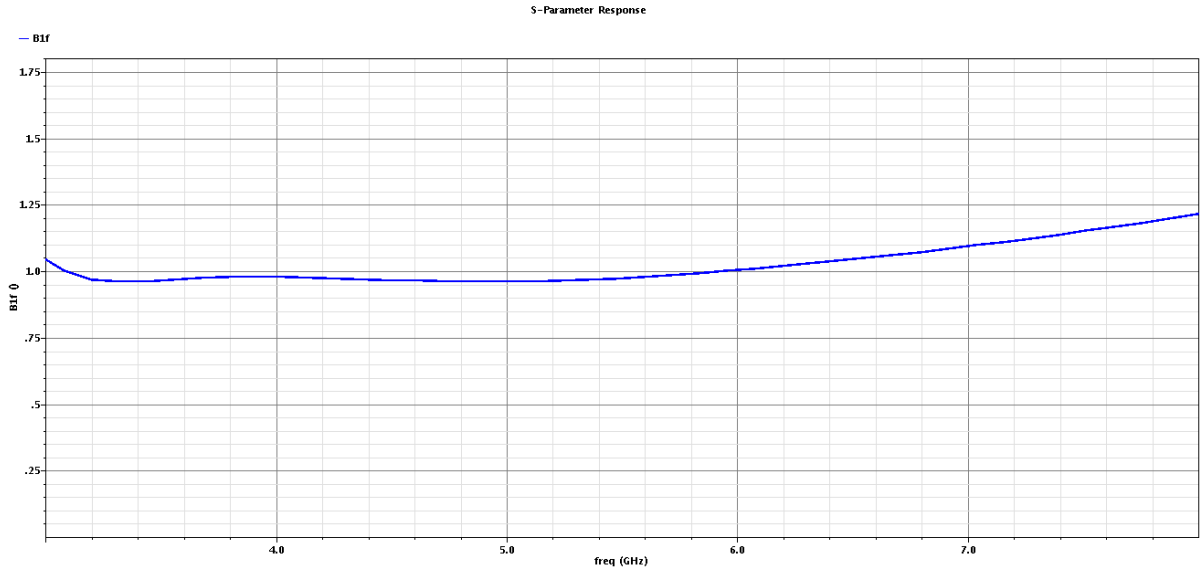

Figure 2.15: Alternative stability factor B_{1f}

2.5.2 Large signal simulation

Figure 2.16 large signal analysis is performed to find the1dB compression point P_{1dB} is equal to -25 dBm.

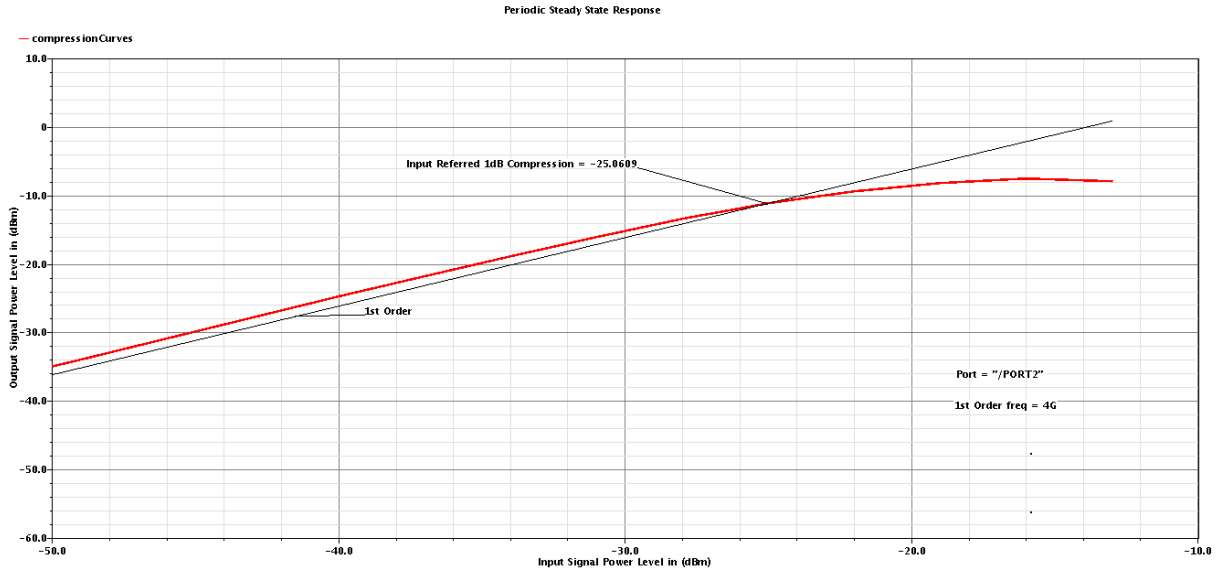

Figure 2.16: 1dB compression point

Figure 2.17 the IIP_3 is evaluated at 4 GHz with two blockers at frequencies 4.1 GHz and 4.2 GHz it is found to be -17 dBm.

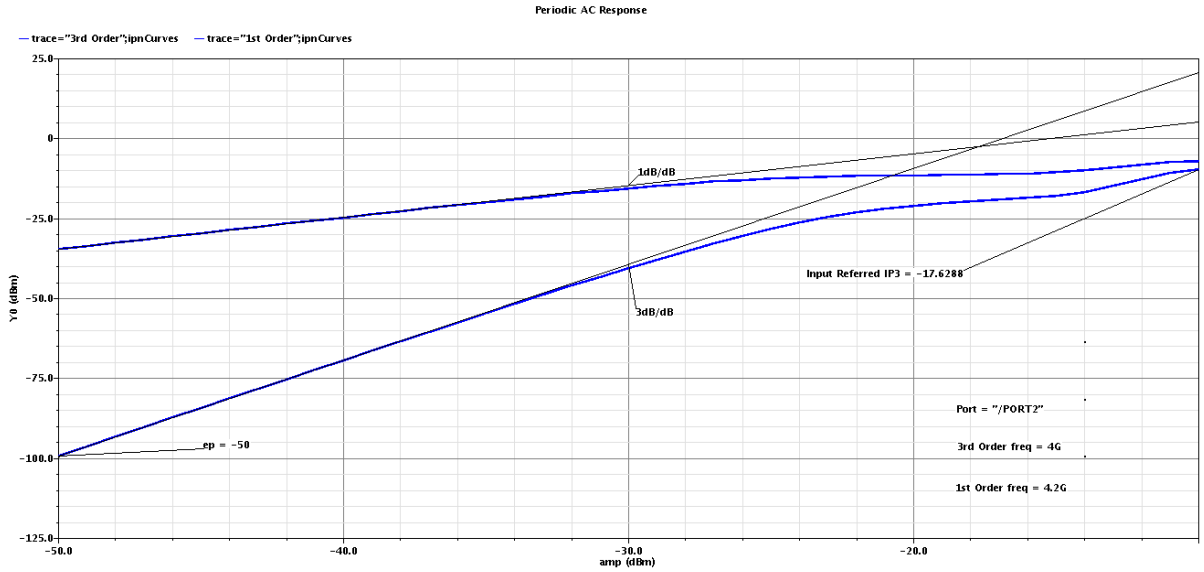

Figure 2.17: The input refered IP3 at 4 GHz

Table 2.5 is a summary of the achieved results

Parameter	Specifications	Achieved
Bandwidth	3.1 GHz to 5.3GHz	3.1 GHz to 5.3GHz
Input Reflection Coefficient (S_{11})	< -10 dB	-15 dB
Noise Figure (NF)	< 4dB	4 dB
Gain (S_{21})	14 dB to16 dB	15 dB
Reverse isolation (S_{12})	Lowest possible	< -51 dB
Power	Lowest possible	3.2 mW
IIP_3	> -15 dBm	-17 dB
FOM	-	5.1

Table 2.5: Achieved results using TSMC13RF design kit

It is noticeable that most of the targeted specifications are achieved except for the IIP_3 which is expected to be lower than the targeted value due to the low supply voltage 1.2V and the cascading of three transistors which limits the output swing and decrease the linearity.

As linearity is a secondary specification in the design of the LNA, this value is considered acceptable.

2.6 TSMC13RF DESIGN KIT PROCESS CORNERS SIMULATION RESULTS

2.6.1 Small signal process corners

Figure 2.18 the input reflection coefficient S_{11} process corners results.

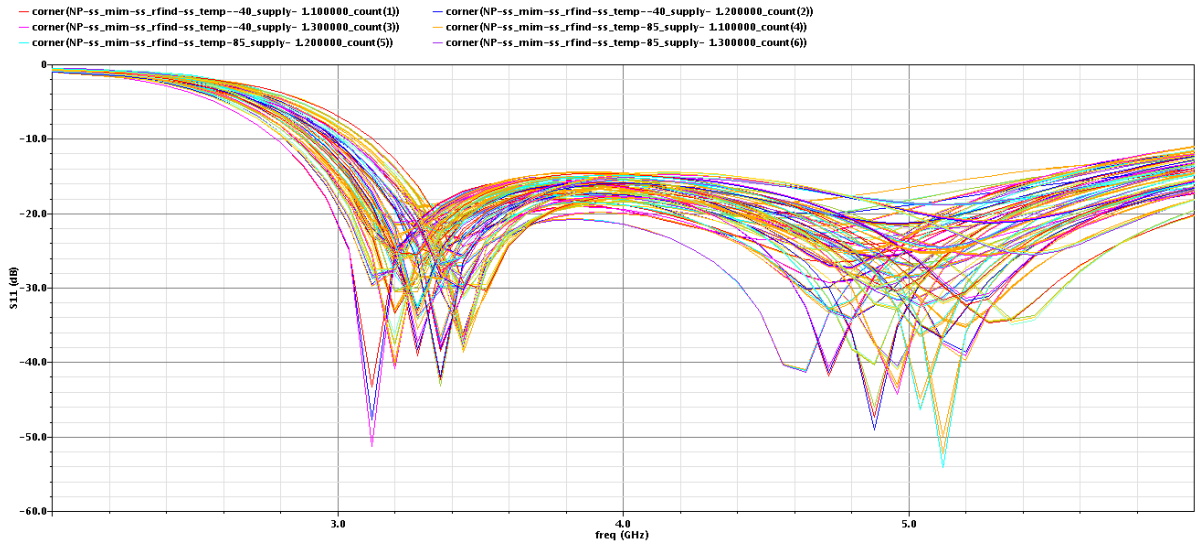

Figure 2.18: S_{11} process corners results

Figure 2.19 input reflection coefficient worst case corner: NMOS is slow, Cap. is fast, Ind. is fast, Temp is 85ºC and Vdd=1.3V. The maximum S_{11} was found to be -9.5 dB.

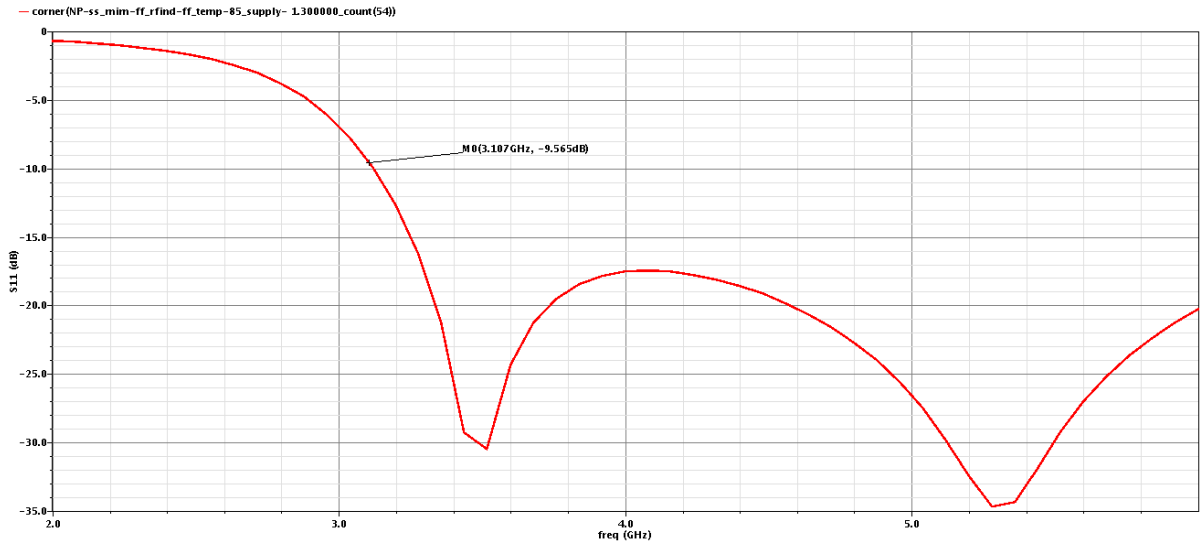

Figure 2.19: S_{11} worst case corner

Figure 2.20 the power gain S_{21} process corners results. The gain variation is from 10 dB to 21 dB.

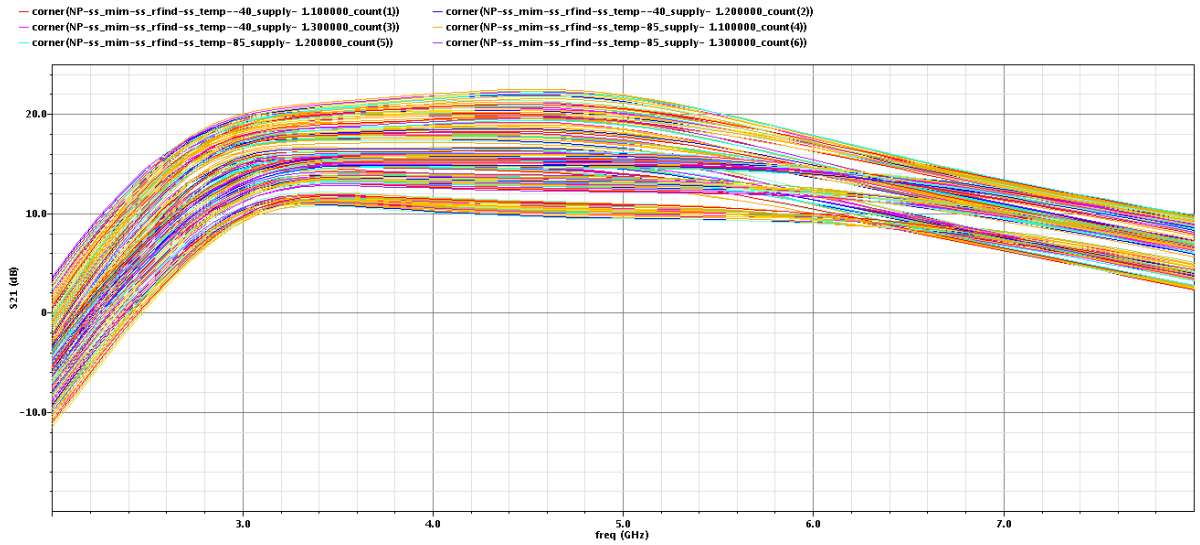

Figure 2.20: S_{21} process corners results

Figure 2.21 power gain worst two corners: NMOS is slow, Cap. is fast, Ind. is typical, Temp is 85ºC and Vdd=1.1V, the gain is reduced to 10 dB and NMOS is fast, Cap. is slow, Ind. is fast, Temp is -40ºC and Vdd=1.3V, the gain increased to 21 dB.

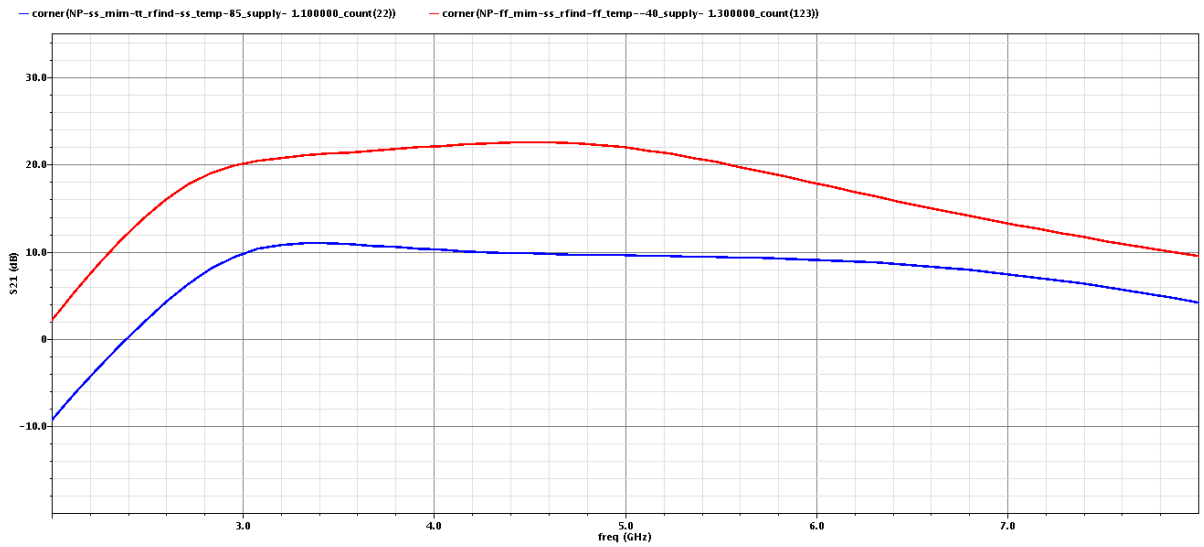

Figure 2.21: S_{21} worst case corners

Figure 2.22 noise figure process corners results. The maximum noise figure is 5.2 dB.

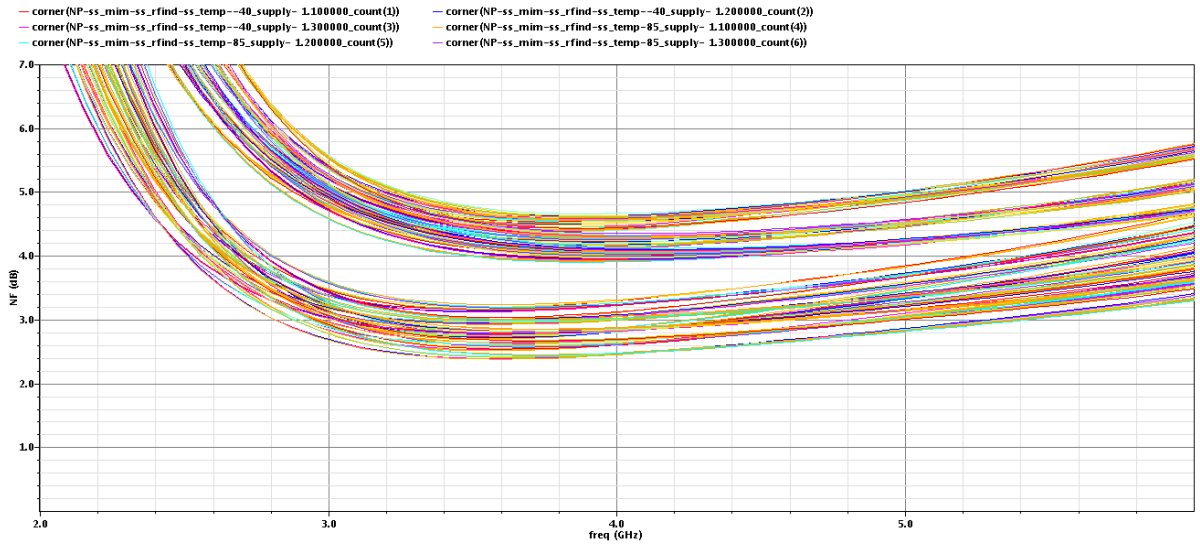

Figure 2.22: NF process corners results

Figure 2.23 noise figure worst case corner NMOS is slow, Cap. is fast, Ind. is fast, Temp is 85ºC and Vdd=1.1V the noise figure increased to 5.2 dB.

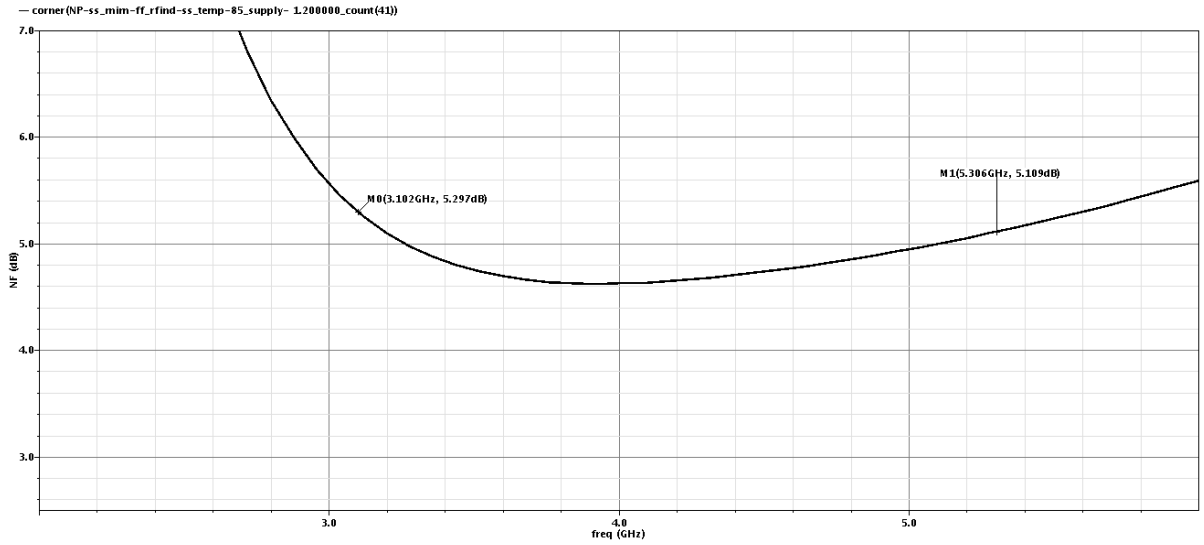

Figure 2.23: NF worst case corner

Figure 2.24 reverse isolation S_{12} process corners results. The maximum value is -47 dB.

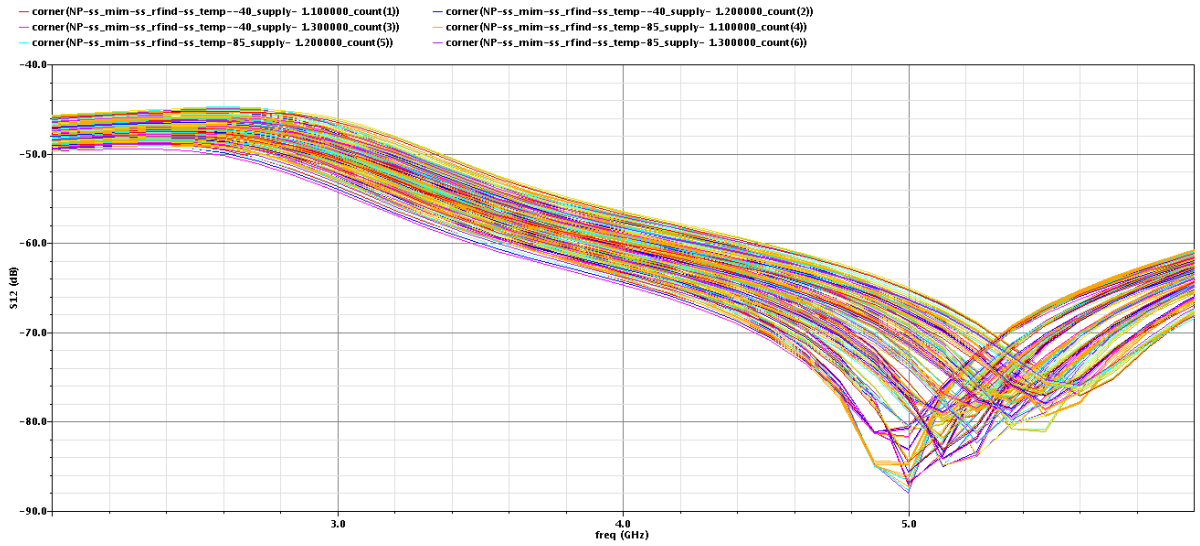

Figure 2.24: S_{12} Process corners results

Figure 2.25 reverse isolation worst case corner NMOS is slow, Cap. is fast, Ind. is fast, Temp is 85ºC and Vdd=1.1V.

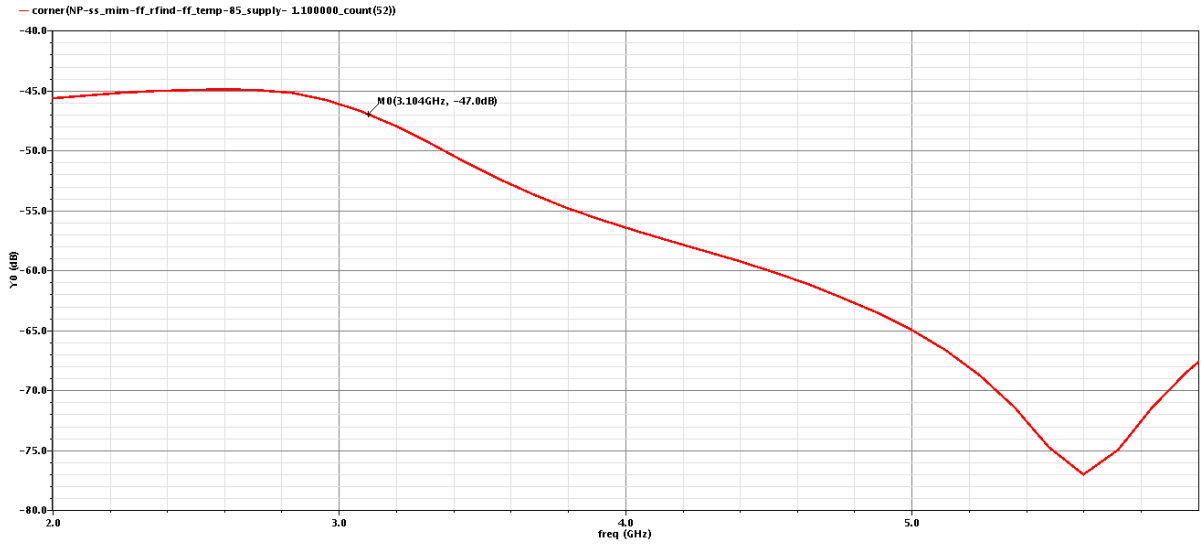

Figure 2.25: S_{12} worst case corner

Figure 2.26 stabilty factor K_f porocess corners results. K_f is greater than one across all corners.

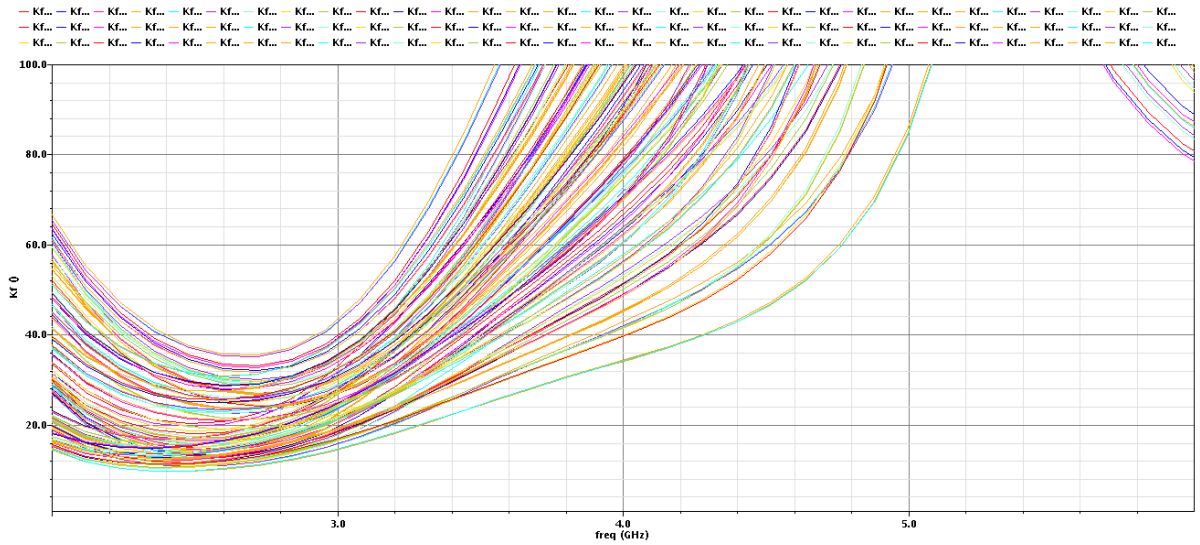

Figure 2.26: K_f process corners results

Figure 2.27 alternative stability factor B_{1f} process corners results. B_{1f} is greater than zero across all corners.

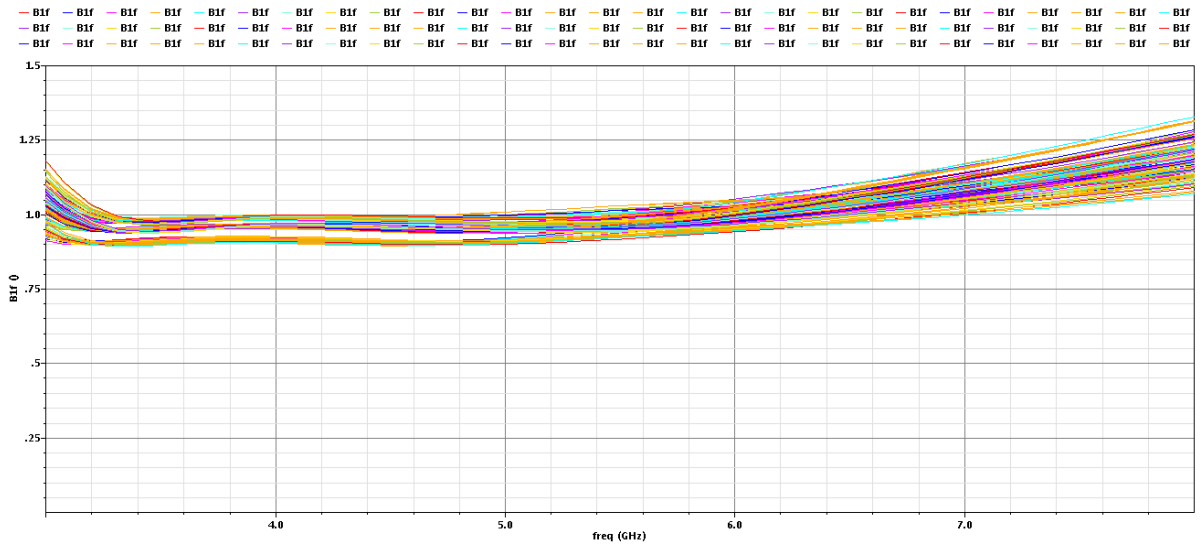

Figure 2.27: B_{1f} process corners results

Based on the above two figures the LNA is unconditionally stable across all corners.

2.6.2 Large signal process corners

Figure 2.28 is the worst case corner for the LNA linearity NMOS is fast, Cap. is slow, Ind. is fast, Temp is -40ºC and Vdd=1.3V, the P_{1dB} is decreased to -28 dBm.

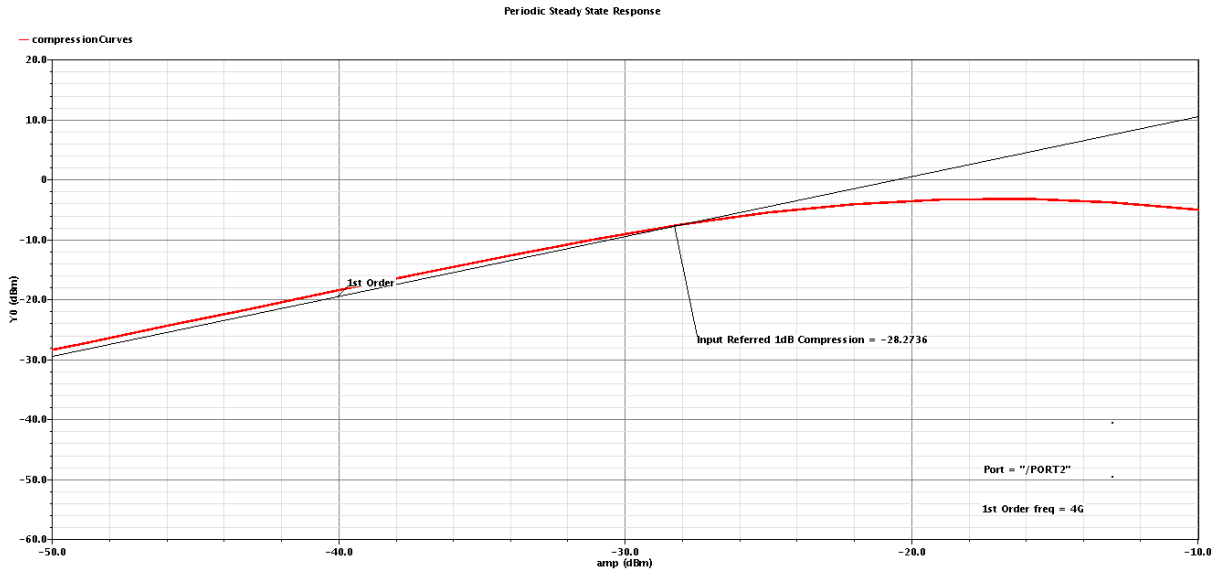

Figure 2.28: P_{1dB} worst case corner

Table 2.6 shows the achieved results from running process corners simulations.

Parameter	Achieved	Worst case corner
Bandwidth	3.1 GHz to 5.3GHz	3.1 GHz to 5.3GHz
Input Reflection Coefficient (S_{11})	-15 dB	-9.5 dB
Noise Figure (NF)	4 dB	5.2 dB
Gain (S_{21})	15 dB	Varies from 10 dB to 21 dB
Reverse isolation (S_{12})	< -51 dB	< -47
IIP_3	-17 dBm	-18 dBm

Table 2.6: Summary of the process corners performance of the LNA

The only problem appeared after running process corners simulations is the gain variation from 10 dB to 21 dB this problem can be solved by two ways either changing the LNA bias circuit to be a constant g_m circuit this will decrease the gain variation or adapt the VGA following the LNA for such large variation across corners.

2.7 LF15RF DESIGN KIT SIMULATION RESULTS

The transistors sizing and the components values of the above design kit is presented in Table 2.7.

Transistors width	M_1 = 194µ, M_2 and M_3 = 97µ, M_4 and M_5 = 48µ
Transistors length	150 nm for all transistors
Capacitors	C_1 = 700fF, C_2 = 3pF, C_g = 900fF, C_b = 3.5pF and C_B = 3pF
Inductors	L_1, L_g and L_2 = 2nH, L_s = 560pH, L_d = 5.2nH, L_{pk} = 2.2nH and L_3 =1.3nH
Supply voltage	1.8 V
Power dissipation	6.12 mW

Table 2.7: Transistors sizing and components values for LF15RF design kit

2.7.1 Small signal simulation

The small signal simulations are performed to evaluate the S-parameters, noise figure and stability parameters.

Figure 2.29 the input reflection coefficient S_{11} is less than -12 dB.

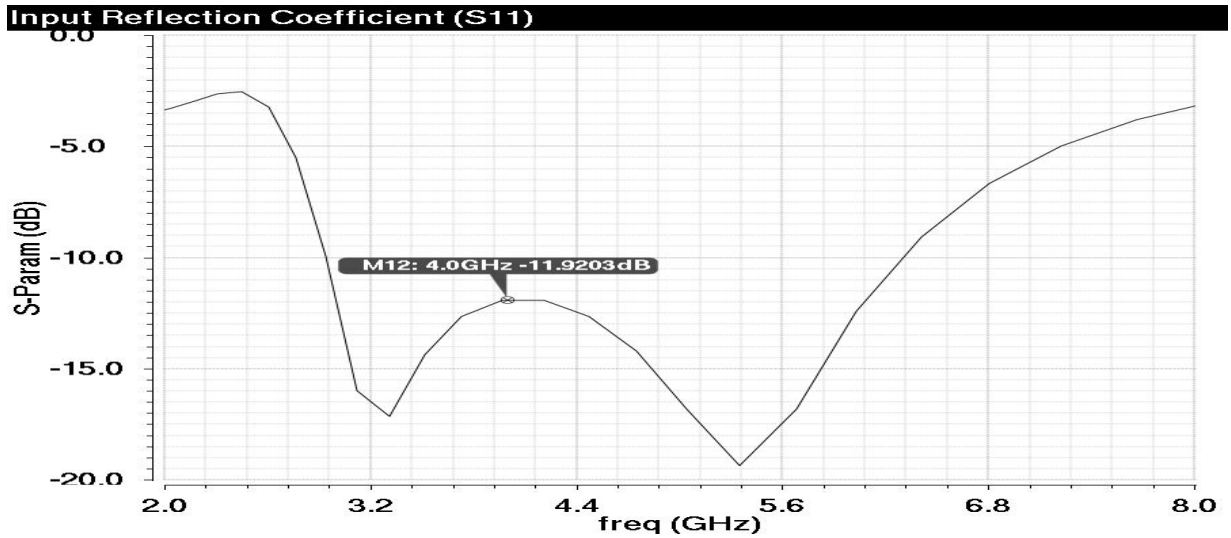

Figure 2.29: The input reflection coefficient S_{11}

Figure 2.30 the noise figure is of maximum value 3.5 dB at 5.3 GHz and minimum value 2.8 dB at 3.9 GHz.

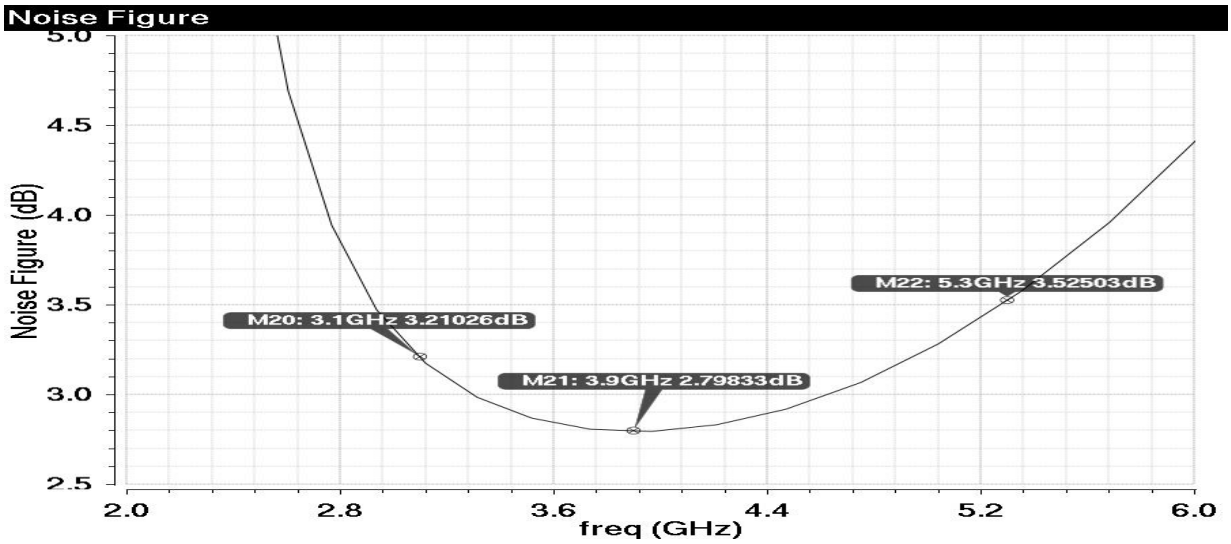

Figure 2.30: Noise Figure

The reason of this relatively low noise figure at 5.3 GHz is the high quality factor of the inductors L_1, L_g and L_2 which is equal to 16 at this frequency. The quality factor of the inductor is given by: $Q = \frac{\omega L}{R}$ and the high quality factor means less resistance and therefore low noise figure.

Figure 2.31 the power gain S_{21} of value 14.5 dB with variations less than 1 dB across the desired band width.

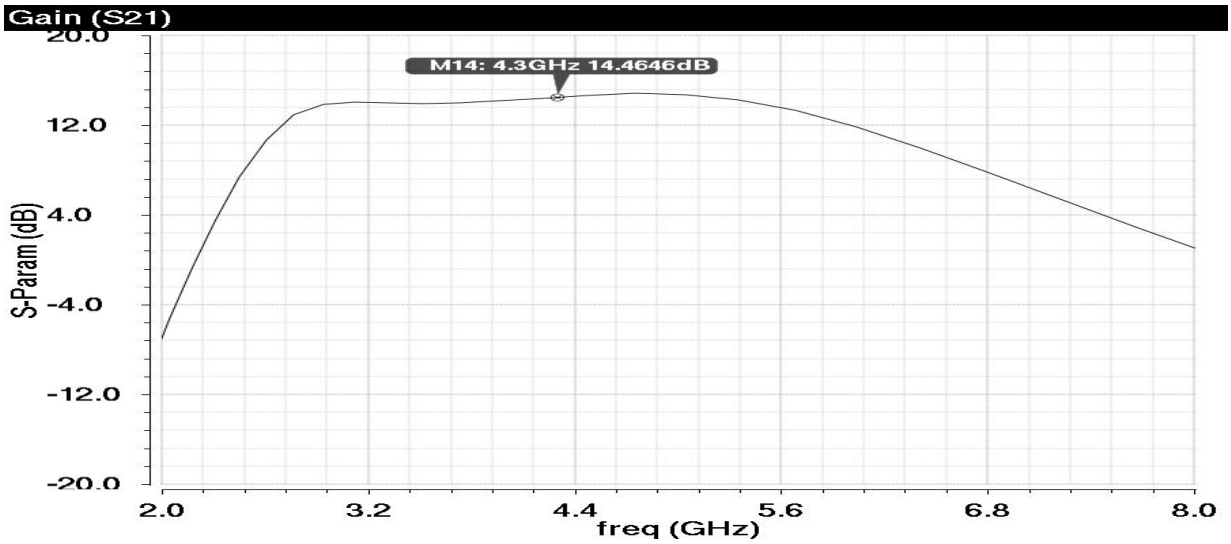

Figure 2.31: The power gain S_{21}

Figure 2.32 the reverse isolation is less than -82dB.

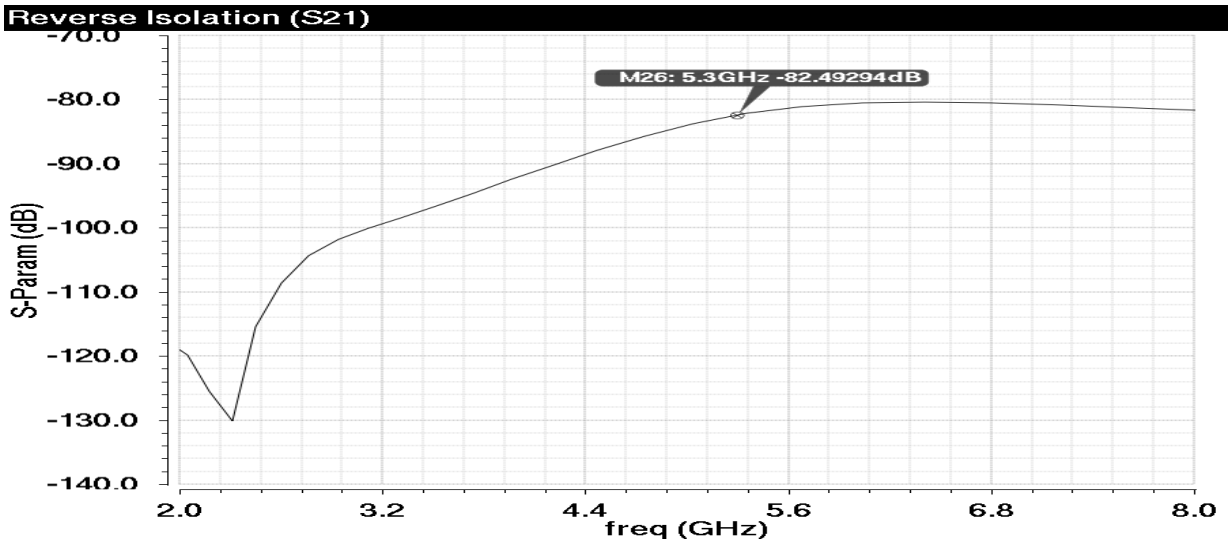

Figure 2.32: Reverse isolation S_{12}

Figure 2.33 the stability factor K_f is greater than one across all frequencies.

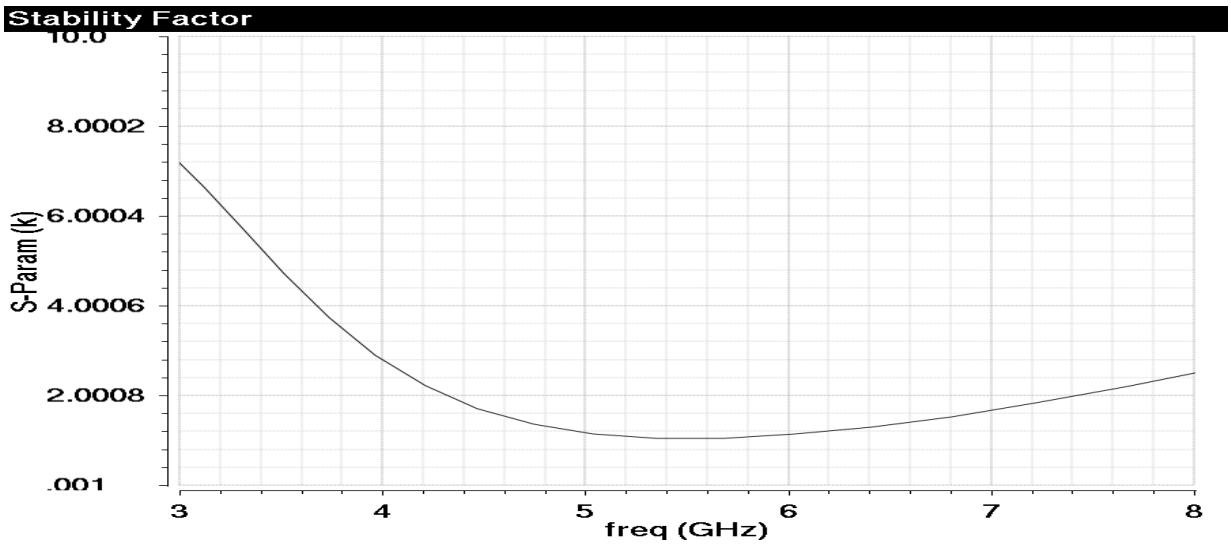

Figure 2.33: Stability factor K_f

Figure 2.34 the alternative stability factor B_{1f} is greater than zero across all frequencies therefore the LNA is unconditionally stable.

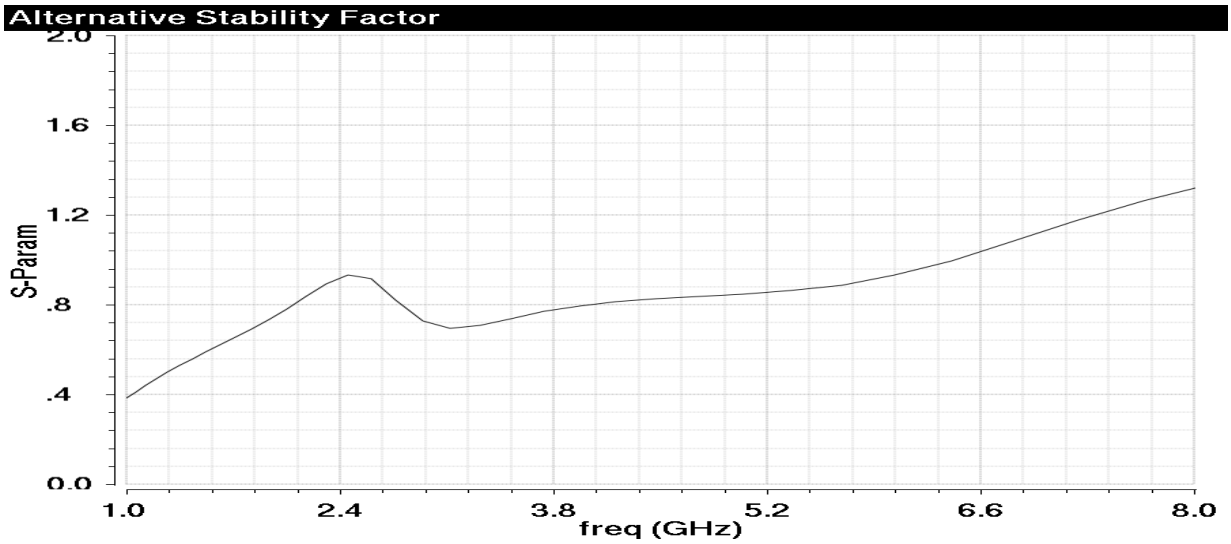

Figure 2.34: Alternative stability factor B_{1f}

2.7.2 Large signal simulation

Figure 2.35 large signal analysis is performed to find the1dB compression point P_{1dB} is equal to -21 dBm.

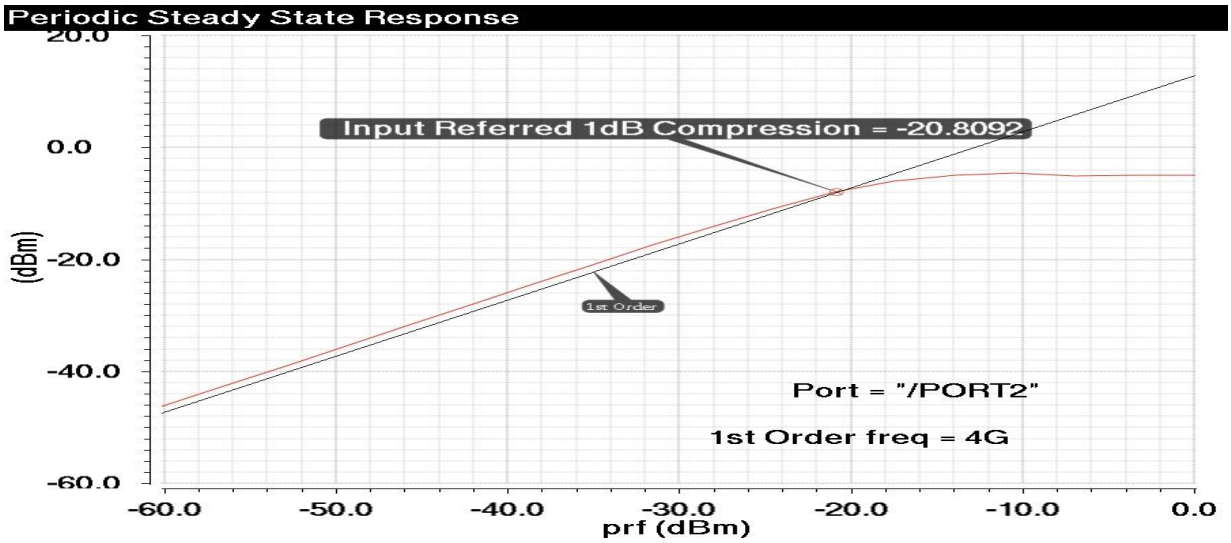

Figure 2.35: 1dB compression point

Figure 2.36 the IIP_3 is evaluated at 4 GHz with two blockers at frequencies 4.1 GHz and 4.2 GHz it is found to be -12 dBm.

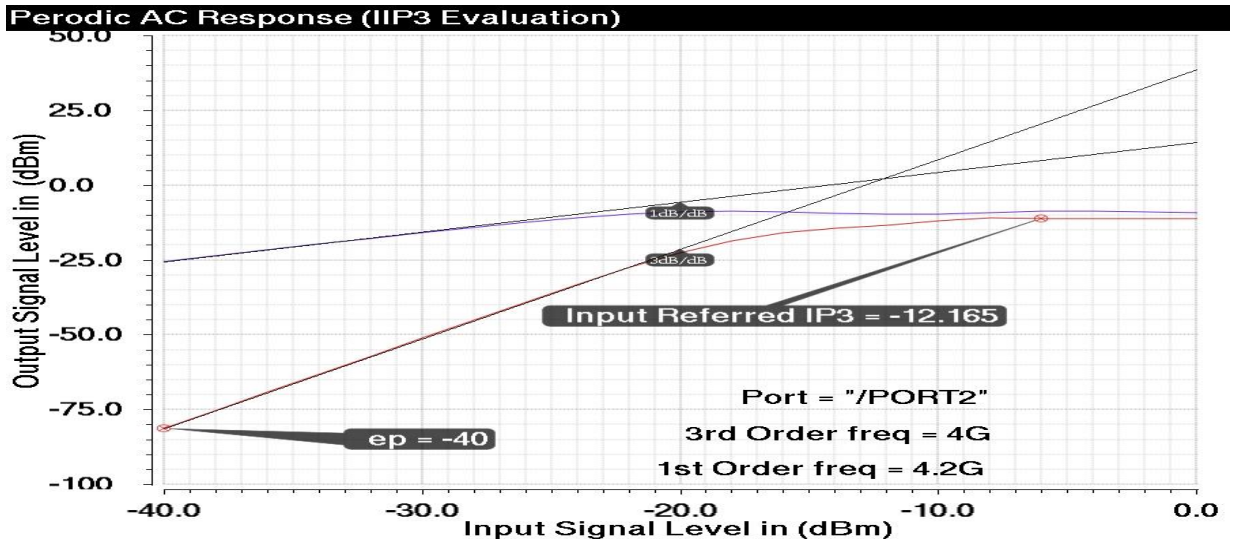

Figure 2.36: The input referred IP3 at 4 GHz

Table 2.8 is a summary of the achieved results

Parameter	Specifications	Achieved
Bandwidth	3.1 GHz to 5.3GHz	3.1 GHz to 5.3GHz
Input Reflection Coefficient (S_{11})	< -10 dB	-12 dB
Noise Figure (NF)	< 4dB	3.5 dB
Gain (S_{21})	14 dB to16 dB	14.5 dB
Reverse isolation (S_{12})	Lowest possible	< -82 dB
Power	Lowest possible	6.12 mW
IIP_3	> -15 dBm	-12 dB
FOM	-	2.51

Table 2.8: The achieved results using LF15RF design kit

All the targeted specifications are achieved and the problem of the high IIP_3 vanishes due to the presence of a high supply voltage 1.8V that does not limit the output swing but this comes in the expense of high power consumption which is approximately double the previous one and relatively low figure of merit.

2.8 LF15RF DESIGN KIT PROCESS CORNERS SIMULATION RESULTS

2.8.1 Small signal process corners

Figure 2.37 input reflection coefficient S_{11} process corners results.

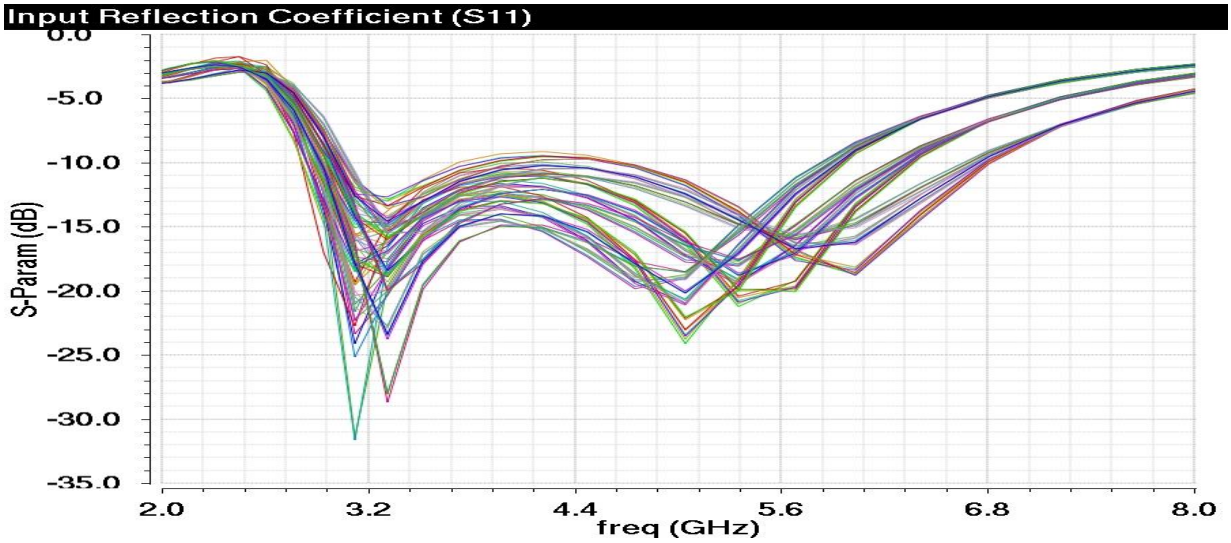

Figure 2.37: S_{11} process corners results

Figure 2.38 input reflection coefficient worst case corner: NMOS is slow, Cap. is max., Temp is -40ºC and Vdd=1.62V. The maximum S_{11} was found to be -9.2 dB.

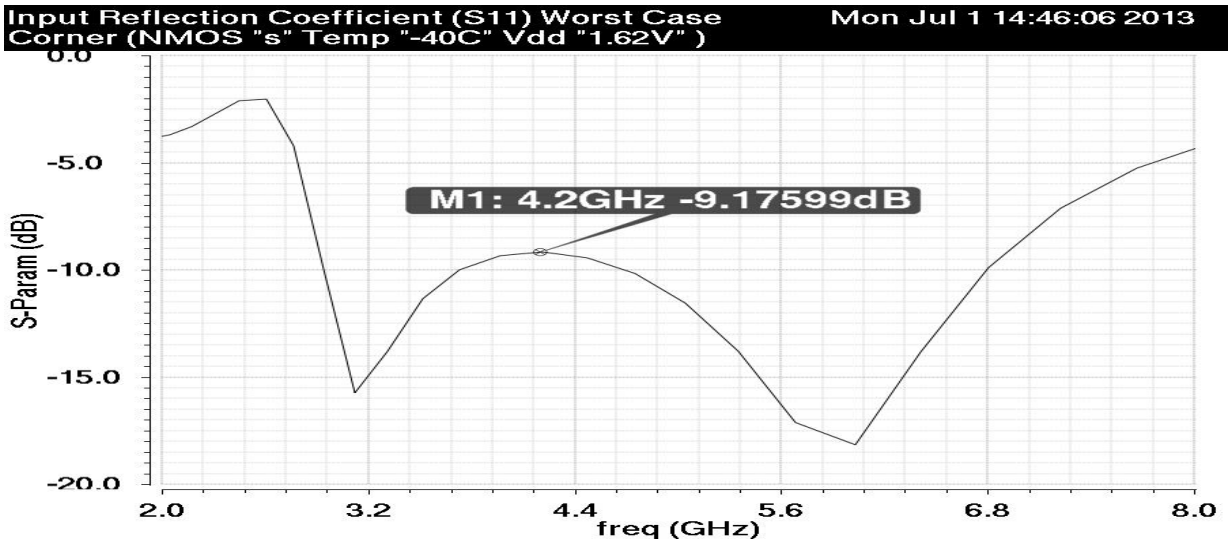

Figure 2.38: S_{11} worst case corner

Figure 2.39 the power gain S_{21} process corners results. The gain variation is from 7.6 dB to 19 dB.

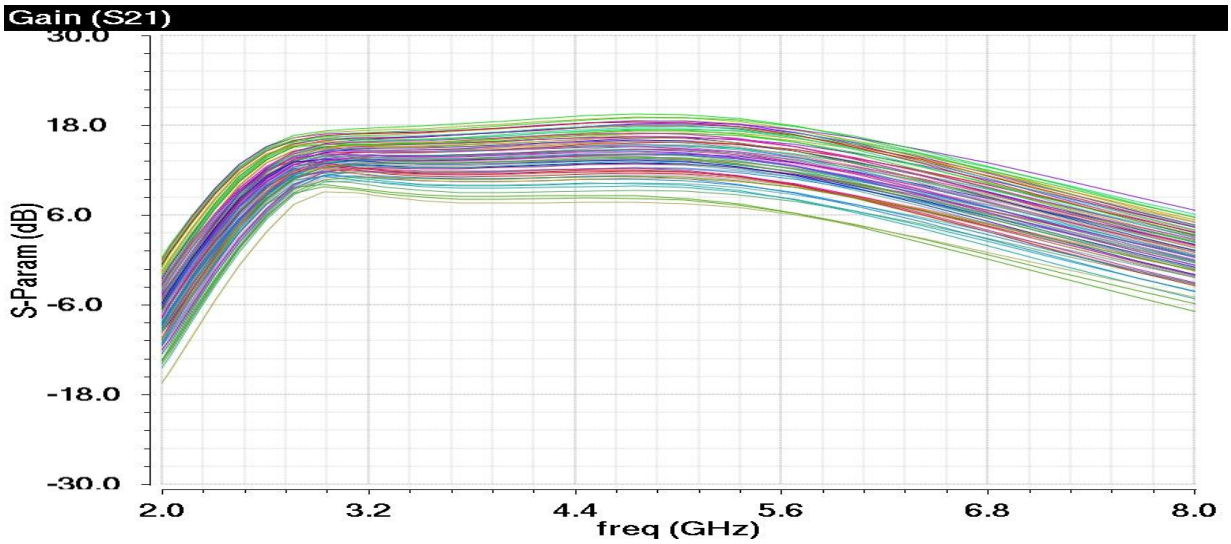

Figure 2.39: S_{21} process corners results

Figure 2.40 power gain worst two corners: NMOS is slow, Cap. is min., Temp is 85ºC and Vdd=1.62V, the gain is reduced to 7.6 dB and NMOS is fast, Cap. is max., Temp is -40ºC and Vdd=1.98V, the gain increased to 19 dB.

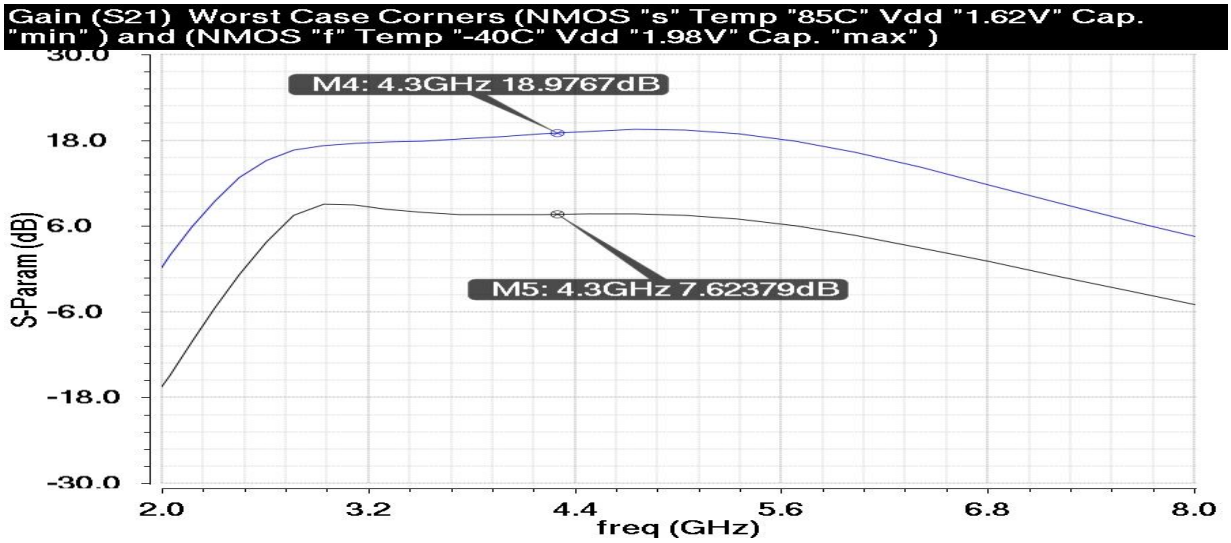

Figure 2.40: S_{21} worst case corners

Figure 2.41 noise figure process corners results. The maximum noise figure is 5.4 dB.

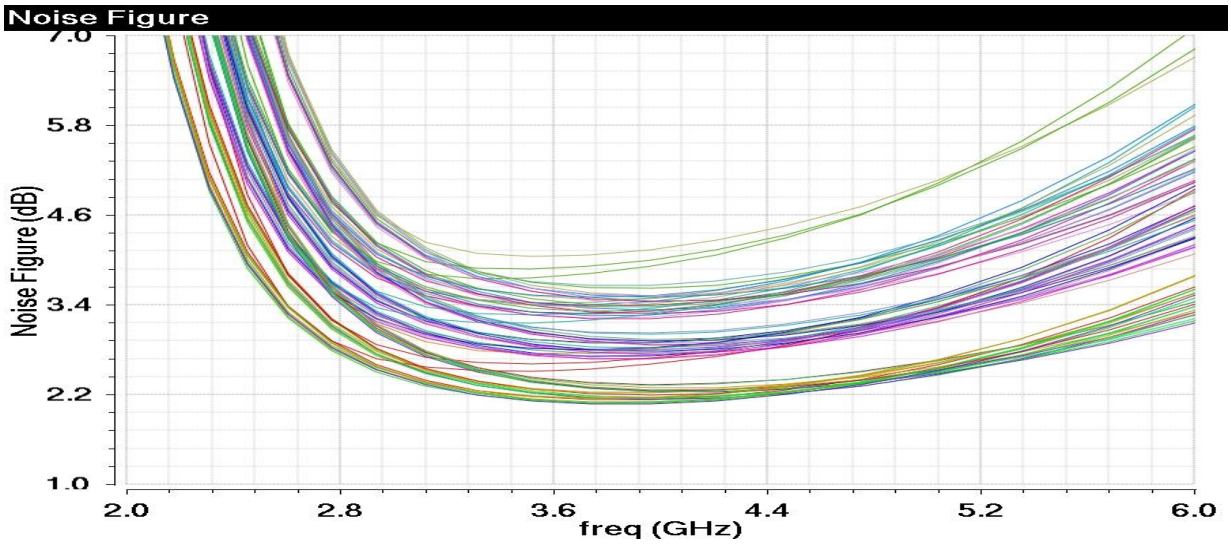

Figure 2.41: NF process corners results

Figure 2.42 noise figure worst case corner NMOS is slow, Cap. is min, Temp is 85ºC and Vdd=1.62V the noise figure increased to 5.4 dB.

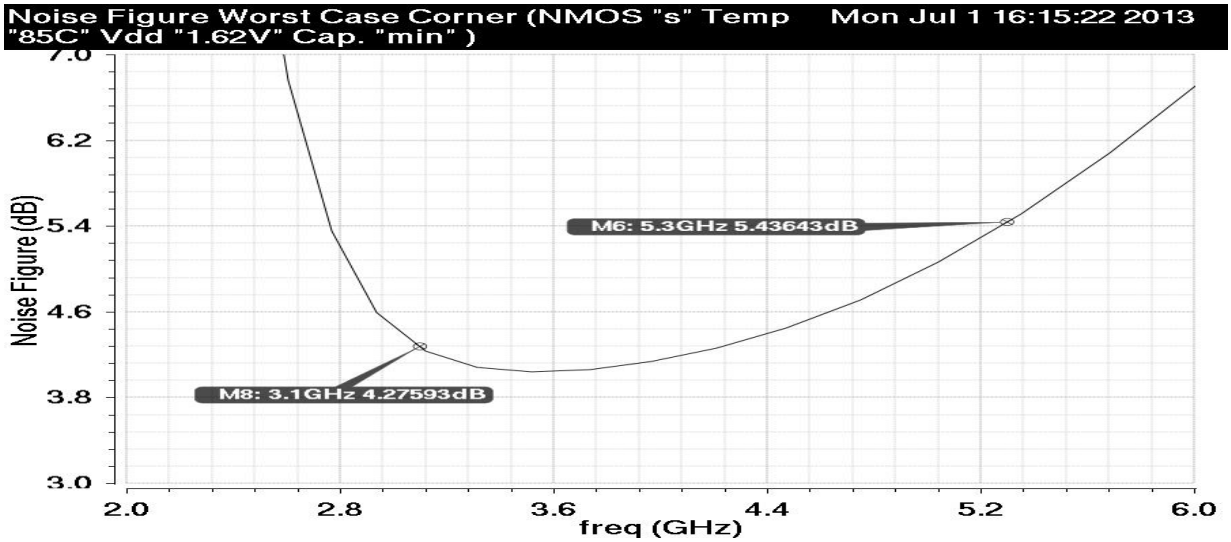

Figure 2.42: NF worst case corner

Figure 2.43 reverse isolation S_{12} process corners results. The maximum value is -79 dB.

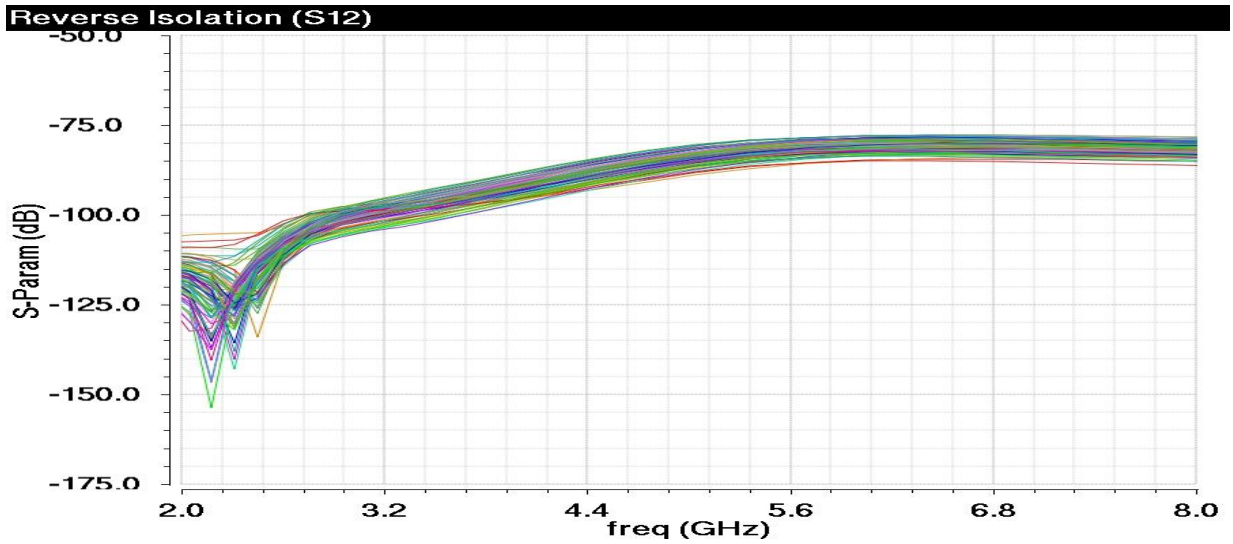

Figure 2.43: S_{12} process corners results

Figure 2.44 reverse isolation worst case corner NMOS is fast, Cap. is max,Temp is 85ºC and Vdd=1.62V.

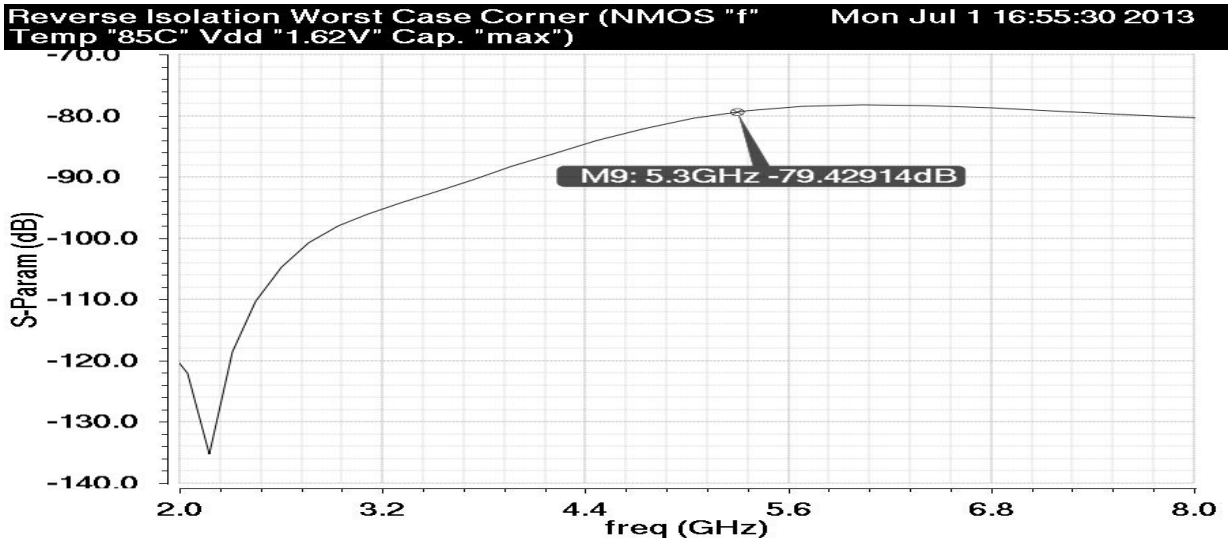

Figure 2.44: S_{12} worst case corner

Figure 2.45 stabilty factor K_f porocess corners results. K_f is greater than one across all corners.

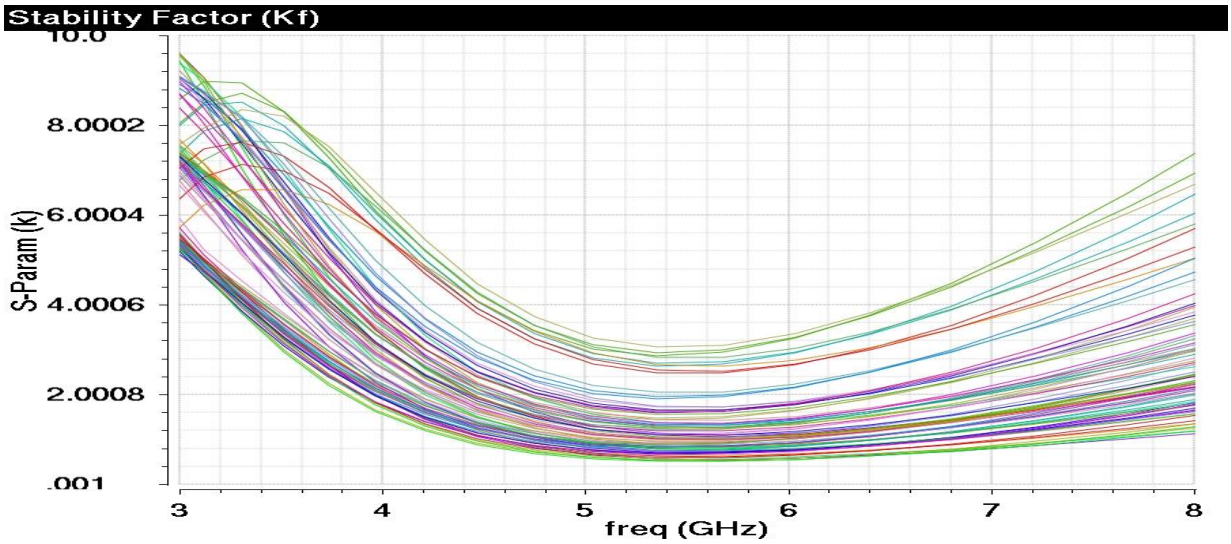

Figure 2.45: K_f process corners results

alternative stability factor B_{1f} process corners results. B_{1f} is greater than zero across all corners.

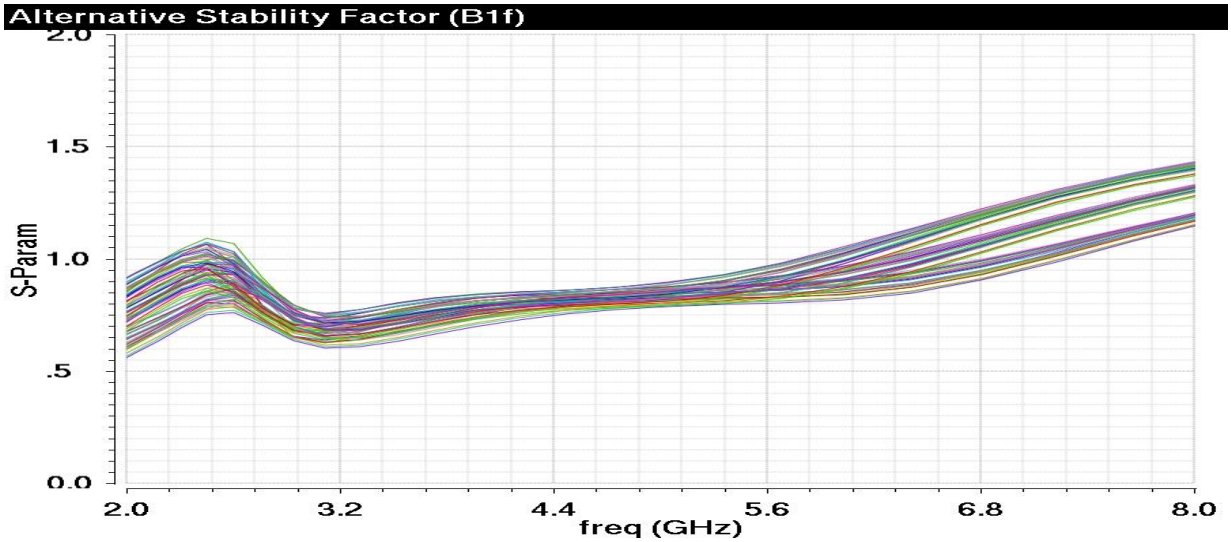

Figure 2.46: B_{1f} process corners results

Based on the above two figures the LNA is unconditionally stable across all corners.

2.8.2 Large signal process corners

Figure 2.47 is the worst case corner for the LNA linearity NMOS is fast, Cap. is min., Temp is -40ºC and Vdd=1.98V, the $IIP_3$is decreased to –15.7 dBm.

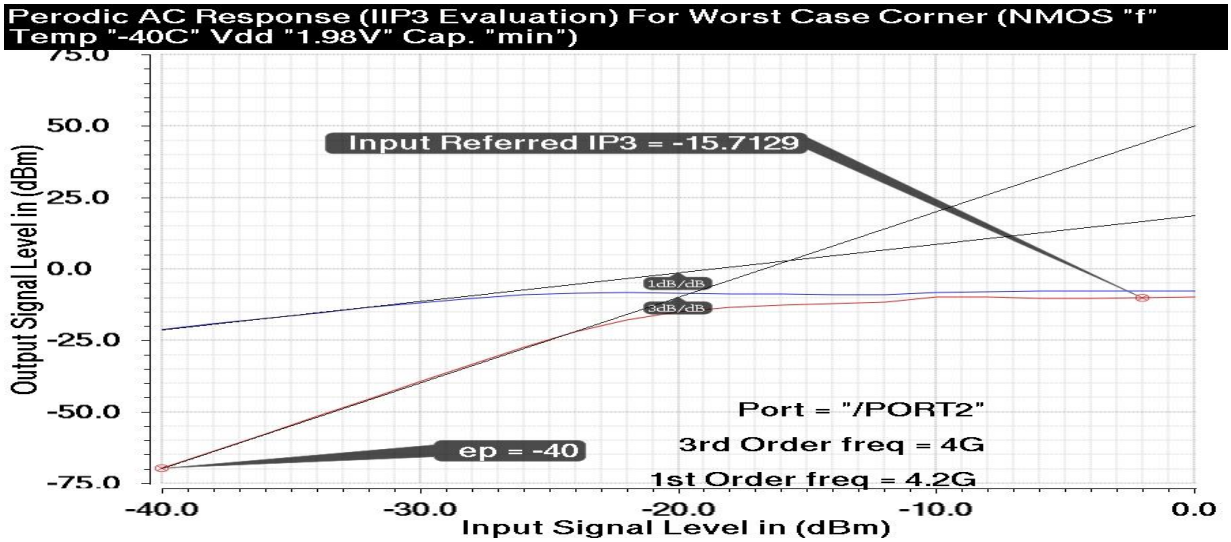

Figure 2.47: IIP_3 worst case corner

Table 2.9 shows the achieved results from running process corners simulations.

Parameter	Achieved	Worst case corner
Bandwidth	3.1 GHz to 5.3GHz	3.1 GHz to 5.3GHz
Input Reflection Coefficient (S_{11})	-12 dB	-9.2 dB
Noise Figure (NF)	3.5 dB	5.4 dB
Gain (S_{21})	14.5 dB	Varies from 7.6 dB to 19 dB
Reverse isolation (S_{12})	< -82 dB	< -79
IIP_3	-12 dBm	-15.7 dBm

Table 2.9: Summary of the process corners performance of the LNA

The same problem of the large gain variation is repeated as in the previous design and can be solved by the save methods proposed.

2.9 CIRCUIT LAYOUT

Figure 2.48 shows the circuit layout. This layout passes the design rule check.

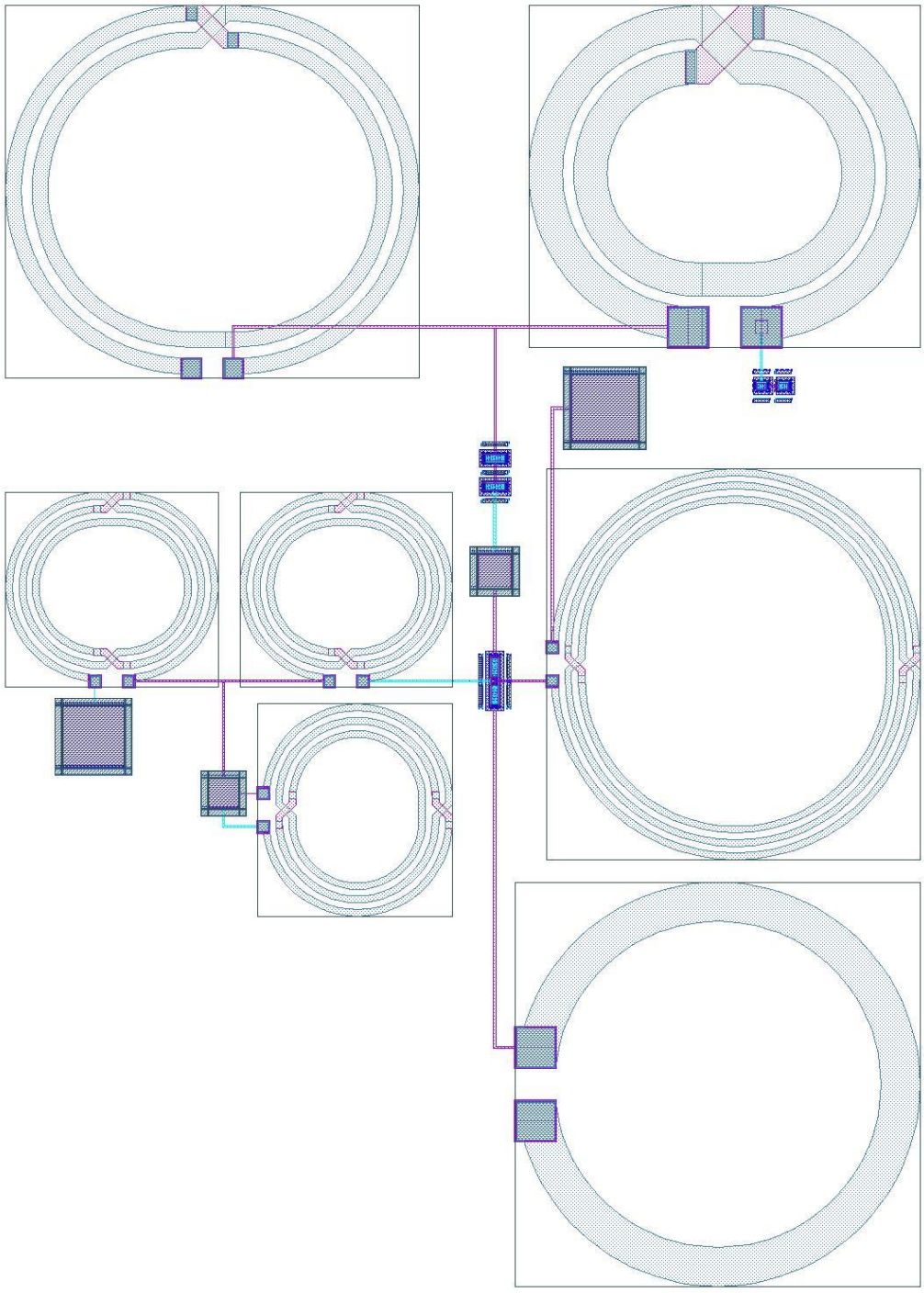

Figure 2.48: Circuit layout

2.10 CONCLUSION

An UWB-LNA is designed and optimized using TSMC13RF design kit to fullfil1 the system specifications. A brief discussion of the main LNA topologies is presented and the advantage and disadvantage of each topology is listed The LNA is designed using the current-reuse technique due the advantages of this technique that are mentioned earlier. Also, the design targets, tradeoffs and drawbacks are presented and a solution to the problems that appears is proposed.

Simulation of the different process corners is performed and the effect of each parameter in the process variation is discussed. Worst case corners are presented and they are found to have no effect on the system specifications. Also, solutions to the gain variation problem are presented.

After the optimized design is finished this design is migrated to a new technology and a new design kit which is LF15RF for fabrication purposes. Table 2.10 summarize the main positive and negative points of the two design kits.

Point of comparison	TSMC13RF	LF15RF
Power consumption	Low due to low supply voltage 1.2V	High due to high supply voltage 1.8V
Linearity	Less linearity	High linearity
Noise Figure	Higher due to the low quality factor of the inductors at high frequency	Low due to the high quality factor of the inductors at high frequency

Table 2.10: The main positive and negative points of the two design kits

Finally the circuit layout is presented and this layout passes the design rule check and waiting to pass the layout versus schematic to run the parasitic extraction then to be ready for the tape out.

Chapter 3 - SQUARER

3.1 - SQUARER TOPOLOGY

To perform the squaring function on the signal, a mixer is required. The usage of a conventional mixer such as a Gilbert cell as shown in (17) is not effective in this case as the Gilbert cell requires a large local oscillator (LO) signal in order to function correctly. The input of a small RF signal on the LO port of the Gilbert cell will not cause the required switching action in order for the cell to cause the mixing action. The proposed receiver architecture evades using a local oscillator to reduce the power consumption by omitting the need for a PLL**.**

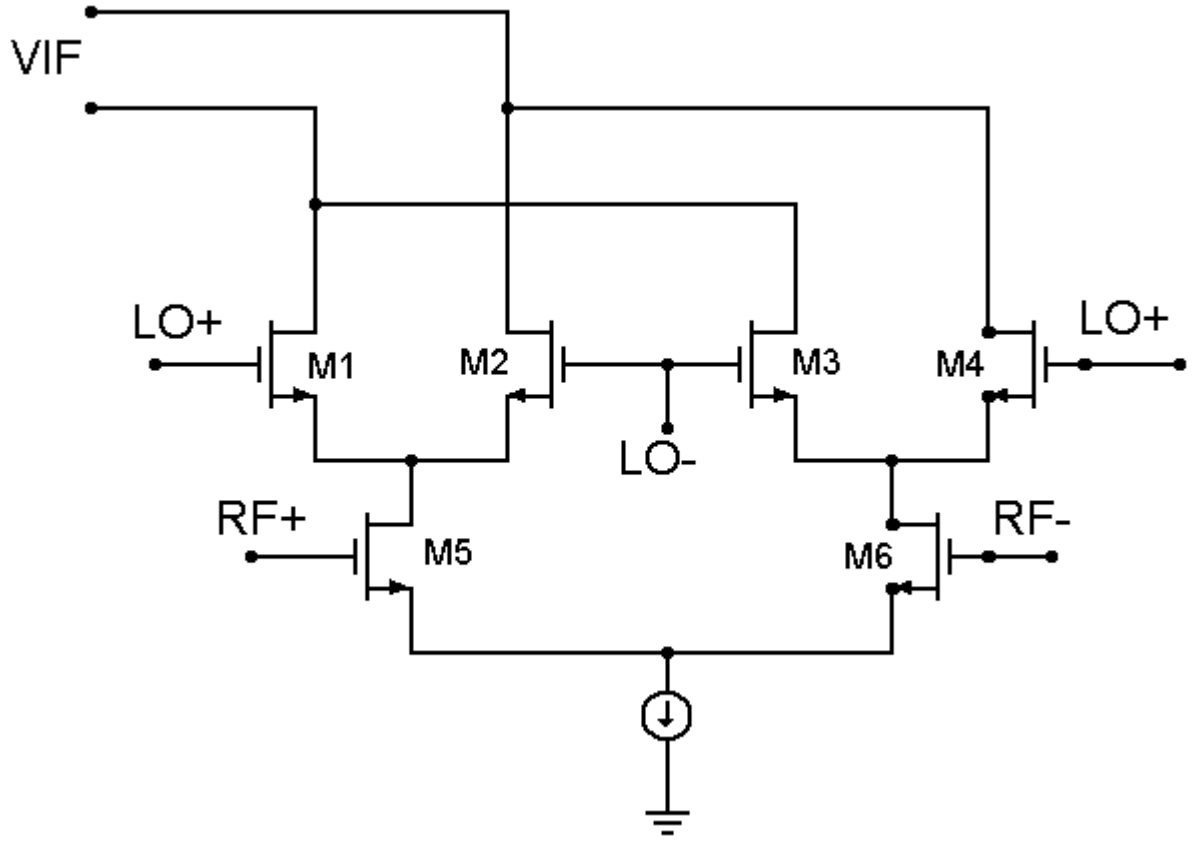

Figure 3.1: A conventional Gilbert cell

The used squarer topology, proposed in (17) and shown in Figure 3.2 enables performing the squaring action without the need for an LO. The transistors M1-4 are identical in size. Transistors M1-2 perform the squaring action while transistors M3-4 are used for DC offset cancellation only and are connected to an AC ground through a coupling capacitor. The operation of the squarer depends on the square law of the MOSFET.

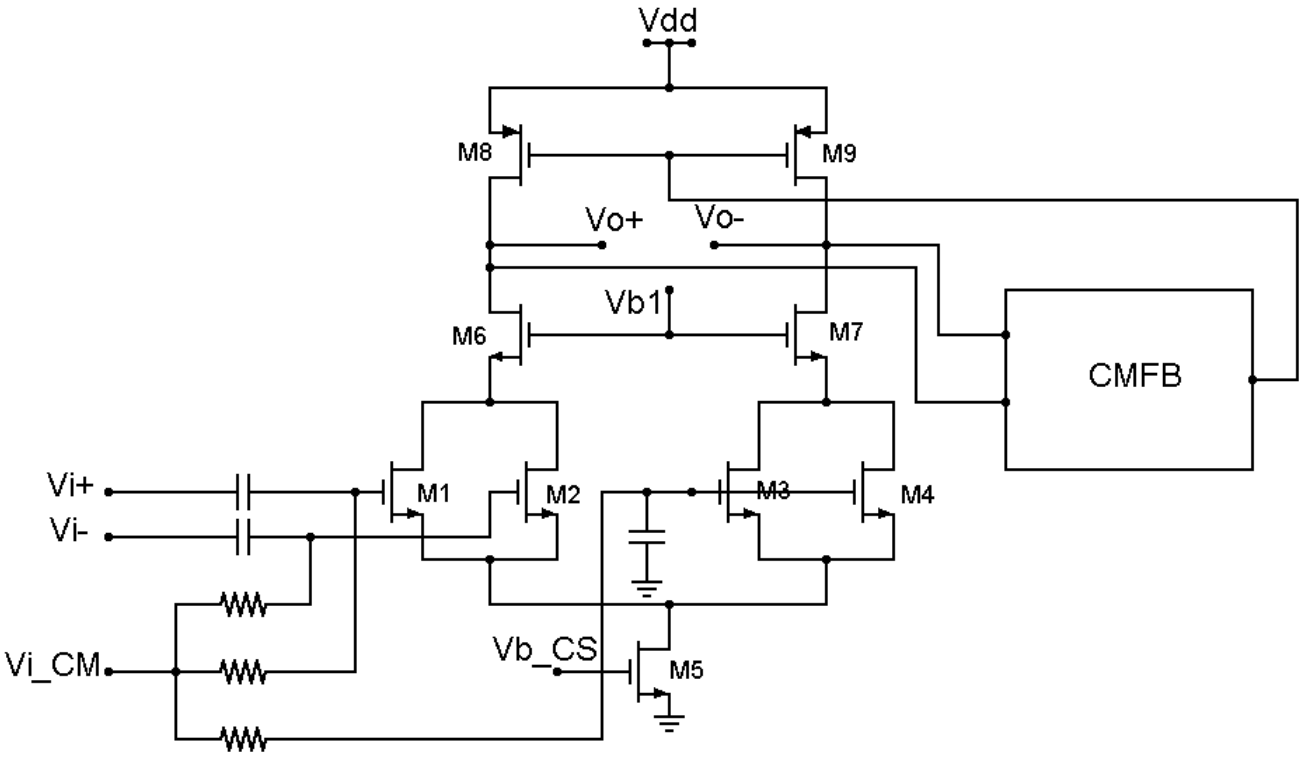

Figure 3.2: Schematic diagram of the squarer

The currents I_1through I_4 in M1 through M4 respectively are given by:

$$\boldsymbol{I_1 = \frac{1}{2}\beta\left(\frac{W}{L}\right)\left(V_B + \frac{v_{in}}{2} - V_{th}\right)^2} \qquad \textbf{(3.1)}$$

$$\boldsymbol{I_2 = \frac{1}{2}\beta\left(\frac{W}{L}\right)\left(V_B - \frac{v_{in}}{2} - V_{th}\right)^2} \qquad \textbf{(3.2)}$$

$$\boldsymbol{I_3 = I_4 = \frac{1}{2}\beta\left(\frac{W}{L}\right)(V_B - V_{th})^2} \qquad \textbf{(3.3)}$$

where β is the transistor constant, $\frac{W}{L}$ is the size ratio, $V_B$is the bias voltage and $V_{th}$is the threshold voltage of the transistor. The squarer output voltage is given by:

$$\boldsymbol{V_{out} = I_{out}.R_{out} = (I_1 + I_2 - I_3 - I_4).R_{out}} \qquad \textbf{(3.4)}$$

After simplification, the output is given by

$$\boldsymbol{V_{out} = \frac{\beta}{4}\frac{W}{L}v_{in}^2 R_{out}} \quad \textbf{(3.5)}$$

where R_{out} is the output resistance of the circuit. The output current passes through the cascade devices M6-M7 that increase the output resistance of the circuit. An active load of a PMOS is used to provide a high output resistance without taking up much headroom. At low frequencies, the output impedance $R_{out}$is limited by the squarer output resistance since the output is connected to the high resistance of the next stage gate and is given by:

$$\boldsymbol{R_{out} \cong r_{o,M8} || \left[\left(1 + \frac{g_{m,M6}.r_{o,M1}}{2}\right) r_{o.M6}\right]} \qquad \textbf{(3.6)}$$

where $r_o$is the transistor output resistance and $g_m$is the transistor transconductance.

Since the conversion gain of this topology is independent of gm and only depends on $\beta\frac{W}{L}$, the transistors M1-M4 are desired to have a very large $\frac{W}{L}$ ratio and hence they operate in subthreshold region.

3.2 CURRENT MIRRORS

The circuit is biased by a current biasing using a tail current source which comes from a simple current mirror circuit that mirrors current at the desired mirroring ratio. Transistors M1-M2 are connected to the input RF signal through AC coupling capacitors to separate the common mode of the squarer from that of the preceding stage. The input common mode voltage Vi_CM comes from a suitable current mirror and is fed to the input gates through large resistors that are large enough to perform correctly without adding much noise. The cascade transistors M6-M7 are also biased by means of a suitable current mirror. The used current mirrors are shown in Figure 3.3.

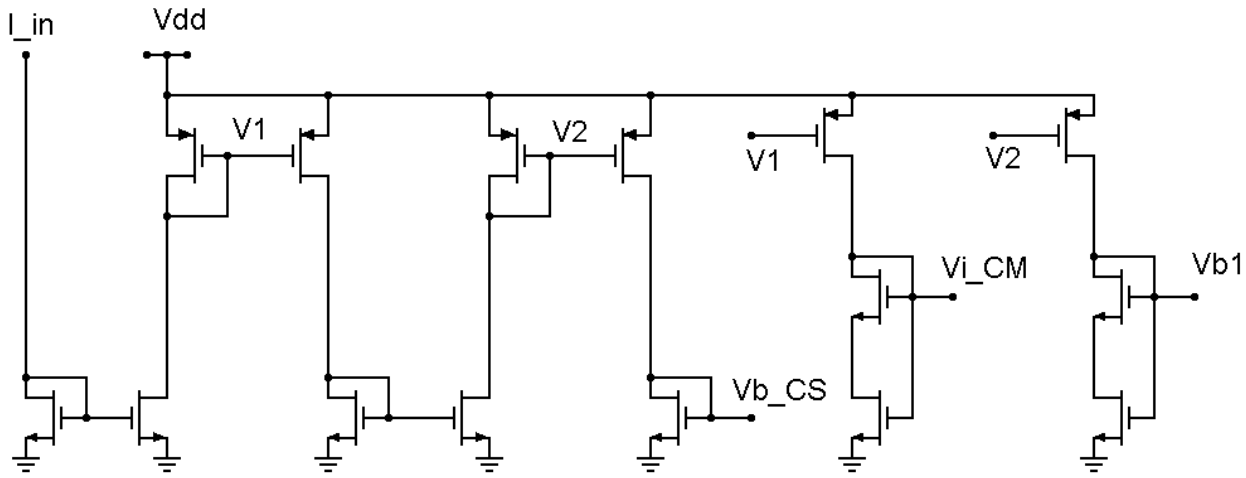

Figure 3.3: Schematic diagram of the current mirrors

Since the tail source current is relatively large, many stages of mirrors are used to provide it as shown in figure to prevent large mirroring ratios for better matching as a mirroring ratio higher than 10 is not recommended. The current mirrors used to generate Vi_CM and Vb1 are of cascade type for getting better performance across corners as they are connected to transistors that are connected to other MOSFETS at their source and not to the ground.

3.3 COMMON MODE FEEDBACK

Since the output is connected to the drains of a cascade device and a PMOS load, the output node is a high impedance node. To set the common mode voltage of this output high impedance node, a common mode feedback (CMFB) circuit is used. The common mode feedback circuit senses the output common mode voltage and sets the gate voltage of MOSFETS M8 and M9 to the value that makes the common mode voltage equal to the desired reference value.

The common mode feedback topology used is shown in Figure 3.4. It consists of an OTA with diode connected load. Transistors M1 and M2 act as a common mode feedback sense that senses the output common mode voltage of the squarer without loading on the squarer and they act as if they are one transistor. The reference voltage is input to the gate of M3 which is sized to have twice the size of M1 and M2.

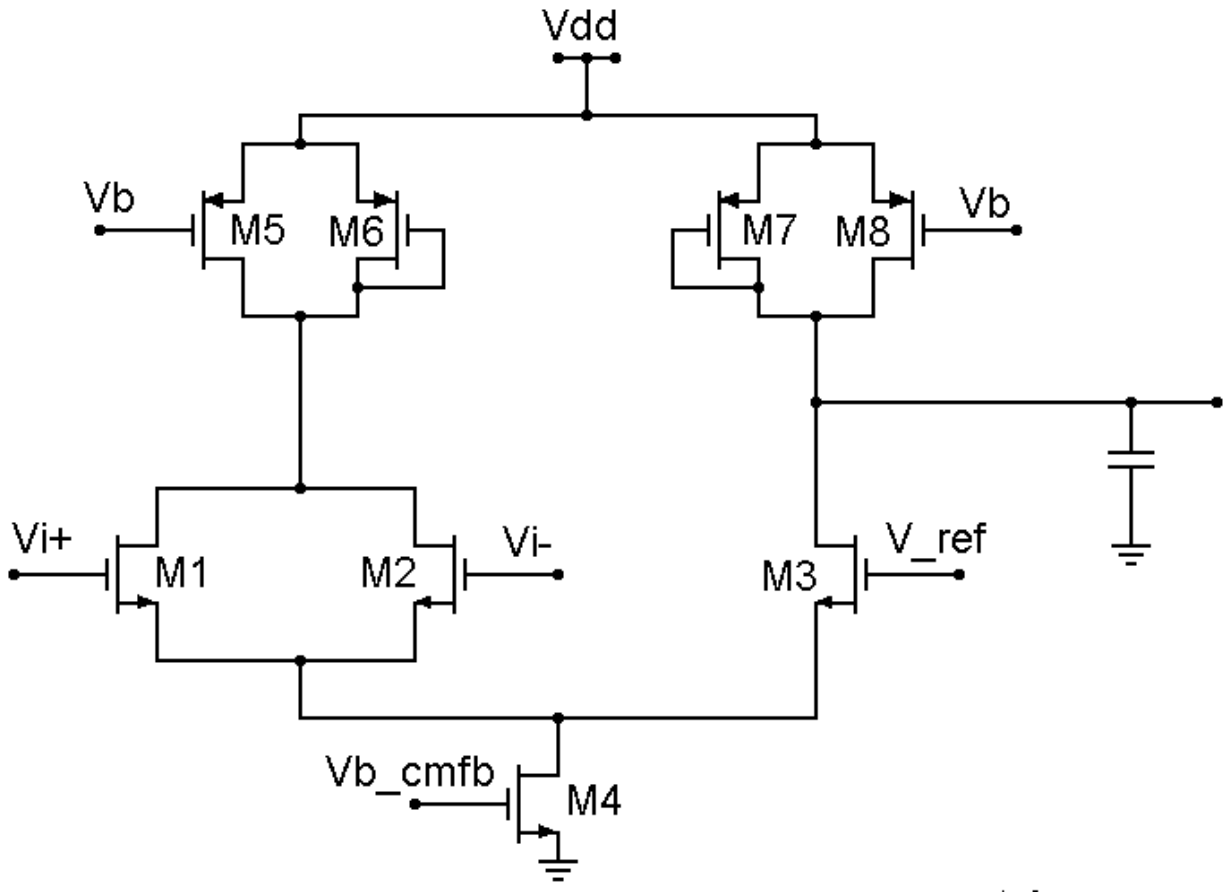

Figure 3.4: Schematic diagram of the CMFB circuit

The gain of this structure is approximately given by: $\frac{1}{2}.\frac{gm_3}{g_{m7}}$. A sufficiently large gain is required to decrease the error between the common mode output of the squarer and the reference voltage but not too large so that not to affect the stability of the common mode feedback loop. To get sufficient gain, gm_3 must be much larger than gm_7. Since both M3 and M7 have the same drain current, this requires M7 to have a very large overdrive voltage which causes the output DC voltage of the CMFB circuit to be low. To solve this issue, a current starving transistor M8 is used which acts as a current source that takes most of the current of M3 and starves the current of M7. This enables reducing the gm of M7 with a reasonable output DC voltage. The bias voltage Vb is designed to be the same as V1 in the current mirror circuit in Figure 3.3 which eliminates the need for another current mirror to bias M8.

An important issue to that must be noted in CMFB circuit is that the polarity of the inputs and outputs should be chosen such that to guarantee a negative feedback in the common mode feedback loop or else the common mode feedback loop will oscillate.

The reference voltage is generated using a resistive divider circuit as shown in Figure 3.5. Since the reference voltage is input to the gate of a MOSFET which shows high impedance, the CMFB circuit will draw negligible current from the resistive divider and hence it will not affect its operation. The values of the resistances should be large enough to prevent drawing large current from the supply and increasing wasting power consumption.

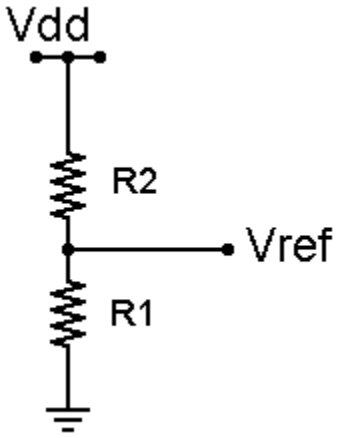

Figure 3.5: Schematic diagram of a resistive divider circuit

3.4 SIMULATION RESULTS

The squarer topology above was implemented on LF150, the 150nm technology from LFoundry with 6 metal layers. The supply voltage in this technology is 1.8 volt. The technology has special RF MOSFETS with only three options for the width and minimum length. The transistor models are BSIM 3v3 models. The design is simulated using Cadence Virtuoso custom IC design suite version 6.

The total current consumption of the squarer including the current mirrors and the common mode feedback circuit is 2.594 mA, corresponding to a power consumption of 4.67mW. Since the gain is independent of gm and the input transistor of the squarer is biased in subthreshold region, this power consumption could have been greatly reduced without affecting the conversion gain so much; But this resulted in a very bad noise performance so the current was mainly increased to reduce the noise of the squarer and achieve the desired noise figure.

3.4.1 Conversion gain

To simulate a conventional mixer circuit and get the simulated conversion gain, noise figure and IIP3, a periodic steady state analysis (PSS) is usually used. The PSS analysis solves the circuit with the large LO signal to get a periodic operating point for the circuit. The simulator then linearizes the mixer circuit around this periodic operation point which is periodic with the LO frequency. After linearizing the circuit, a PAC and a PNOISE analysis are made to get the AC gain and noise and hence the conversion gain and noise figure.

The usage of this this method for simulating an ultra-wideband squarer is impossible as the squarer circuit is used to mix a wide "band" with itself (another wide "band"). The PSS and QPSS analysis linearizes the circuit about a single frequency or about a finite number of single tones. Since the input to the squarer is rather a "band" and not a single tone, the usage of PSS or QPSS will not take the effect of mixing of each frequency of the band with all other frequencies and will give wrong results.

An ordinary AC analysis or NOISE analysis cannot be used too as they are linear small signal analysis about the DC operating point and the squarer is based on the non-linearity of the MOSFET.

In order to simulate the circuit correctly the only available option was using transient analysis. Transient analysis takes the effect of non-linearity and can correctly predict the circuit behavior by solving it in time domain.

To get the conversion gain of the mixer, the ultra-wideband transmitted pulse is modeled in the simulator, the pulse is fed to the circuit and the output waveform is observed. Since we deal with the signal by its RMS power, the conversion gain is calculated by dividing the RMS value of the output signal by the RMS value of the input signal.

The pulse model as shown in Figure 3.6 consists of a pulse voltage generator, which outputs a square wave with a very low duty cycle. The pulse width is 1 ns and pulse repetition rate equal to the data rate (1Mbps). The resulting pulse is multiplied by a sine wave of frequency of 4 GHz in order to shift it in the middle of the required band using an ideal multiplier. The multiplier is implemented using Verilog-A code which is given in Appendix B. The resulting spectrum is a sinc function. The main lobe of the sinc function is taken and the side lobes are suppressed by means of an ideal forth order band pass filter from 3.1 GHz to 5.3 GHz, which is the desired frequency band.

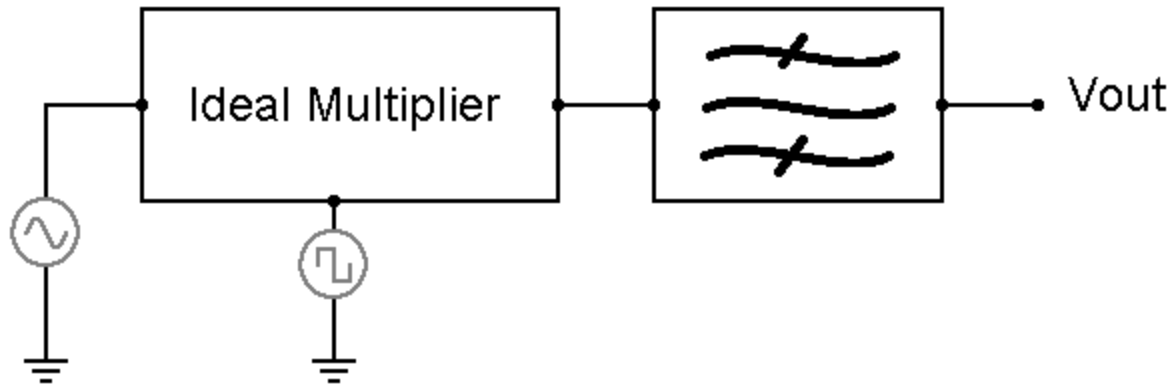

Figure 3.6: Schematic diagram of the pulse model

The resulting pulse is shown below in Figure 3.7:

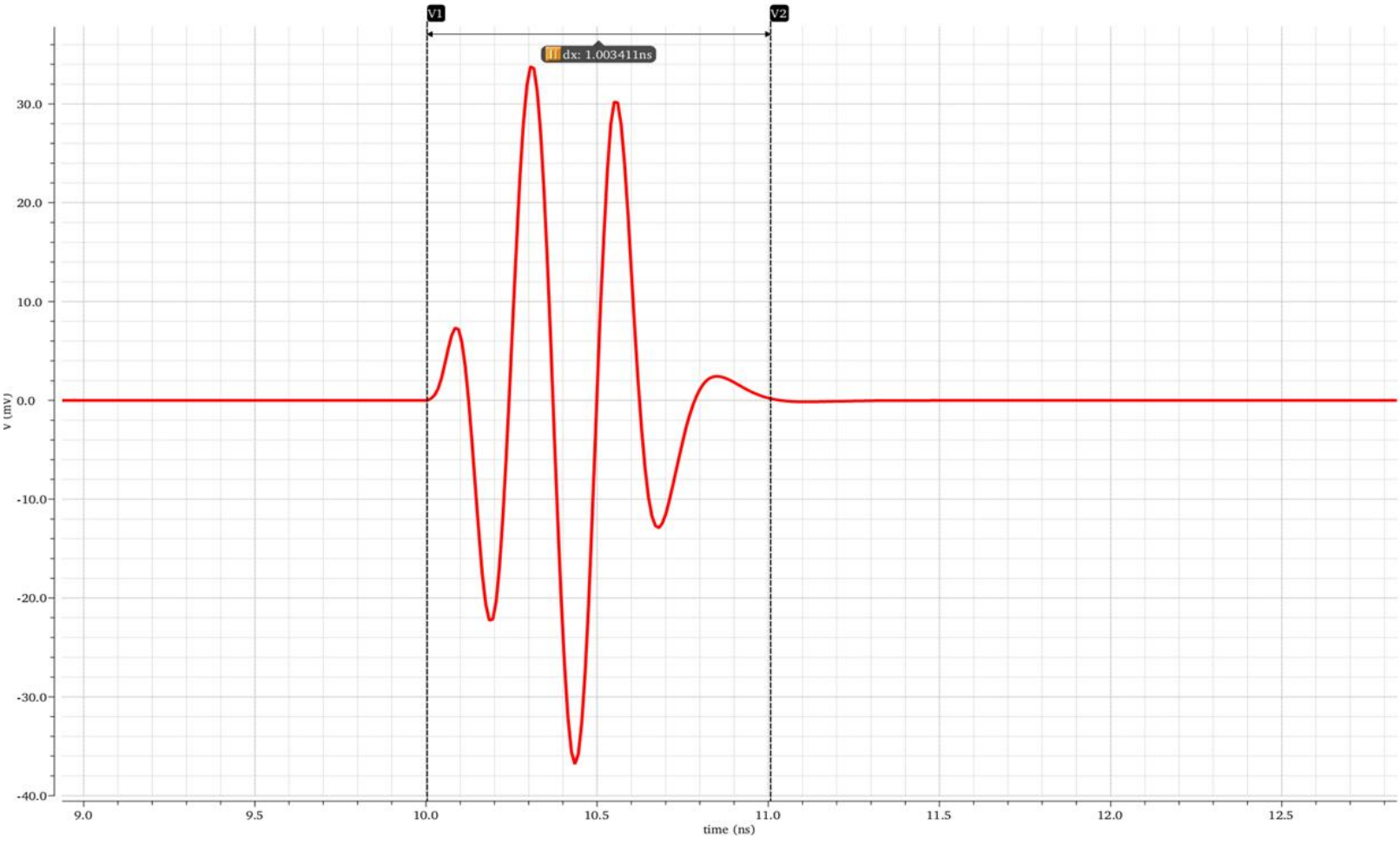

Figure 3.7: Ultra-wideband pulse waveform

The output waveform corresponding to the above pulse is shown below in Figure 3.8. The squaring action caused the pulse to have positive values of voltage for all time and eliminated the negative parts. Also it is clear that the variations in the pulse are much slower, which means that the squarer output has much lower frequency contents than the input. The maximum frequency content is limited by the output pole resulting from the parasitic capacitance at the output node and the output resistance of the squarer. This pole also acts as a low pass filter that suppresses the second harmonic of the input band which should result from squaring the input signal.

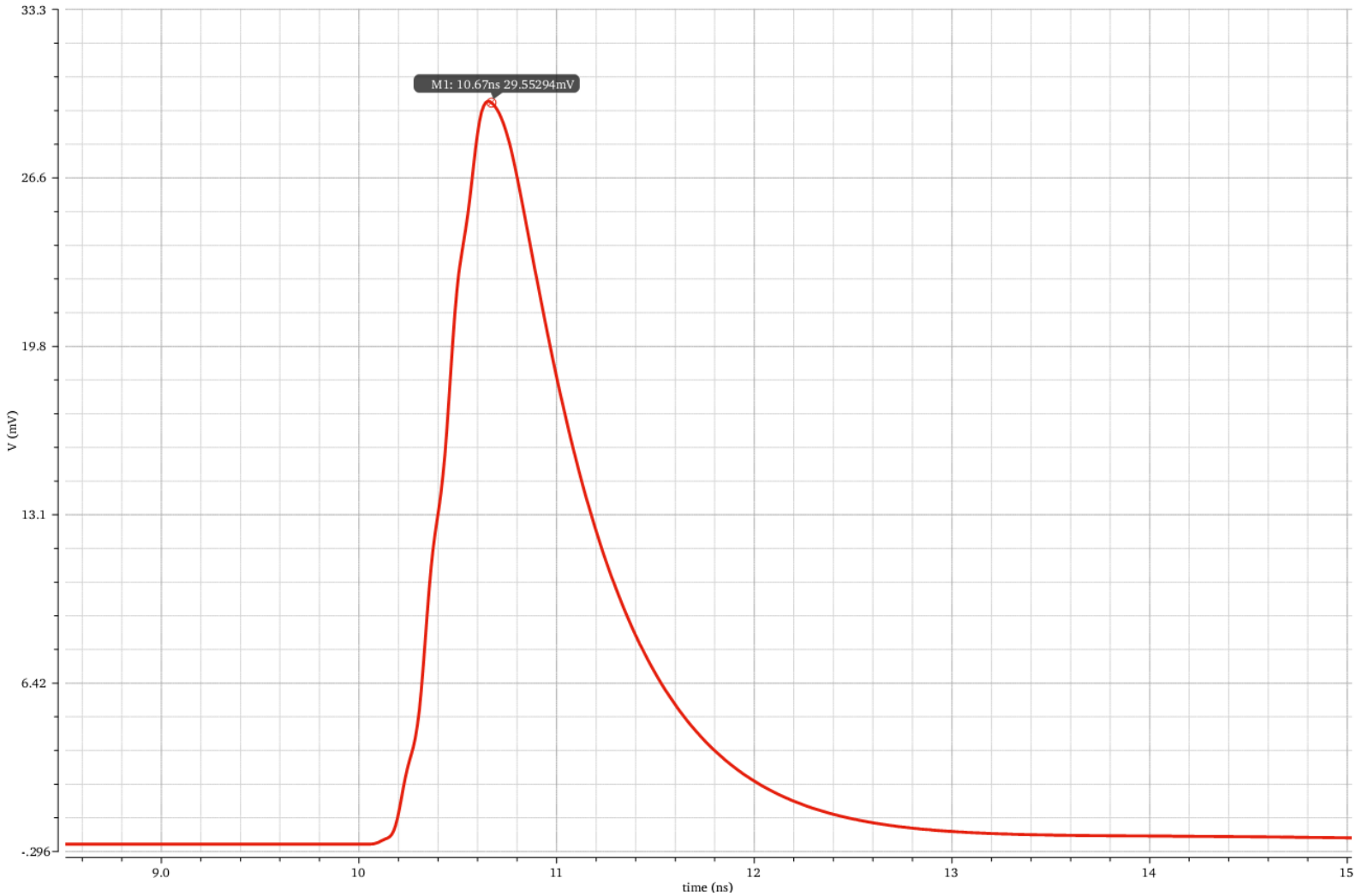

Figure 3.8: Squarer output waveform

A corner simulation was performed on this transient simulation and the output waveform was recorded in each case as shown in Figure 3.9. The RMS value of the output was also calculated and recorded in each case. The corner simulation was performed by writing Ocean code that simulates the circuit in each corner successively and is given in Appendix C – OCEAN CODE In the corner simulation, Vdd is varied 10% (from 1.62 to 1.98), the temperature is varied from -40 ℃ to 85℃, both the analog MOSFETS and the RF MOSFETS are varied in slow and fast PMOS and NMOS and the resistance is varied from minimum to maximum.

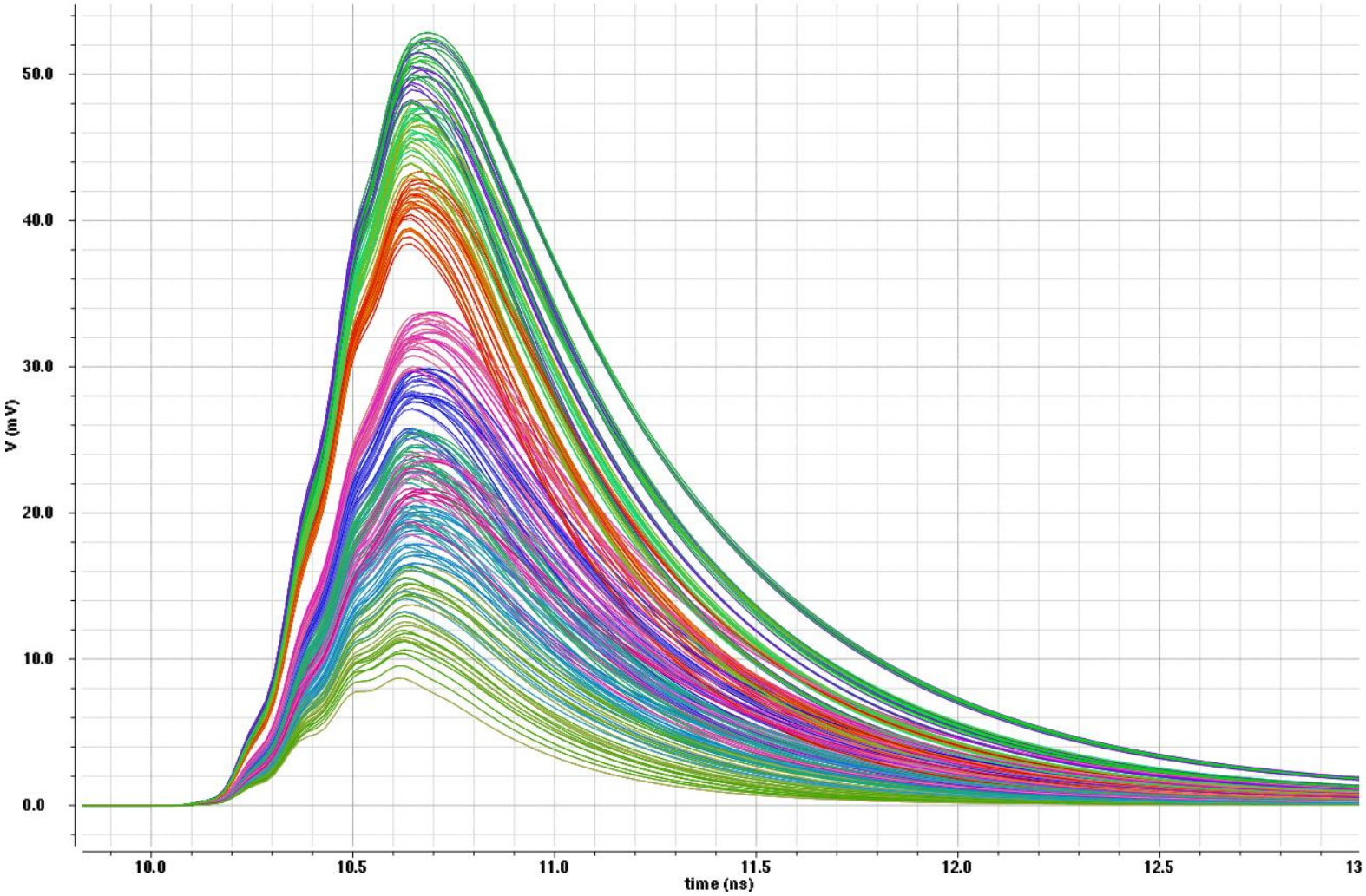

Figure 3.9: Squarer output waveform across corners

The resulting variation is large due to the change of mobility and hence the β of the transistors. This variation could be greatly reduced by using a constant gm bias circuit instead of a constant current source, but this was not implemented due to the lack of time.

The best corner and worst corners were found to be:

Parameter	Best Corner	Worst Corner
Analog MOSFET	FF	SF
RF MOSFET	SS	FS
Resistance	MAX	MIN
Temperature	-40℃	85℃
Vdd	1.98	1.62

Table 3.1: Squarer Best and worst corners

The summary of the results of this corner simulation at 1 Mbps, 33.78 mV peak input and 0.508 mV RMS input is given in the table below:

Parameter	Min	Typical	Max
Peak output	8.7 mV	29.6 mV	53.86 mV
RMS output	0.173 mV	0.679 mV	1.304 mV
RMS gain (ratio)	0.342	1.336	2.567
RMS gain (dB)	-9.3	2.516	8.19

Table 3.2: Summary of squarer corners

3.4.2 Noise simulation

In order to simulate the noise performance of the circuit, the input pulse was removed and a transient noise simulation was used. This simulation calculated a sample function of the waveform of the output noise of the squarer. The RMS value of the output noise waveform $v_{no,RMS}$ is calculated. The output noise power spectral density is given by:

$$\boldsymbol{v_{no}^2 = \frac{v_{no,RMS}^2}{F_{max}}} \qquad \textbf{(3.7)}$$

where F_{max} is the maximum noise frequency parameter that was input to the simulator (10 GHz was used).

Hence, the noise figure can be calculated as:

$$\boldsymbol{NF = 10\log(1 + \frac{v_{no}^2}{4KTR_s*(RMS_{GAIN})^2})} \qquad \textbf{(3.8)}$$

The results of the noise simulation for the squarer are given in the table below:

Parameter	Min NF	Typical	Max NF
v_{no}^2	820.4e-18 V^2	445.2e-18 V^2	66.98e-18 V^2
NF (dB)	21.798	24.8	28.405

Table 3.3: Summary of squarer noise results

It is noticed that the output noise power may increase while the noise figure decreases as the RMS gain significantly changes and affects the result.

3.4.3 Gain compression

The linearity of conventional narrowband mixers is measured by the 1 dB compression point by making a PSS sweep on input power and by the IIP3 which is based on the two tone test. Since the PSS analysis cannot be used in the case of the squarer as discussed above, the linearity of the squarer is measured by the 1 dB compression point. To measure it the input pulse power is changed in a parametric sweep and a transient simulation is run for each value. In each case, the input RMS power and output RMS power are calculated. The resulting plot saturates for large input power as shown Figure 3.10. A tangent line is drawn to the curve at small input and the value of the input power at which the output curves drops by 1 dB below this tangent is calculated as shown in Figure 3.11 and Figure 3.12 for the cases of highest and lowest gain corners respectively. The MATLAB code is given in Appendix A.

Since the squarer output voltage is proportional to the square of the input voltage, the conversion gain of the input increases linearly with the input amplitude. This is demonstrated in Figure 3.13, Figure 3.14 and Figure 3.15 for the typical, min and max cases respectively

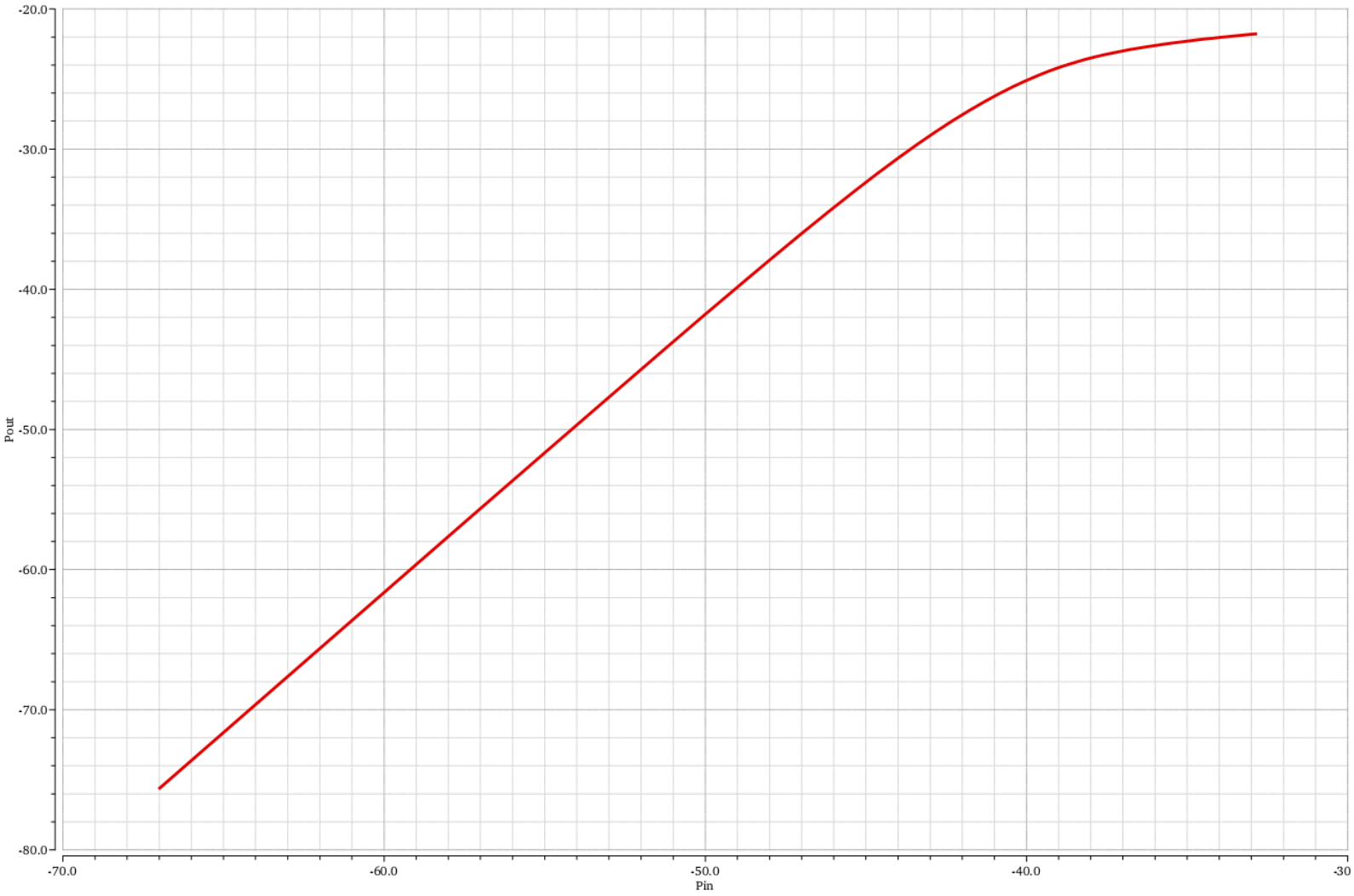

Figure 3.10: Squarer input power versus output power

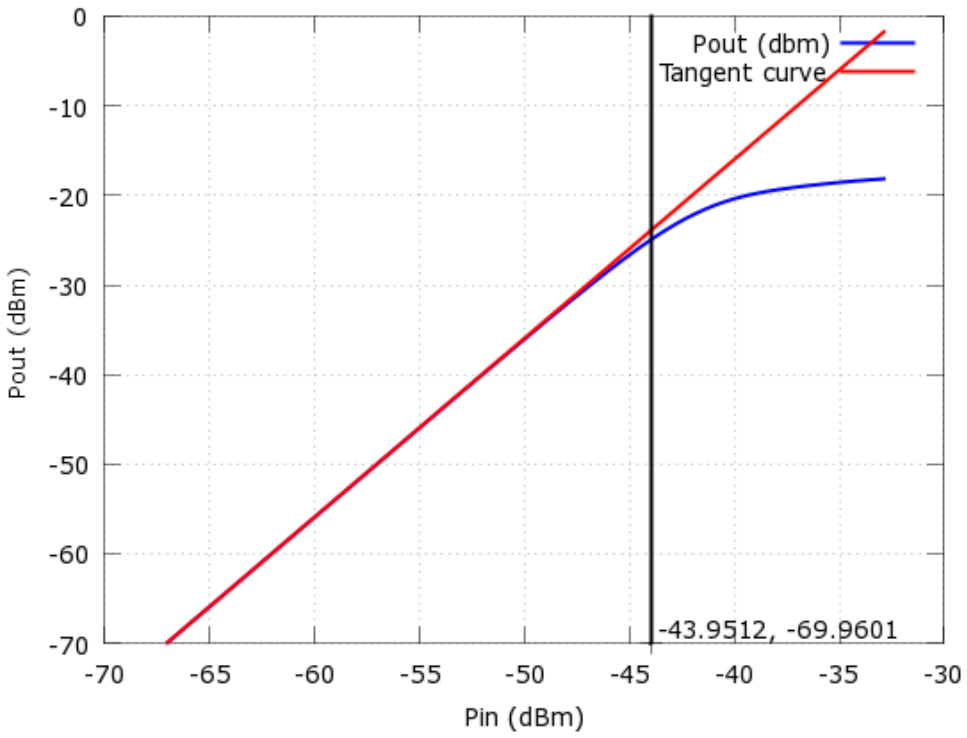

Figure 3.11: 1 dB compression for highest gain corner

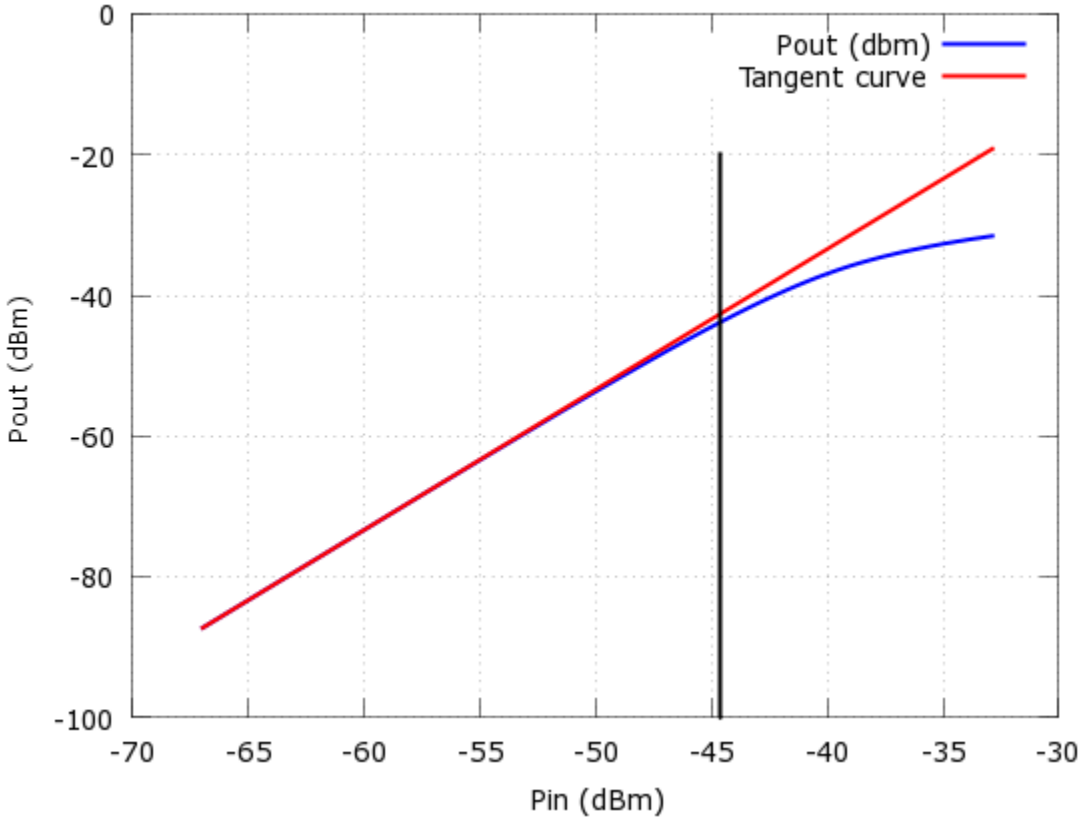

Figure 3.12: 1 dB compression for lowest gain corner

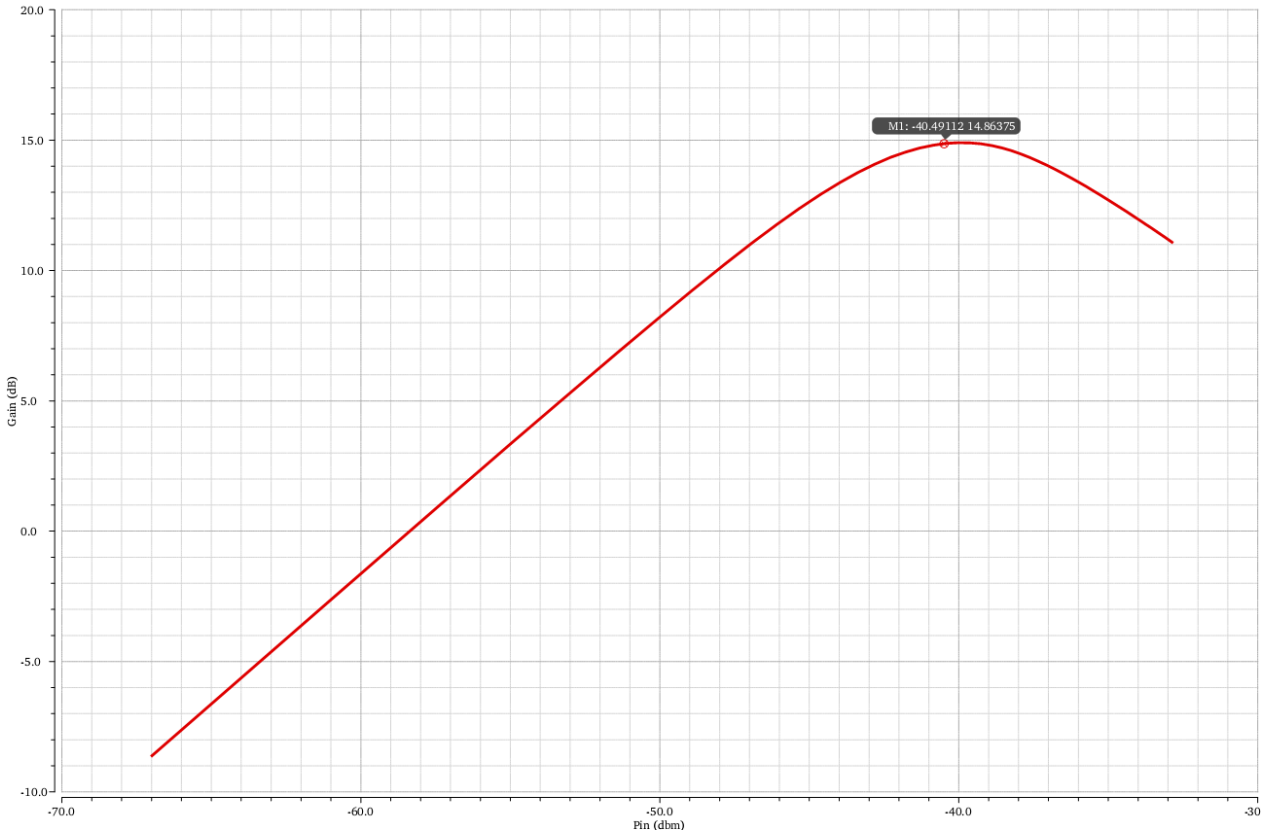

Figure 3.13: Conversion gain (dB) versus squarer input power (dBm) for the typical case

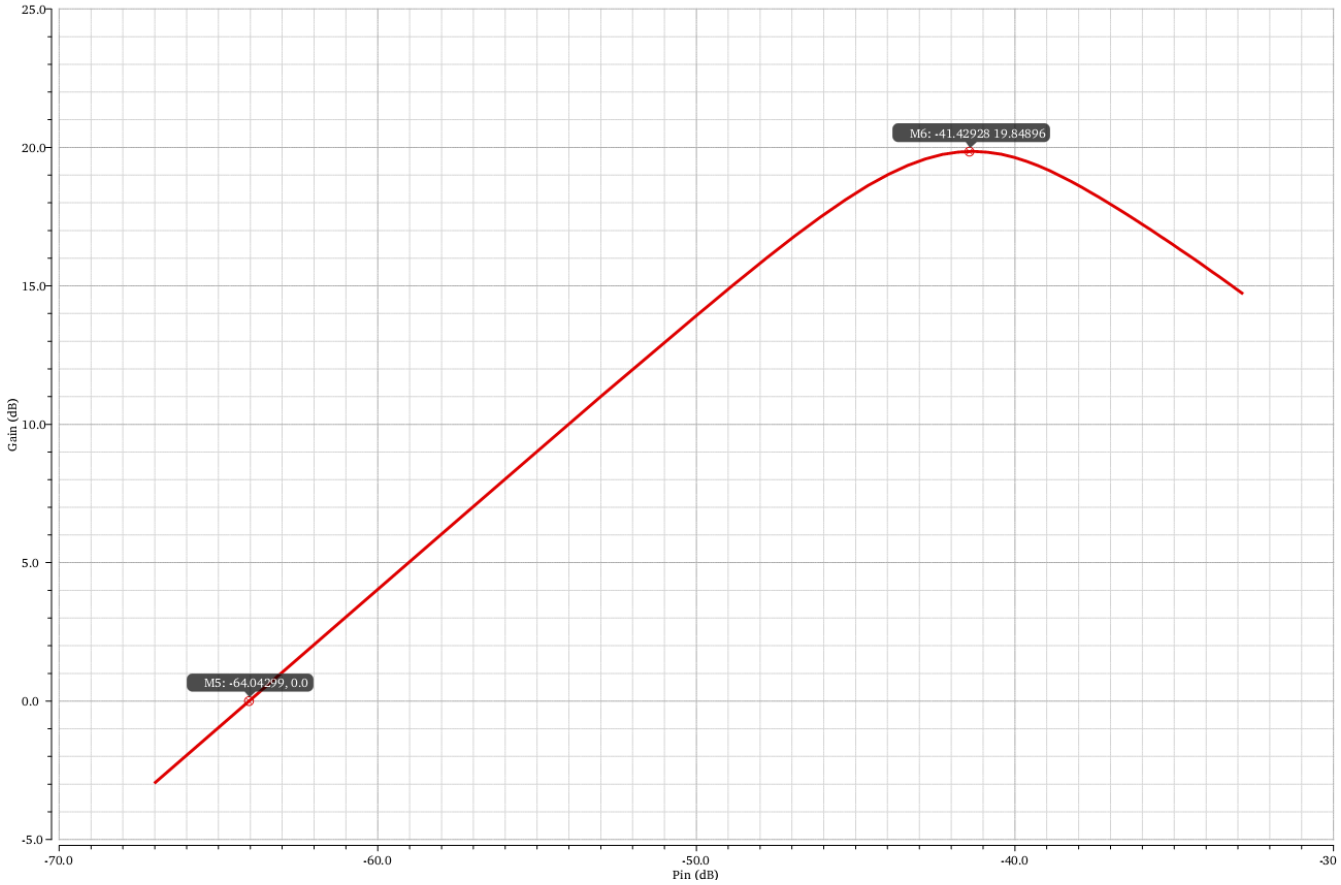

Figure 3.14: Conversion gain (dB) versus squarer input power (dBm) for the max case

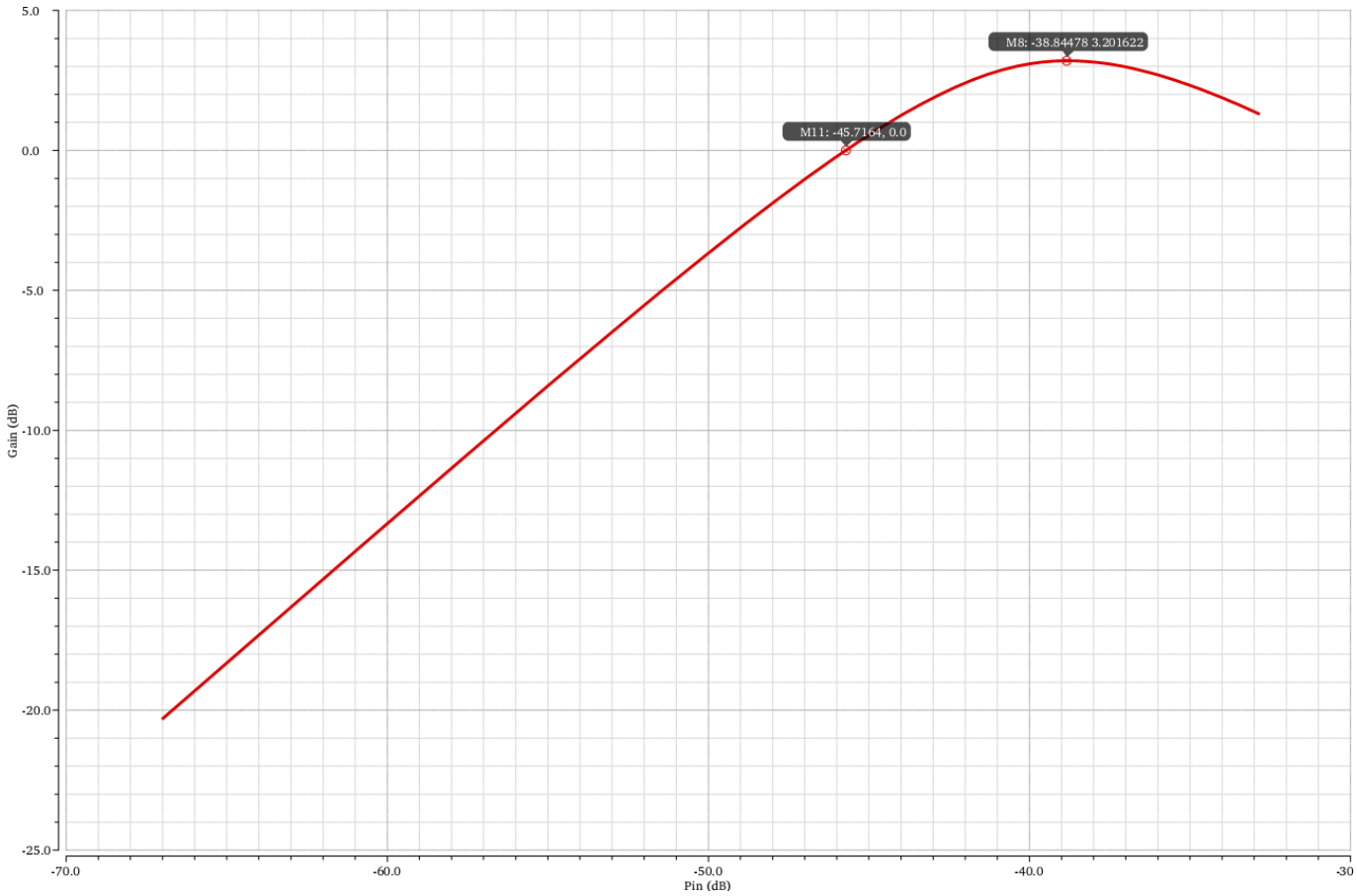

Figure 3.15: Conversion gain (dB) versus squarer input power (dBm) for the min case

3.4.4 Common mode feedback circuit

The AC response of the common mode feedback circuit is shown in Figure 3.16, which shows a gain of 16 dB and a 3 dB bandwidth of 1.95 MHz. The loop gain of the CMFB loop is also simulated using stability analysis to ensure that the common mode feedback loop is stable and will not oscillate. The loop amplitude response and phase response are shown in Figure 3.17, which shows that the loop is stable with a phase margin of about 19 degrees, which is not so good but the circuit is stable.

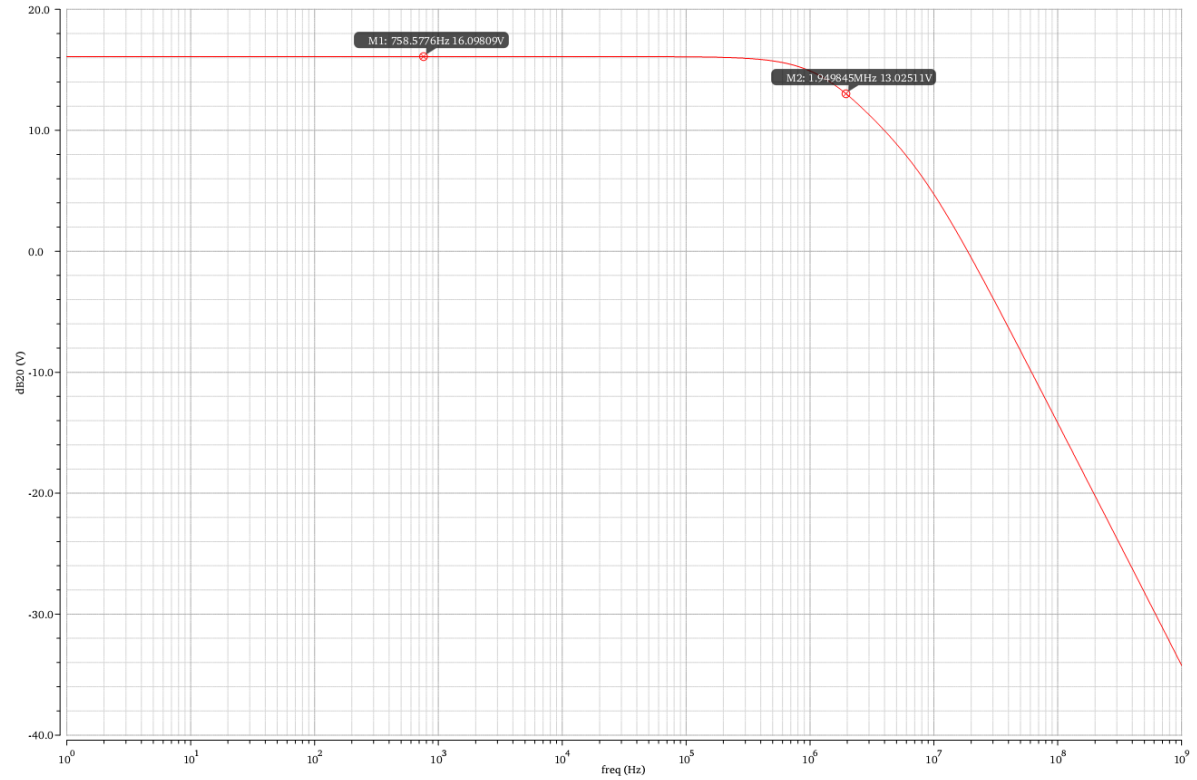

Figure 3.16: AC response of the CMFB circuit

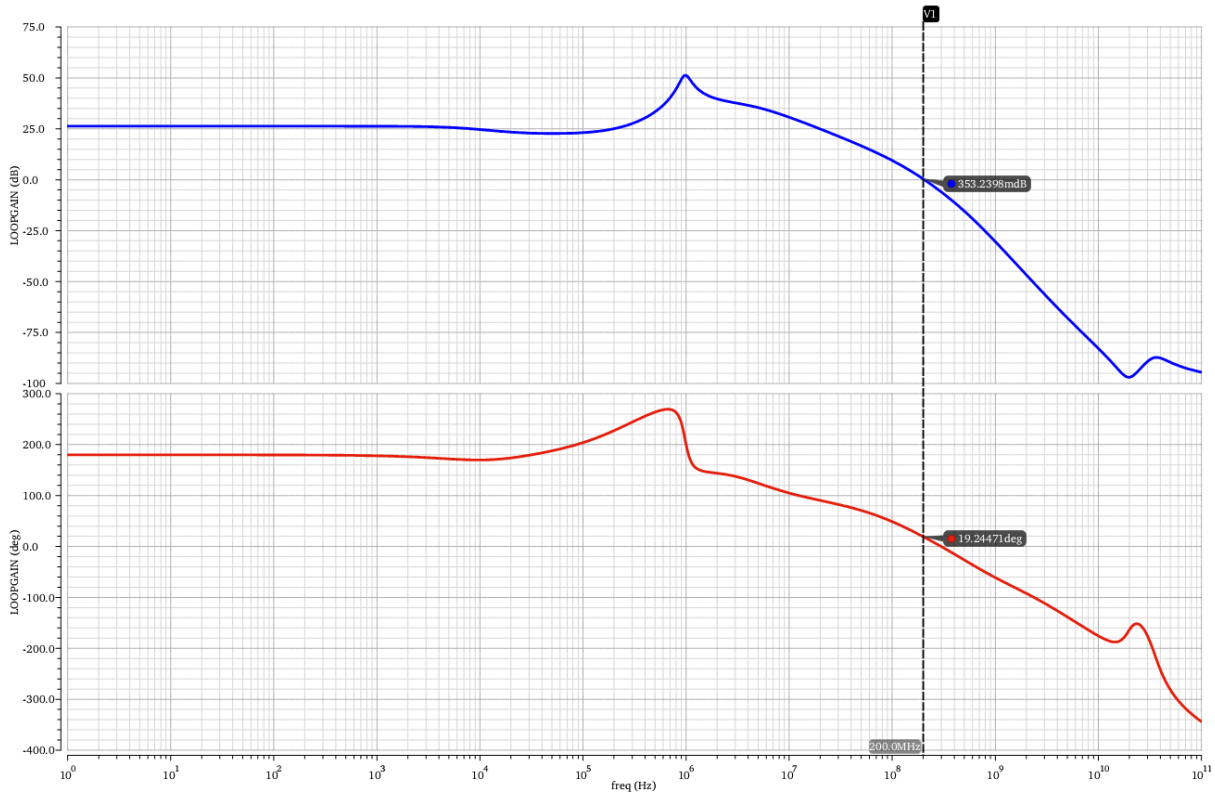

Figure 3.17: Loop gain of the CMFB circuit

The summary of the required and achieved specs for the squarer block are shown in Table 3.4:

Spec	Required	Achieved
Gain	> 0 dB	0.9 dB
NF	< 30 dB	28.4 dB

Table 3.4: Summary of squarer achieved specs

References

1. *Ultra-Wideband Radio.* **Robert A. Scholtz, David M. Pozar, Won Namgoong.** s.l. : EURASIP Journal on Applied Signal Processing, 2005.

2. Federal Communications Commission (FCC), "Revision of part 15 of the commission's rules regarding ultra-wideband 98–153, FCC 02–48;. Adopted: February 2002; Released: April 2002.

3. *Wikipedia.* [Online] http://en.wikipedia.org/wiki/Shannon%E2%80%93Hartley_theorem.

4.] Y.-L. Chao and R. A. Scholtz "Optimal and suboptimal receivers forultra-wideband transmitted reference systems,"IEEE Global Telecommun. Conf.'03, vol. 2, pp. 759-763, Dec. 1-5, 2003.

5. **Khan, Muhammad Gufran.** *on coherent and non-coherent receiver structures for impulse radio uwb systems.* s.l. : Blekinge Institute of Technology, 2009.

6. D. Cassioli, M. Z. Win, F. Vatalaro, and A. F. Molisch, "Performance of low-complexity Rake reception in a realistic UWB channel", Proc. IEEE Int. Conf. on Commun., pp. 763767, May 2003.

7. Ning He, C. Tepedelenlioglu, "Performance analysis of non-coherent UWB receivers at different synchronization levels", IEEE Global Telecommunications Conference, 2004. GLOBECOM '04., vol. 6, pp. 3517- 3521.

8. R. Price, P. E. Green, "A Communication Technique for Multipath Channels", Proceedings of the IRE, vol. 46, no. 3, pp. 555-570.

9. T. Q. S. Quek, M. Z. Win, "Ultrawide bandwidth transmitted-reference signaling", Communications, 2004 IEEE International Conference on,vol.6, pp. 3409- 3413.

10. J. H. Reed et. al. An Introduction to Ultra Wideband Communication Systems, Prentice Hall, 2005.

11. S. Paquelet, L. M. Aubert, and B. Uguen, "An impulse radio asynchronous transceiver for high data rates", in Proc. IEEE Ultrawideband Syst. Technol. (UWBST), Kyoto, Japan, pp. 15, May 2004.

12. M. Weisenhorn and W. Hirt, "Robust noncoherent receiver exploiting UWB channel properties", in Proc. IEEE Conference on UWB Systems and Technologies, pp. 156-160, May 2004.

13. M.E. Sahin, I. Guvenc, H. Arslan, "Optimization of energy detector receivers for UWB systems", IEEE 61st Vehicular Technology Conference,2005. VTC 2005-Spring., vol. 2, pp. 1386- 1390.

14. *Weighted Non-coherent Energy Detection Receiver for UWB OOK Systems.* **Dazhong Mu, Zhengding Qi.** s.l. : ICSP, 2008.

15. *A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise.* **Yi-Jing Lin, Shawn S. H. Hsu, Member, IEEE, Jun-De Jin, and C. Y. Chan.**

16. *Broadband CMOS LNAs for IR-UWB Receiver.* **Xinzhong Duo, Li-Rong Zheng, Mohammed Ismail, Hannu Tenhunen.** s.l. : Laboratory of Electronics and Computer Systems Royal Institute of Technology (KTH), Electrum 229, 16440 Kista, Sweden.

17. *Low-Power CMOS RF Front-end for Non-CoherentLow-Power CMOS RF Front-end for Non-Coherent.* **Yuan Gao, Yuanjin Zheng, Chun-Huat Heng.** 2008, IEEE.

Appendix A – MATLAB CODE

A.1 RECEIVER SYSTEM SIMULATION

TxRx_tb.m

```
close all;
ts=1e-11;
t=0:ts:10e-6;
pulse_width = 1e-9;
input = 0.5+0.5*square(2*pi*200e3*t);
tx_out = UWB_Tx(input,ts,pulse_width,t);
tx_power = sum(tx_out.^2)*ts/t(end)
tx_power_dbm = 10*log10(tx_power/1000)
figure(1);
subplot(2,1,1);
plot(t,input);
title('Data Input');
xlabel('Time');
grid on;
axis([0,10e-6,-0.1,1.1]);
subplot(2,1,2);
plot(t,tx_out);
grid on;
title('Transmitter Output');
xlabel('Time');
% figure(4)
[tx_out_f f] = time2spec(tx_out,1/ts);
% semilogx(f,20*log10(tx_out_f));
% title('Transmitter output');
% xlabel('Freq');
% ylabel('Amplitude');
```

```
figure(7)
semilogx(f,20*log10(tx_out_f));
title('Filtered Signal with gain');
xlabel('freq');
ylabel('Amplitude');

received = UWB_Rx(tx_out,t,ts);
figure(2)
plot(t,received);
```

UWB_Tx.m

```
%       UWB Transmitter
%       output = UWB_Tx(input,ts,pulse_width,t)
%       output : received signal
%       input : input signal
%   ts : sampling time
%       pulse_width : width of UWB pulse
%       t: time

function output = UWB_Tx(input,ts,pulse_width,t)
        pulses = Pulse_Generator(input,pulse_width,ts,t);
        figure(5)
        [a f] = time2spec(pulses,1/ts);
        semilogx(f,20*log10(a));
        title('Unfiltered Spectrum');
        xlabel('freq');
        ylabel('Amplitude');
        pulses = pulses * 1000;
        output = tx_filter(pulses ,ts,3.5e9,4.5e9);

endfunction
```

UWB_Rx.m

```
%       UWB Receiver
%       output = UWB_Rx(input,ts)
%       output : received signal
%       input : input signal
%       t : time
%   ts : sampling time

function output = UWB_Rx(input,t,ts)
        gain = 1;
        fdump = 1e6;
        dump = 0.5+0.5*square(2*pi*fdump*t+1);
        figure(3)
        plot(t,dump)
        squared = input.*input;
        figure(8);
        plot(t,squared);
        figure(9);
        [squared_f f] = time2spec(squared,1/ts);
        power_to_13G = sum(squared_f(find(f<0.6e9)).^2)*(f(2)-f(1))/f(end);
%powerp_to_0.6G =  80
        power_to_40G = sum(squared_f(find(f<4e9)).^2)*(f(2)-f(1))/f(end);
%powerp_to_40G =  84.874
        total_p = sum(squared_f.^2)*(f(2)-f(1))/f(end);
        powerp_to_13G = power_to_13G/total_p*100
        powerp_to_40G = power_to_40G/total_p*100
        semilogx(f,20*log10(squared_f));
        % plot(f,squared_f);
        title('Squarer output spectrum');
        xlabel('freq');
        ylabel('Amplitude');
```

```
        integ_out = integrate_dump(squared,dump,ts);
        output = integ_out;

    endfunction
```

integreate_dump.m

```
    %   Integrate and Dump
    %   output = integrate_dump(input,ts)
    %   output : output signal
    %   input : input signal
    %  ts : sampling time

    function output = integrate_dump(input,dump,ts)
        clock = diff(dump);
        dump_position = find(clock > 0.5);
        output = 0;
        sum = 0;
        for(i=1:length(input))
            if (find(dump_position==i))
                sum = 0;
            else
                sum = sum + input(i)*ts;
            end
            output(i) = sum;
        end
    endfunction
```

delay.m

```
    %   Delay a signal
    %   result = delay(in, delay, ts)
    %   result : delayed signal
    %   in : input signal
```

```
%       delay_val : required delay seconds
%   ts : sampling time

function result = delay(in,delay_val,ts)
        n_delay = round(delay_val/ts);
        result=0;
        result(1+n_delay:length(in)) = in(1:end-n_delay);

endfunction
```

A.2 SQUARER 1 dB GAIN COMPRESSION POINT

```
input = csvread('Pout_Pin_min.csv');
x = input(:,1);
y = input(:,2);
x = x(2:end);
y = y(2:end);
plot(x,y,'linewidth',2);
hold on;
xp = x(2);
yp = y(2);
slope = (y(2)-y(1))/(x(2)-x(1));
tangent = yp + slope * (x - xp);
plot(x,tangent,'r','linewidth',2);
comp_pt_index = find(tangent-y>1);
comp_pt_index = comp_pt_index(1);
plot ([x(comp_pt_index) x(comp_pt_index)],[-100 -20],'k','linewidth',2);
legend('Pout (dbm)','Tangent curve');
grid on;
xlabel('Pin (dBm)');
ylabel('Pout (dBm)');
hold off;
```

Appendix B – Verilog-A CODE

B.1 IDEAL MULTIPLIER CODE:

```
// VerilogA for Project_v0.04, Mixer_ideal, veriloga

`include "constants.vams"
`include "disciplines.vams"

module Mixer_ideal(in1,in2,out);
        electrical in1,in2,out;
        analog
                V(out) <+ V(in1)*V(in2);

endmodule
```

Appendix C – OCEAN CODE

C.1 SQUARER CORNER SIMULATION

```
simulator( 'spectre )
design( "/simulation/squarer_v1_tb/spectre/schematic/netlist/netlist")
resultsDir( "/simulation/squarer_v1_tb/spectre/schematic" )

filehandle = outfile("~/Desktop/rms_corners.csv" "a")
fprintf(filehandle "analog_mos,mos,res,temp,vdd,rms\n")
desVar(             "vdd" 1.8       )

clearAll()
mos = list("ss" "tt" "ff" "fs" "sf" )
analog_mos = list("ss" "tt" "ff" "fs" "sf" )
temp = list(-40 27 85)
vdd = list(1.62 1.8 1.98)
res = list("typ" "min" "max")
foreach( analog_mos_var analog_mos
        foreach( mos_var mos
                foreach(res_var res
                        foreach( temp_var temp
                                temp(temp_var)
                                foreach( vdd_var vdd
                                        desVar( "vdd" vdd_var)
                                        modelFile(

list("/users/soft/PDKs/PDK_LF150i_V2_0_0/analog/models/spectre/lf150.scs" sprintf(nil
"%s_hs" analog_mos_var))

list("/users/soft/PDKs/PDK_LF150i_V2_0_0/analog/models/spectre/lf150rf.scs" sprintf(nil
"%s_rf_hs" mos_var))
```

```
list("/users/soft/PDKs/PDK_LF150i_V2_0_0/analog/models/spectre/lf150rf.scs" sprintf(nil
"resrf_%s" res_var))

'("/users/soft/PDKs/PDK_LF150i_V2_0_0/analog/models/spectre/lf150rf.scs" "mimrf_typ")
                                        )
                                        analysis('tran ?stop "25n"  ?maxstep "0.1n"  )
                                        save( 'v  "/out" )
                                        run()
                                        selectResult( 'tran )
                                        plot(getData("/out") ?expr list( sprintf(nil "Tran:
analog_mos_%s mos_%s res_%s temp_%d vdd_%g" analog_mos_var mos_var res_var
temp_var vdd_var ) ))
                                        result = VT("/out")
                                        rms_value = rms(result)
                                        fprintf(filehandle "%s,%s,%s,%d,%g,%g\n"
analog_mos_var mos_var res_var temp_var vdd_var rms_value)
                                        drain(filehandle)
                                    )
                                )
                            )
                        )
)
```