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DESIGN OF RF RECIEVER FOR IEEE 802.16M STANDARD

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Abstract

In this project, possible LNA, Mixer and VCO suitable for RF front-ends of wireless receivers are proposed. The main objective in the project is to meet the requirements of the IEEE 802.16m Standard for WiMAX.

The proposed LNA is capable of providing high power gain in the 3.25 GHz band with a gain of 21 dB, on-chip input matching circuit, and high reverse isolation.

The LNA is a differential type CMOS amplifier following a stage that converts the single ended signal from the antenna to a differential-ended signal.

A Gilbert-cell down-converting mixer was designed for integrated receiver front-ends. This mixer is suitable for RF receivers that require IF output of 250 MHz.

The gain of this mixer equals 10.5 dBm, with noise figure of 11.9 dBm.

In this research, a voltage controlled oscillator design is proposed. The generated signal has a frequency of 3.016-2.985 GHz, phase noise of -116.2 dBc @ 1 MHz and output power of 4.1 dBm.

Each design in this research is implemented using TSMC 130nm and TSMC 180nm, the EDA programs are Agilent Advanced design system 2009 and Cadence Virtuoso. Layouts are designed using Cadence Virtuoso and Tanner tools 13.0.

Chapter -1
1.Introduction

1.1. Scope

The goal of this research is to design complete radio frequency (RF) receiver with heterodyne architecture in an integrated circuit. The research team focused on the receiver front-end design in the 3.25 frequency band which is suitable for using for IEEE 802.16m standard for WiMAX, a modern competitive communication technology.

1.2. Problem Overview

Many of today's communication devices, especially mobile devices, require high performance, low power consumption ICs to insure steady connectivity and longer battery life. The evolution of digital devices goes from small to smaller, which requires minimizing the sizes of ICs as possible.

One of the best ways to meet this is by fully integrating the communication circuit in one single chip. This would lead to smaller size, lower power consumption and higher performance.

The problem of trade-offs in analog designs is clearly observed while thinking about full integration of RF receiver in one chip, besides many other problems including matching, size, noise transfer between blocks.

1.3. Outline

In chapter 2, the concepts of RF front ends are discussed with its common architectures and techniques, besides the basic concepts in RFIC design.

In chapter 3, a quick overview on the IEEE 802.16m standard for WiMAX is discussed, explaining its features over older standards for WiMAX.

In chapter 4, a review of the Low Noise Amplifier is made, talking about its common topologies, then discussing the proposed design and results in chapter 5.

Chapter 6, talking about the mixer, its design and specifications, then the proposed design it presented in chapter 7.

The VCO is illustrated in chapter 8 with its different schemes and characteristics; the final design is then presented in chapter 9.

Chapter 2:
2. Background and literature review

2.1. RF front-end

Introduction

The RF front end is generally defined as everything between the antenna and the digital baseband system. For a receiver, this "between" area includes all the filters, low-noise amplifiers (LNAs), and down-conversion mixer(s) needed to process the modulated signals received at the antenna into signals suitable for input into the baseband analog-to-digital converter (ADC). For this reason, the RF front end is often called the RF-to-baseband portion of a receiver.

Conversely, a transmitter is an up converts an outgoing signal prior to passage through a high power amplifier. In this case, non-linearity of the amplifier is a primary concern. Yet, even with these differences, the design of the receiver front end and transmitter back end share many common elements—like local oscillators.

Still, regardless of the level of integration, the basic RF architecture remains unchanged: signal filtering, detection, amplification and demodulation. More specifically, a modulated RF carrier signal couples with an antenna designed for a specific band of frequencies.

2.2. Analog RF Front End Architectures

1- Super-heterodyne receiver.

2- Direct conversion receiver.

Super heterodyne receiver architecture

The concept of heterodyning an RF signal to convert it to a lower frequency was developed by Armstrong in 1918. The original block diagram of Armstrong's receiver is shown in Figure 1.

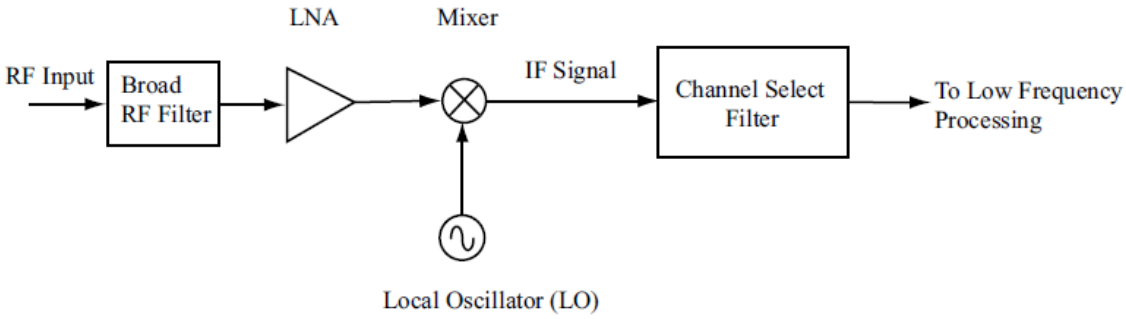


Figure 1: Block diagram of Armstrong's super-heterodyne receiver.

It was thought that the super-heterodyne architecture would be the best architecture for receivers because of its high sensitivity, selectivity and additional advantages including:

- Amplification of the input signal can be done at low frequency where it is easier to achieve high gain.
- Amplification is done at two stages and at two different frequencies. Thus, there is less possibility of regenerate feedback and instability.
- High order and narrow band filters are easier to build in the low frequency than the RF.
- Adjustment of the low frequency IF band-pass filters can be done just once, and after that the tuning can be achieved by varying the heterodyne oscillator frequency.

In a super-heterodyne receiver, the input signal is first amplified at RF in a tuned stage, then down converted by a mixer to a lower intermediate frequency, and substantially amplified in a tuned IF stage containing highly selective passive band-pass filters.

The main issue in the super-heterodyne receiver is the trade-off between image rejection and adjacent channel suppression. If the IF frequency is chosen to be high, as shown in Figure 2, the image signal is greatly attenuated whereas nearby interferers remain at high level. On the other hand if the IF frequency is selected to be low, the image corrupts the down converted signal but the adjacent interferers are suppressed significantly as illustrated in Figure 3.

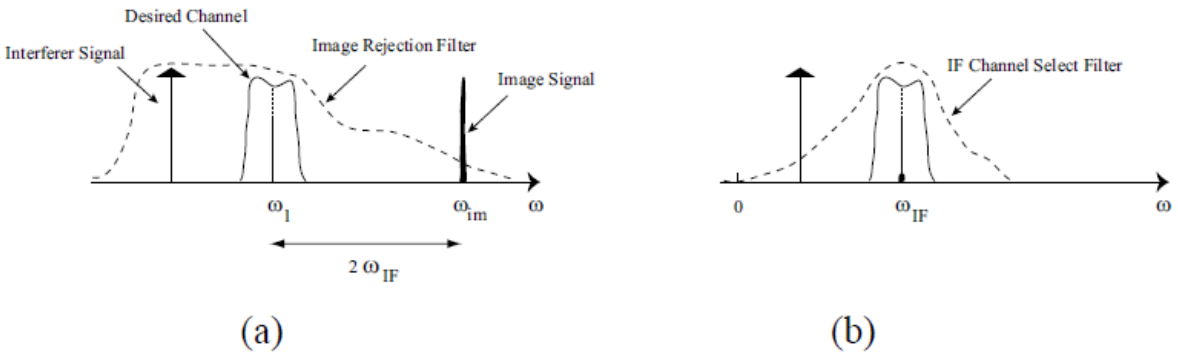


Figure 2: The frequency scheme of a super-heterodyne receiver with high IF. (a) before down conversion and (b) after down conversion.

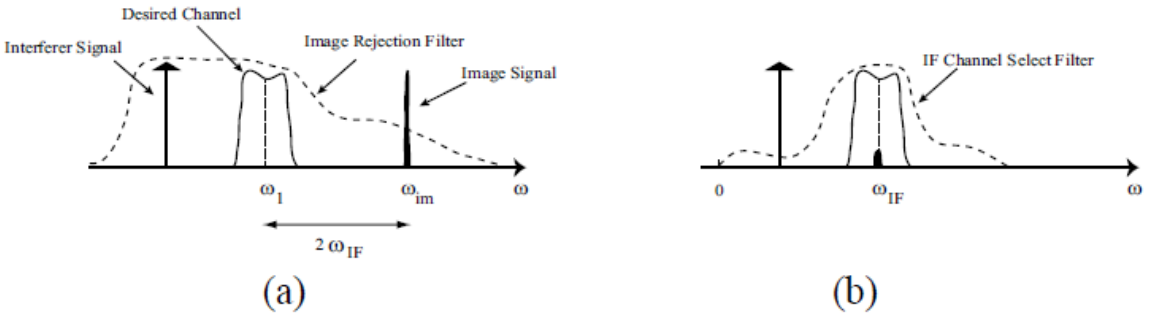


Figure 3: The frequency scheme of a super-heterodyne receiver with low IF.

Direct conversion RF front-end architecture

Direct conversion, also called zero-IF was introduced many decades ago, and is the natural approach to down convert a signal from RF to baseband.

In contrast to the multi-step down conversion approach of the super-heterodyne receiver, a direct conversion receiver moves the signal energy from the received RF frequency down to the baseband in a single step. The block diagram of a direct conversion receiver is illustrated in Figure 4.

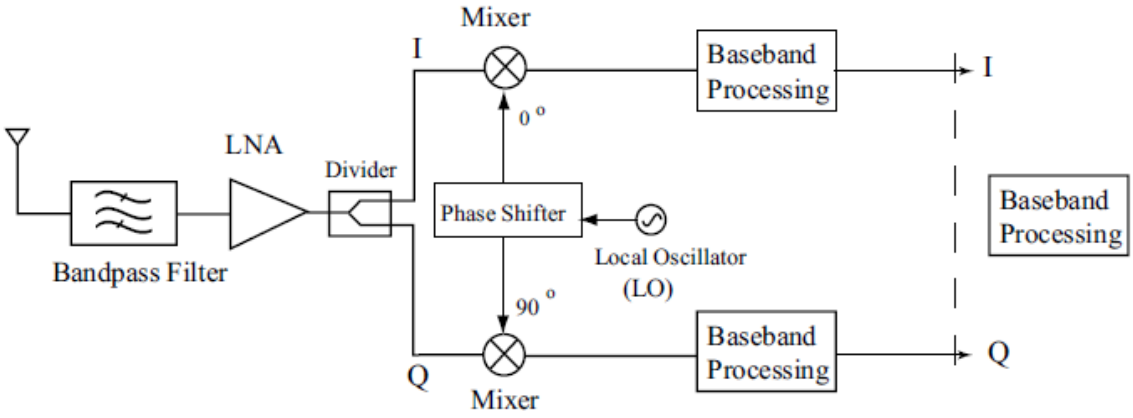


Figure 4: Block diagram of a direct conversion receiver.

The center of the generated IF signal in a direct conversion receiver is at zero frequency, therefore no image response is produced, and no image rejection filter is needed. Therefore, the signal does not need to be routed off-chip to an image rejection filter in which a 50 ohm drive is required for load.

Interferer signals above and below the desired signal frequency are down converted to the IF baseband frequencies, above that of the desired signal. They will be removed from the processed signal in the baseband by low-pass filtering. For these reasons, the direct conversion receiver architecture can be viewed as a selective demodulator operating directly at the RF frequency.

Today, all of the transmitters in digital cellular telephones use direct conversion to produce a single sideband output. In the receiver however, the classical super-heterodyne architecture is still more common. Only a handful of IC manufacturers use direct conversion for their receiver products. In Alcatel has publicized its use of this architecture for its GSM and DECT receivers. However, Alcatel's front-end is a small IC and is implemented in bipolar technology.

Direct conversion architecture issues

1- DC offset:

DC offsets are considered the most serious problem of direct conversion. As in the direct conversion receiver the RF signal is transformed to zero frequency, a large DC offset can corrupt the signal and saturate the signal processing blocks such as an ADC.

2- I/Q Mismatch:

To recover the [I] and [Q] components of the signal, the LO signals fed into the mixers must be 90° apart in phase. Any change in this angle will corrupt the down converted signal.

3- Flicker noise.

Random trapping and releasing of charge carriers in submicron devices introduces flicker noise also known as *1/f* noise or pink noise. The trapping and releasing of the charge carriers mostly happens at low frequency.

Due to the effect of flicker noise, the noise figure of the receiver increases, affecting the sensitivity of the receiver.

4- Even-order Distortion:

The nonlinear behavior of the active element of the circuits leads to generating undesired baseband components which affect the desired baseband signal.

Due to the advantages and disadvantages of both architectures, we chose the super heterodyne architecture for our project due to the features it shows against the direct conversion issues.

2.2 Access techniques:

Three commonly used techniques for accommodating multiple users in wireless communication are frequency division multiplexing (FDMA), time division multiple access (TDMA) , and code division multiple access(CDMA).FDMA and TDMA are old technologies and have been used for quite a while .code division multiple access is the emerging technology for many new cellular phone systems.

Frequency Division Multiple Access (FDMA)

The available frequency band is split into a specific number of channels, and the bandwidth of each channel depends on the type of information to be transmitted .To transmit a number of channels over the same system , the signals must be kept apart so that they do not interfere with each other.

The guard band is placed between two adjacent signals to avoid interference. A multiplexer is used to combine the signals, and the combined signals are then up converted and amplified.

In the receiver, the signals are separated by a multiplexer that consists of many filters. The information is recovered after the demodulator.

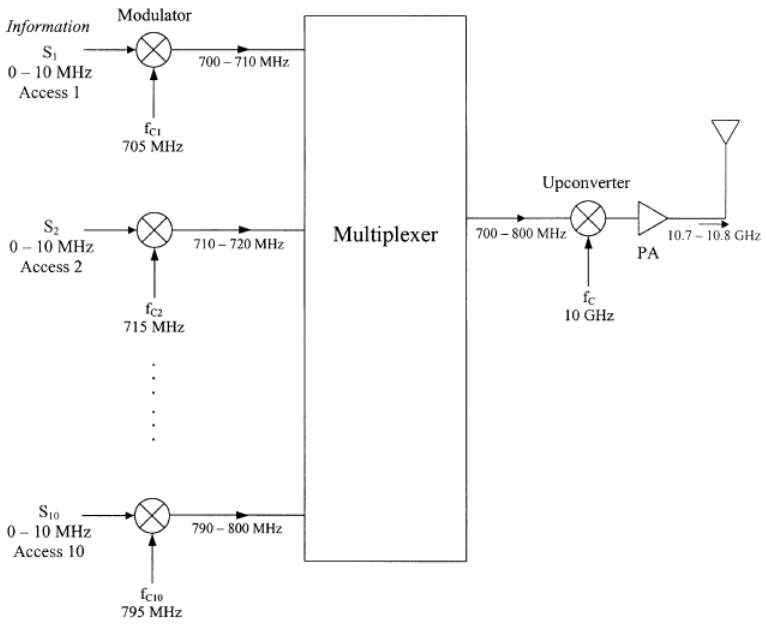


Figure 5: FDMA architecture.

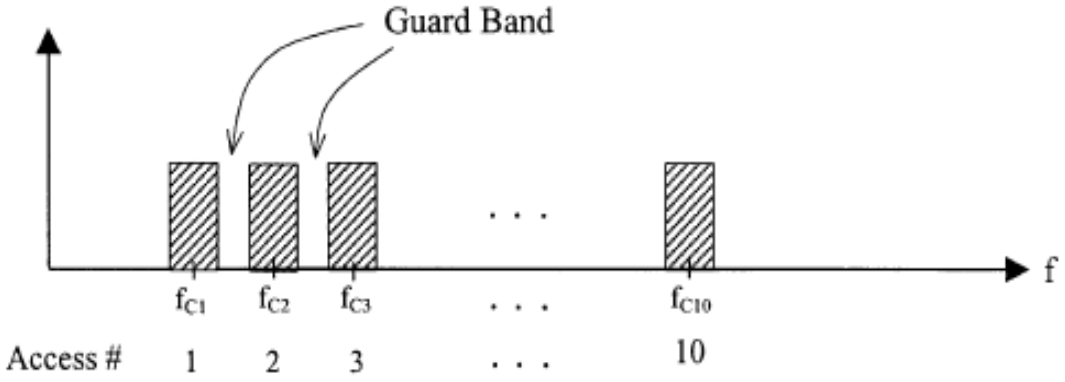


Figure 7: frequency spectrum in FDMA

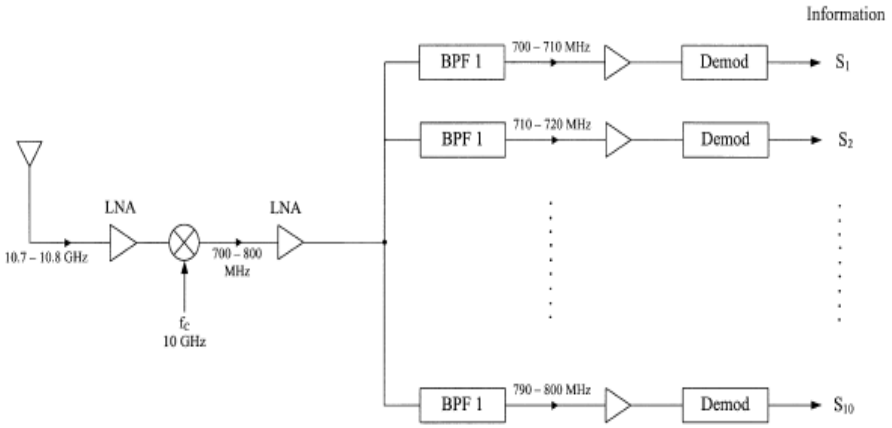


Figure 8: receiver of FDM system

The advantage of FDMA is that no network timing is acquired , and the major disadvantages include required power control , a wide frequency band and interference caused by intermodulation and sideband distortion.

Time Division Multiple Access (TDMA):

TDM system uses a single frequency band to simultaneously transmit many signals (channels) in allocated time slots. These different channels time-share the same frequency band without interfering with each other.

The advantages of TDMA as compared to FDMA are the requirement of a narrower frequency bandwidth, invulnerability to inter-channel crosstalk and imperfect channel filtering, no power control required, and high efficiency, the disadvantage is the requirement of network timing.

In TDMA transmitting system, the samples are interleaved, and the composite signal consists of all of the interleaved pulses. A commutator or switch circuit is normally used to accomplish the data interleaving.

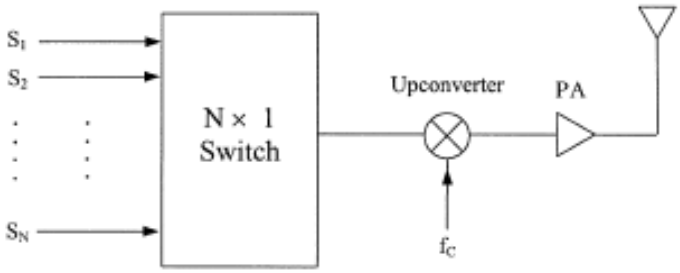


Figure 9: transmitter of TDMA system

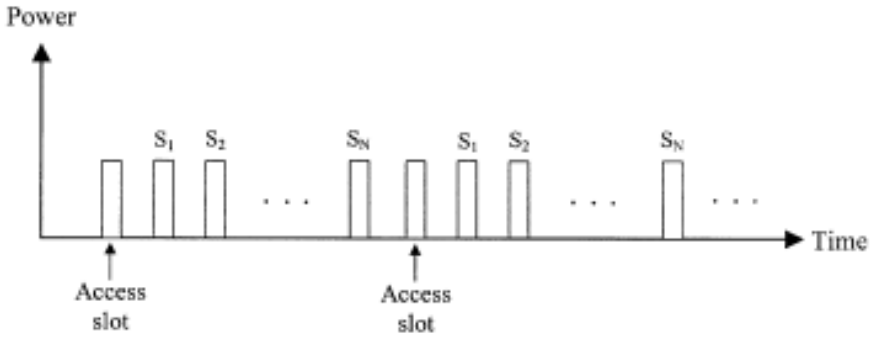


Figure 10: data slot allocation for N signals

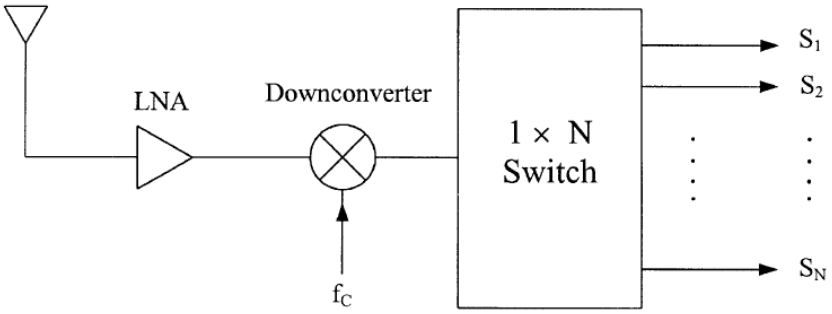


Figure 11: TDMA receiver

Code division multiple access (CDMA):

In FDMA and TDMA, the transmitted signals avoid interfering with each other in either frequency domain or the time domain. The signals are orthogonal in one of these domains. A third method of multiple access allows complete overlap of signals in both frequency and time, but employs "orthogonal messages" to avoid interference.

CDMA is a special case of "spread spectrum" (SS) communications, whereby the baseband data of each user is spread over the entire available bandwidth. CDMA is also called "direct-sequence"(DS-SS)communication .

Spread spectrum has the following features and advantages:

1. It improves the interference rejection.

1. Because each user needs a special code to get access to the data stream , it has applications for secure communications and code division multiple access.
2. It has a good antijamming capability.
3. The capacity and spectral efficiency can be increased by the use of spread spectrum techniques . Many users can use the same frequency band with different codes.
4. It has a nice feature of graceful degradation as the number of users increases.
5. Low cost IC components can be used for implementation.

2.3 Basic concepts

2.3.1 Linearity and nonlinearity

All electronic devices are nonlinear. Using linearity in modeling electronic devices is an approximation to simplify the calculations. Linearity and nonlinearity may be responsible for increasing and decreasing the performance of the circuit. In circuit such small signal amplifier the nonlinearity must be minimized as possible for better performance.

Other circuits, as frequency multiplier, would not exist if there is no nonlinearity, here; increasing nonlinearity increases the system performance.

The problem of analyzing and designing nonlinear circuits is usually more complicated than for linear circuits.

2.3.1.1 Linearity:

Linear systems, processes and actions are those in which the output is directly proportional to the input. Linear circuits are defined as those for which the superposition principle holds.

If for input $x_1\ (t)$ and $x_2\ (t)$

$x_1\ (t) \rightarrow y_2\ (t)\ \ ,\ \ x_2(t) \rightarrow y_2\ (t)$

$ax_1(t) + bx_2(t) \rightarrow ay_1(t) + by_2(t)$

For all value of constant of a and b .any system does not satisfy this condition is not satisfied.

2.3.1.2 Nonlinearity:

Non-linearity means that the output is not directly proportional to the input

Nonlinear systems do not obey the rule of additivity. The sum of inputs A and B does not equal the same result as if each of these is input individually and their results summed.

Nonlinearity circuit can be:

i. Weakly nonlinear circuits:

Those which can be described with accepted accuracy by Taylor series expansion of its nonlinear characteristics: ([I/V], [Q/V], or [ϕ/I]).

ii. Strongly nonlinear circuits:

Circuits that do not satisfy the definition of weakly nonlinear circuits, require time-domain analysis or harmonic balance analysis.

iii. Quasi linear circuit:

A weakly nonlinear circuit is treated for most purposes as linear circuit. Although it may include weak nonlinearities.

Two-terminal nonlinearity:

Resistors, capacitors, and inductors, which are expected to be linear under virtually all conditions, are nonlinear in the extremes of their operating ranges. When large voltages or currents are applied to resistors, for example, heating changes their resistances.

It is a simple nonlinear resistor, capacitor, or inductor whose value is a function of one independent variable, the voltage and current in its terminals are called control voltage and control current.

NONLINEAR PHENOMENA

Nonlinear behavior in radio circuits causes problems such as distortion, crosstalk and desensitization.

1) Harmonic Generation:

Non-linear systems generate harmonic, meaning that if the input of a non-linear system is a signal of a single frequency, $f_a$then the output is a signal which includes a number of integer multiples of the input frequency; (i.e. some of $f_a, 2f_a, 3f_a, 4f_a, \dots\dots$).

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency component that are integer multiples of the frequency.

If $x(t) = A\cos\omega t$, then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2 cos^2\omega t + \alpha_3 A^3 cos^3\omega t$$

$$y(t) = \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}(1+\cos 2\omega t) + \frac{\alpha_3 A^3}{4}(3\cos\omega t + \cos 3\omega t)$$

$$\mathrm{y(t)} = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t.$$

The term with input frequency is called" fundamental frequency"And the higher order term is called "harmonic frequency"

In narrow-band systems, harmonics are not a serious problem because they are far removed in frequency from the signals of interest and inevitably are rejected by filters.

In others, such as transmitters, harmonics may interfere with other communications systems and must be reduced by filters or other means.

2) Intermodulation Distortions:

When two signal with different frequency are applied to nonlinear system ,the output in general exhibit some component that are not harmonic of input frequency this is called intermodulation .this phenomena arises from mixing (muliplication) of two signal when their sum is arises to power greater than unity.

Intermodulation or intermodulation distortion (IMD) is the amplitude modulation of signals containing two or more different frequencies in a system with nonlinearities. The intermodulation between each frequency component will form additional signals at frequencies that are not just at harmonic frequencies (integer multiples) of either, but also at the sum and difference frequencies of the original frequencies and at multiples of those sum and difference frequencies.

Disadvantage of inter modulation:

- IM products generated in an amplifier or communications receiver often present a serious problem, because they represent spurious signals that interfere with, and can be mistaken for, desired signals.
- IM products are generally much weaker than the signals that generate them; however, a situation often arises where in two or more very strong signals, which may be outside the receiver's pass band, generate an IM product that is within the receiver's pass band and obscures a weak, desired signal Inter modulation is a major concern in microwave systems.

Intermodulation is rarely desirable in radio or audio processing, as it creates unwanted spurious emissions, often in the form of sidebands. For radio transmissions this increases the occupied bandwidth, leading to adjacent channel interference, which can reduce audio clarity or increase spectrum usage.

Causes of intermodulation:

- A linear system cannot produce intermodulation.

Intermodulation occurs when the input to a non-linear system is composed of two or more frequencies. Consider an input signal that contains three frequency components at f_a, f_b, and f_c; which may be expressed as

$$x(t) = M_a \sin(2\pi f_a t + \phi_a) + M_b \sin(2\pi f_b t + \phi_b) + M_c \sin(2\pi f_c t + \phi_c)$$

Where the M and ϕ are the amplitudes and phases of the three components, respectively.

We obtain our output signal, y(t) , by passing our input through a non-linear function:

$$y(t) = G(x(t))$$

Y(t) Will contain the three frequencies of the input signal, f_a,f_b , and f_c (which are known as the *fundamental* frequencies), as well as a number of linear combinations of the fundamental frequencies, each of the form

$$k_a f_a + k_b f_b + k_c f_c$$

Where k_a, k_b, k_c are arbitrary integers which can assume positive or negative values. These are the **intermodulation products** (or **IMPs**).

In general, each of these frequency components will have a different amplitude and phase, which depends on the specific non-linear function being used, and also on the amplitudes and phases of the original input components.

More generally, given an input signal containing an arbitrary number N of frequency components $f_a, f_b, \ldots, f_N$, the output signal will contain a number of frequency components, each of which may be described by

$$k_a f_a + k_b f_b + \cdots + k_N f_N$$

Where the coefficients k_a, k_b …etc. are arbitrary integer values.

Cross modulation:

Other phenomena that occur when a weak signal and strong signal and strong interfere pass through a nonlinear system is the transfer of modulation (on noise) on the amplitude of interfere to amplitude of weak signal called cross modulation.

Saturation and Desensitization

Saturation occurs in all circuits because the available output power is finite. If a circuit such as an amplifier is excited by a large and a small signal and the large signal drives the circuit into saturation, gain is decreased for the weak signal as well.

Saturation causes a decrease in system sensitivity, called *desensitization*.

2.3.2 S-Parameters:

Scatter parameters or S-Parameters are two port parameters used in two port theory. They relate to the travelling waves that are scattered or reflected when a network is inserted into a transmission line of certain characteristic impedance.

S-Parameters are important in microwave design because they are easier to measure and to work with in high frequencies than any other kind of two port parameters. They are conceptually simple, analytically convenient, and capable to provide detailed insight into a measurements and modeling problem.

S-Parameters represent the linear behavior of the two-port.

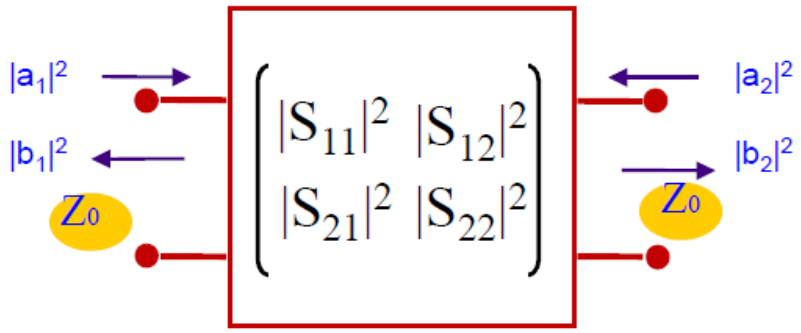


Figure 12: S-Parameters in two-port network

$|a_1|^2$: power travelling towards port 1, $|a_2|^2$: power travelling towards port 2.

$|b_1|^2$: Power reflected from port 1, $|b_2|^2$: Power reflected from port 2.

$$P = V * I \rightarrow P = V * \frac{V}{Z_0} \rightarrow \sqrt{P} = \frac{V}{\sqrt{Z_0}} = I * \sqrt{Z_0}$$

We can convert the power towards the two-port into normalized voltage amplitude of:

$$\therefore a_1 = \frac{V_{Towards\ port\ 1}}{\sqrt{Z_0}}, a_2 = \frac{V_{Towards\ port\ 2}}{\sqrt{Z_0}}$$

And we can convert the power away of the two-port into normalized voltage too:

$$\therefore b_1 = \frac{V_{away\ from\ port\ 1}}{\sqrt{Z_0}}, b_2 = \frac{V_{away\ from\ port\ 2}}{\sqrt{Z_0}}$$

2.3. Determining the values for S-Parameters:

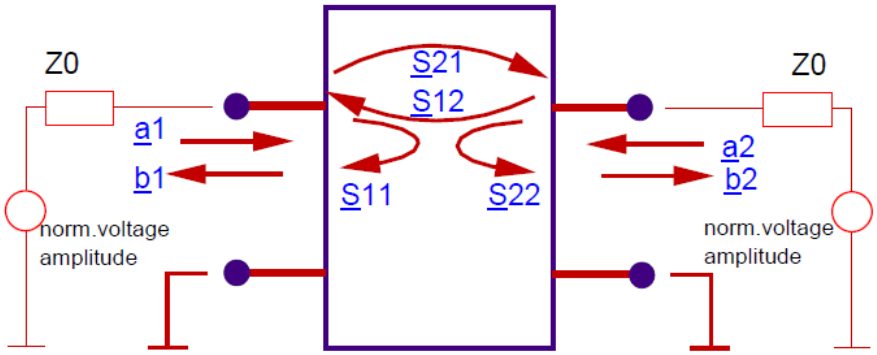


Figure 13: Elements of S-Parameters.

$S11 = \left(\frac{b1}{a1}\right)_{a2=0} = \left(\frac{V_{reflected\ at\ port\ 1}}{V_{towards\ port\ 1}}\right)_{a2=0}$ Representing input matching.

,$S12 = \left(\frac{b1}{a2}\right)_{a1=0} = \left(\frac{V_{out\ of\ port\ 1}}{V_{towards\ port\ 2}}\right)_{a1=0}$ Representing forward gain.

$S21 = \left(\frac{b2}{a1}\right)_{a2=0} = \left(\frac{V_{reflected\ at\ port\ 2}}{V_{towards\ port\ 1}}\right)_{a2=0}$ Representing reverse gain.

$S22 = \left(\frac{b2}{a2}\right)_{a1=0} = \left(\frac{V_{reflected\ at\ port\ 2}}{V_{towards\ port\ 2}}\right)_{a1=0}$ Representing output matching.

Stability with S-Parameters:

The tendency of a transistor toward oscillation can be gauged by its S-parameter data. The calculation can be made even before an amplifier is built and, thus, it serves as a useful tool in finding a suitable transistor for the application.

To calculate the stability of a transistor with S parameters, we must first calculate the intermediate quantity D_S:

$$\boldsymbol{\Delta = S_{11}S_{22} - S_{21}S_{12}}$$

The Rollett Stability Factor (K) is then calculated as:

$$\boldsymbol{K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}}$$

If K is greater than 1, then the device will be unconditionally stable for any combination of source and load impedance. If, on the other hand, K calculates to be less than 1, the device is potentially unstable and will most likely oscillate with certain combinations of source and load

impedance. With *K* less than 1, we must be extremely careful in choosing source and load impedances for the transistor. It does not mean that the transistor cannot be used for the application; it merely indicates that the transistor will be more difficult to use.

2.3.3 STABILITY

The fundamental definition of a stable electrical network is that its response is bounded when the excitation is bounded. In the case of a linear two-port having a sinusoidal steady-state excitation, this definition leads to a stability criterion: the network's poles must all be in the left half of the complex plane.

A stable linear network can be made unstable through an unfortunate choice of source or load impedance. The situation is more complicated in the case of nonlinear circuits because the kinds of interactions that can occur in nonlinear circuits are more complex than in linear ones.

The main way of determining the stability of a device is to calculate the Rollett's stability factor (K), which is calculated using a set of S-parameters for the device at the frequency of operation. The calculations are long winded and it is much quicker to simulate under ADS.

The conditions of stability at a given frequency are $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$, and must hold for all possible values Γ_L & Γ_S obtained using passive matching circuits. We can calculate two Stability parameters K & $|\Delta|$ to give us an indication to whether a device is likely to oscillate or not or whether it is conditionally/unconditionally stable.

The parameters must satisfy $K > 1$ and $|\Delta| < 1$ for a transistor to be unconditionally stable. Once we have calculated the K factor and find the device to be unconditionally stable we can calculate the Maximum available gain (MAG):

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|}.(K - \sqrt{K^2 - 1})$$

Where K is on the limit of unity the above equation reduces down to:-

$$G_{MAX}=|S_{21}|/|S_{12}|$$

Now that it is known that the transistor is conditionally stable it is now necessary to calculate and plot the corresponding stability circles on a Smith chart so that the no-go areas for matches can be highlighted.

The equations for calculation of the stability circles are:

$$r_{s1}=C_1^*/(|S_{11}|^2-|\Delta|^2)$$

This gives the location of the center of the input stability circle

Where $C_1=S_{11}-\Delta.S_{22}$ Note *denotes complex conjugate

$\mathbf{p_{s1}=|(S_{12}.S_{21})/(|S_{11}{}^2-|\Delta|^2)|}$ This gives the radius of the input stability circle .

Similarly for the output

$r_{s2}=C_2*/(|S_{22}|^2-|\Delta|^2)$ This gives the location of the Centre of the output stability circle

Where $C_2=S_{22}-\Delta.S_{11}$ Note *denotes complex conjugate

$p_{s2}=|(S_{12}.S_{21})/(|S_{22}{}^2-|\Delta|^2)|$ This gives the radius of the input stability circle .

2.3.4 Noise:

Noise is a random process that limits the minimum signal level that the circuit can process with acceptable quality. It is one of the trade-offs in today's analog design.

The receiver encounters two types of noise: the noise picked up by the antenna and the noise generated by the receiver. The receiver adds noise to the signal from its amplifiers, filters, mixer and detector stages. Signal to noise ratio SNR measures the quality of the output signal from the receiver.

$$SNR = \frac{Wanted\ Signal\ Power}{Unwanted\ noise\ Power}$$

2.3.4.1 Thermal noise:

This noise is caused by the random fluctuations produced by the thermal agitation of the bound charges. The RMS value of the thermal resistance noise voltage of V_n over a frequency range B is given by:

$$V_n^2 = 4kTBR$$

Where k= Boltzmann constant.

T=absolute temperature. K

B=bandwidth Hz

R= Resistance. Ohm

It is also called white noise due to the distribution of the noise power everywhere in frequency regardless the center frequency.

2.3.4.2 Shot noise:

The fluctuations in the number of electrons emitted from the source constitute the shot noise. Shot noise occurs in tubes or solid-state devices.

2.3.4.3 Flicker, or 1/f, Noise:

A large number of physical phenomena, such as mobility fluctuations, electromagnetic radiation, and quantum noise, exhibit a noise power that varies inversely with frequency. The 1=f noise is important from 1 Hz to 1 MHz, Beyond 1 MHz, the thermal noise is more noticeable.

Receiver noise figure:

Noise figure is a figure of merit quantitatively specifying how noisy a component or system is. The noise figure of a system depends on a number of factors such as losses in the circuit, the solid-state devices, bias applied, and amplification. The noise factor of a two-port network is defined as:

$$F = \frac{SNR\ at\ input}{SNR\ at\ output} = \frac{S_i/N_i}{S_o/N_o}$$

But, using the gain definition for the two port network,

$$S_o = GS_i$$

Note that output noise power equals the gain times the input noise plus the noise generated inside the system, hence:

$$N_o = GN_i + N_n$$

$$\therefore F = \frac{N_0}{GN_i} = 1 + \frac{N_n}{GN_i}$$

And, output noise is given by:

$$N_o = FGN_i$$

Noise figure equals the noise factor in decibel.

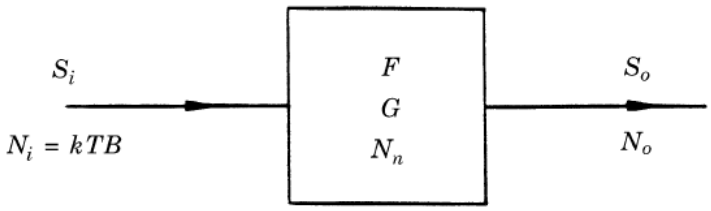


Figure 14: Two-port network with gain G and added noise power Nn

Since the noise figure should be independent of the input noise, we use a standard input noise N_i at room temperature where,

$$N_i = kTB \quad [W]$$

Where T= T_o= 290 K, hence:

$$F = \frac{N_o}{GKTB}$$

For a cascaded circuit with n stages, overall noise factor can be calculated as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots$$

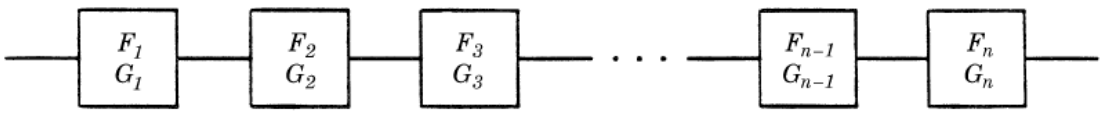


Figure 15: Cascade circuit with n stages

The overall noise figure depends mainly on the low noise, high gain first stage which leads to minimum noise figure.

2.3.5 Impedance Matching

Impedance matching is a major problem in high frequency circuit design. It is concerned with matching one part of a circuit to another in order to achieve *maximum power transfer* between the two parts.

For DC circuits, maximum power will be transferred from a source to its load if the *load resistance* equals the *source resistance.*

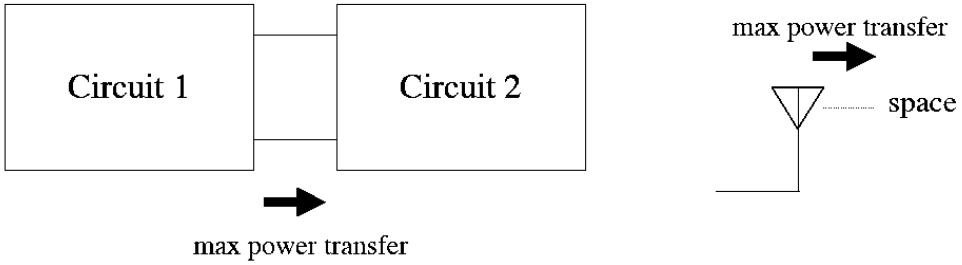


Figure 16: impedance matching

The first Impedance Matching concept in RF domain was related to antenna matching, designing an antenna can be seen as matching the free space to a transmitter or receiver.

The main purpose of Impedance Matching is to match two different terminations (R_{source} and R_{Load}) through a specific pass-band, without having control over stop-band frequencies.

The main role in any Impedance Matching scheme is to force a load impedance to "look like" the complex conjugate of the source impedance, and maximum power can be transferred to the load.

2.3.5.1 What Constitutes a Good Match?

In many situations, a good match is defined arbitrarily as having SWR<1.5. Recall that

$$\mathbf{SWR} = \frac{\mathbf{1}+|\mathbf{\Gamma}|}{\mathbf{1}-|\mathbf{\Gamma}|}, \qquad \text{so,}$$

$$|\boldsymbol{\Gamma}| = \frac{\mathbf{SWR}-\mathbf{1}}{\mathbf{SWR}+\mathbf{1}}$$

Since the reflected power is $|\Gamma|^2$, we can express the so-called return loss as

$$\mathbf{RL} = -\mathbf{10log}|\mathbf{\Gamma}|^{\mathbf{2}} = -\mathbf{20log}|\mathbf{\Gamma}|\mathbf{dB}$$

VSWR (voltage standing wave ratio) is a measure of mismatch from the point of voltage reflection.

$$\mathbf{\Gamma} = \frac{\mathbf{Z_l}-\mathbf{Z_o}}{\mathbf{Z_l}+\mathbf{Z_o}}$$

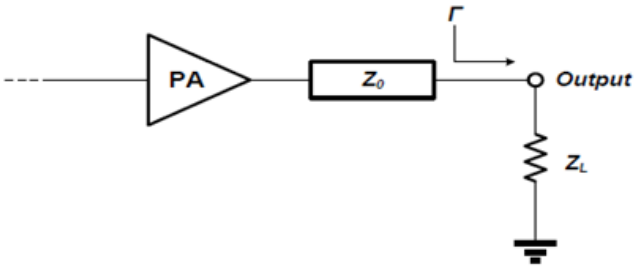


Figure 17: reflection at output node

$$|\Gamma| = \frac{\text{VSWR} - 1}{\text{VSWR} + 1}$$

$$\Gamma = \left|\frac{\text{VSWR} - 1}{\text{VSWR} + 1}\right| e^{j\theta}$$

$$Z_l = \left[\frac{1 + \frac{\text{VSWR} - 1}{\text{VSWR} + 1}}{1 - \frac{\text{VSWR} - 1}{\text{VSWR} + 1}}\right] . Z_O$$

Where θ represents the phase of Γ, and φ is the angle of VSWR.

And the transmitted power to the load, relative to the incident wave power, is

$$\boldsymbol{TL = -10log(1 - |\Gamma|^2)dB}$$

Γ = − 1: maximum negative reflection, when the line is short-circuited,

Γ = 0 : no reflection, when the line is perfectly matched,

Γ = + 1: maximum positive reflection, when the line is open-circuited.

2.3.5.2 Return loss:

Return loss or Reflection loss is the reflection of signal power resulting from the insertion of a device in a transmission line or optical fiber.

If the power transmitted by the source is *PT* and the power reflected is *PR*, then the return loss in dB is given by

$$\mathbf{RL(dB) = 10log_{10}\frac{P_T}{P_R}}$$

Given a load *R*, find a circuit that can match the driving resistance R´ at frequency ω_0.

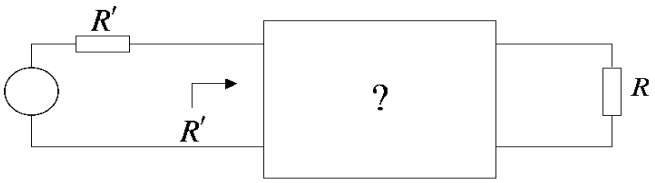


Figure 18: matching circuit

Obviously, the matching circuit must contain L and C in order to specify the matching frequency.

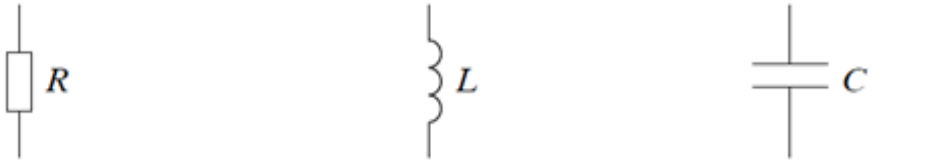
2.3.5.3 Simple matching circuits:

1-L matching circuit (single LC section).

2- π matching circuit.

3-T matching circuit.

From our study:



Resistance (Ω) inductance (H) capacitance (F)

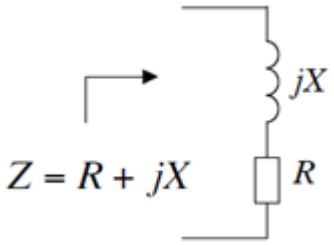
Z	R	$j\omega L = +jX$	$\frac{1}{j\omega C} = -jX$
Impedance	Resistance (Ω)	reactance(Ω) (Ω)	reactance(Ω)
Y	G	$\frac{1}{j\omega L} = +jX$	$j\omega c = +jB$
Admittance	conductance(S)	susceptance(S) (S)	susceptance(S)

2.3.5.4 Quality factor (Q factor):

1) Series:

$$Q = \frac{X}{R} = \frac{1}{RB} = \frac{G}{B}$$

$$Q = \frac{\omega L}{R} \qquad Q = \frac{1}{\omega CR}$$

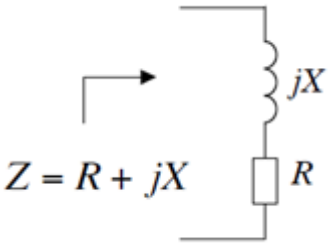


2) Parallel:

$$Q = \frac{R}{X} = RB = \frac{B}{G}$$

$$Q = \frac{R}{\omega L} \qquad Q = \omega RC$$

Series to parallel conversion:

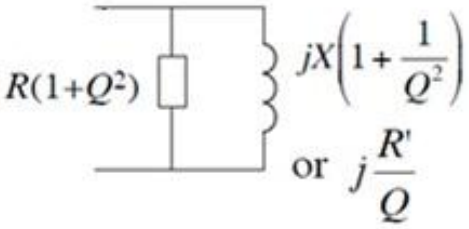


$$\mathbf{Y = \frac{1}{Z} = \frac{1}{R + jX} = \frac{R - jX}{R^2 + X^2}}$$

$$\mathbf{= \frac{R}{R^2 + X^2} - j\frac{X}{R^2 + X^2}}$$

$$\mathbf{= \frac{\frac{1}{R}}{1+\left(\frac{X}{R}\right)^2} + \frac{\frac{1}{X}}{j\left(\left(\frac{R}{X}\right)^2+1\right)}}$$

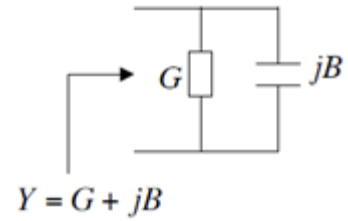
$$\mathbf{= \frac{1}{R(1+Q^2)} + \frac{1}{jX\left(1+\frac{1}{Q^2}\right)}}$$



$$\mathbf{j\frac{R}{Q}(1 + Q^2) = jRQ\left(\frac{1}{Q^2} + 1\right)}$$

Figure 19: series to parallel conversion

Parallel to series conversion:



$$\mathbf{Z = \frac{1}{Y} = \frac{1}{G+jB} = \frac{G-jB}{G^2+B^2}}$$

$$\mathbf{= \frac{G}{G^2+B^2} - j\frac{B}{G^2+B^2}}$$

$$\mathbf{= \frac{\frac{1}{G}}{1+\left(\frac{B}{G}\right)^2} + \frac{\frac{1}{B}}{j\left(\left(\frac{G}{B}\right)^2+1\right)}}$$

$$\mathbf{= \frac{1}{G(1+Q^2)} + \frac{1}{jB\left(\frac{1}{Q^2}+1\right)}}$$

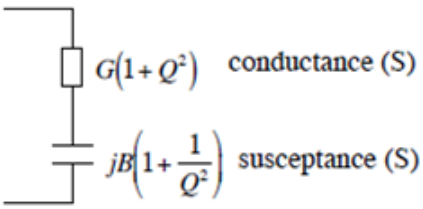


Figure 20: parallel to series conversion

Resonant frequency is $\omega_O = \frac{1}{\sqrt{LC}}$, quality factor Z drops by $\sqrt{2}\ (3dB) at\ \omega_1\ and\ \omega_2$.

$$\omega_{1,2} = (\omega_O)\sqrt{1 + \frac{1}{4Q^2} \pm \frac{1}{2Q}}$$

Bandwidth is $\Delta\omega = \omega_2 - \omega_1 = \frac{1}{RC}$

ω_1, ω_2 re called 3dB corner frequencies . their geometric mean is ω_o.

For narrowband cases, their arithmetic mean is close to ω_o

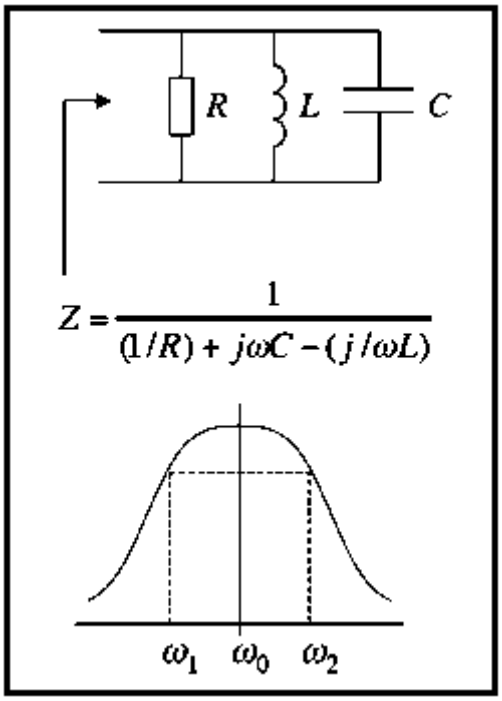
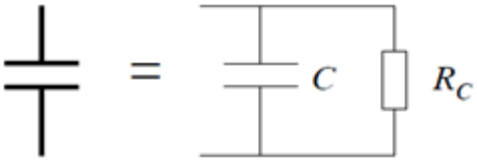
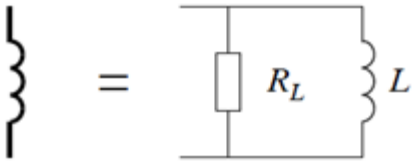


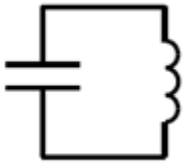
Figure 21 :RLC circuit



Q factor=$Q_c = \omega_O C R_c$ (unloaded Q factor).



Q factor=$Q_L = R_L/\omega_O L$ (unloaded Q factor).



Q_LC unloaded Q factor for the paralleled LC components

$$\frac{1}{Q_{LC}} = \frac{1}{Q_C} + \frac{1}{Q_L}$$

2.3.5.5 Design of *L* matching circuits

Series L matching:

The objective is to match Y_{in} to R' at ω_o, begin with

$$Y_{in} = j\omega C + \frac{1}{R + j\omega L}$$

$$Y_{in} = \frac{R}{R^2 + (\omega L)^2} + j\left[\omega C - \frac{\omega L}{R^2 + (\omega L)^2}\right]$$

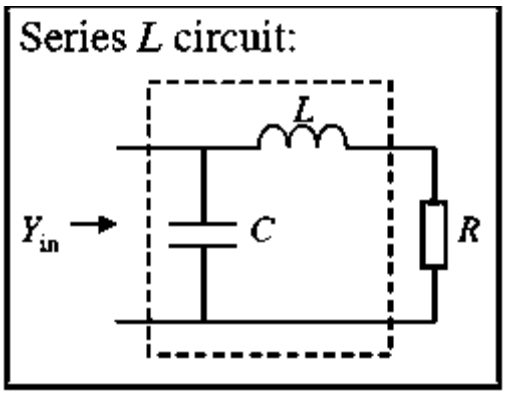


Figure 22: L matching circuit

Obviously, the reactive part is cancelled if we have

$$\frac{L}{R^2+\omega_o^2L^2} \quad where\ \omega_o = \sqrt{\frac{1}{LC}-\frac{R^2}{L^2}} \qquad (\#)$$

Thus, at w=w_o we have a resistance for Y_{in} , which should be set to R´.

$$R' = \frac{R+\omega_0^2 L}{R} = R(1+Q^2) \qquad (*)$$

Here, Q is the Q-factor, which is equal to ω_oL/R (for series L and R)

So, we can see clearly that Q is modifying R to achieve the matching condition.

Design procedure:

-Given R and R´, find required Q from (*).

-Given ω_o ,find the required L from Q= ω_oL/R.

-From (#), find the required C to give the selected resonant frequency ω_o.

Shunt L circuit.

$$Z_{in} = j\omega L + \frac{1}{G+j\omega C}$$

$$= \frac{G}{G^2+\omega^2C^2} + j\left[\omega L - \frac{\omega C}{G^2+\omega^2C^2}\right]$$

Reactive part is cancelled when:

$$\mathbf{L} = \frac{\mathbf{C}}{\mathbf{G^2} + \boldsymbol{\omega}_\mathbf{o}^\mathbf{2}\mathbf{C^2}} \quad \textbf{where } \boldsymbol{\omega}_\mathbf{o} = \sqrt{\frac{\mathbf{1}}{\mathbf{LC}} - \frac{\mathbf{G^2}}{\mathbf{C^2}}} \quad (\#)$$

Finally, the matching condition requires that:

$$\mathbf{R}' = \frac{\mathbf{1/G}}{\mathbf{1+(\omega_o C/G)^2}} = \frac{\mathbf{R}}{\mathbf{1+Q^2}}$$

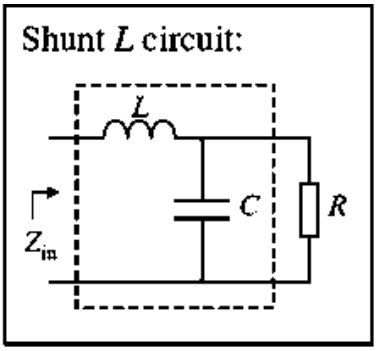


Figure 23: shunt L circuit

Advantages of L circuits:

- Simple.
- Low cost.
- Easy to design.

Disadvantages of L circuits:

- The value of *Q* is determined by the ratio of *R/R'*. Hence,
- There is no control over the value of *Q*.
- The bandwidth is also not controllable.

2.3.5.6 π matching:

Analysis by decomposing into two L circuit sections:

First section (from right):

$$\mathbf{R}' = \frac{\mathbf{R}}{\mathbf{1+Q_1}^2}, \mathbf{X}' = \mathbf{X_2} - \mathbf{R}'\mathbf{Q_1}$$

$$\mathbf{Q_1} = \frac{\mathbf{B_1}}{\mathbf{G}} = \mathbf{B_1 R}$$

Second section:

$$\mathbf{Q_2} = \frac{\mathbf{X}'}{\mathbf{R}'} = \frac{\mathbf{X_2} - \mathbf{R}'\mathbf{Q_1}}{\mathbf{R}'}, \frac{\mathbf{X_2}}{\mathbf{R}'} = \mathbf{Q_1} + \mathbf{Q_2}$$

$$\mathbf{R}'' = \mathbf{R}'\left(\mathbf{1} + \mathbf{Q_2^2}\right)$$

$$\mathbf{B}'' = \mathbf{B_3} - \frac{\mathbf{Q_2}}{\mathbf{R}''}, \mathbf{B_3} = \frac{\mathbf{Q_2}}{\mathbf{R}''}$$

Impedance matching in ρ matching circuits:

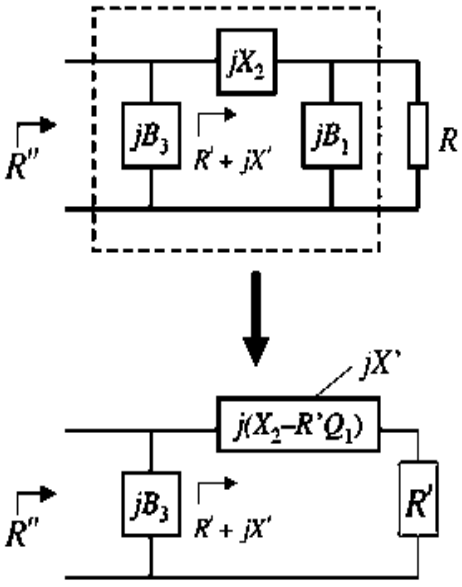


Figure 24: π matching circuit

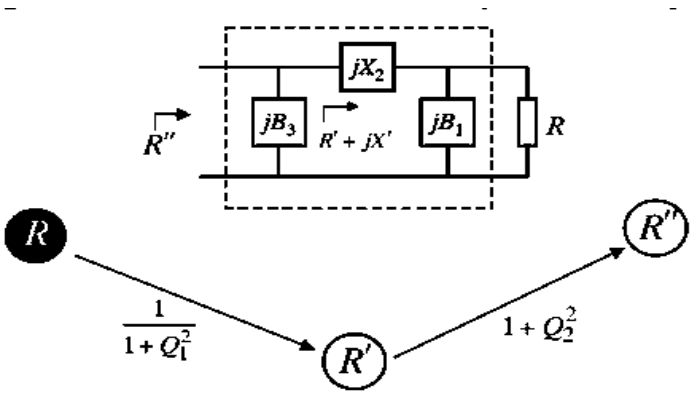


Figure 25: π matching circuit

Obviously we have to set $Q_1 > Q_2$ if we want to have $R'' < R'$.

Likewise, we need $Q_1 < Q_2$ if we want to have $R'' > R'$.

2.3.5.7 T matching circuit:

The analysis is similar to the ρ case.

The difference is that R is first raised to R' by the series reactance, and then lowered to R'' by the shunt reactance.

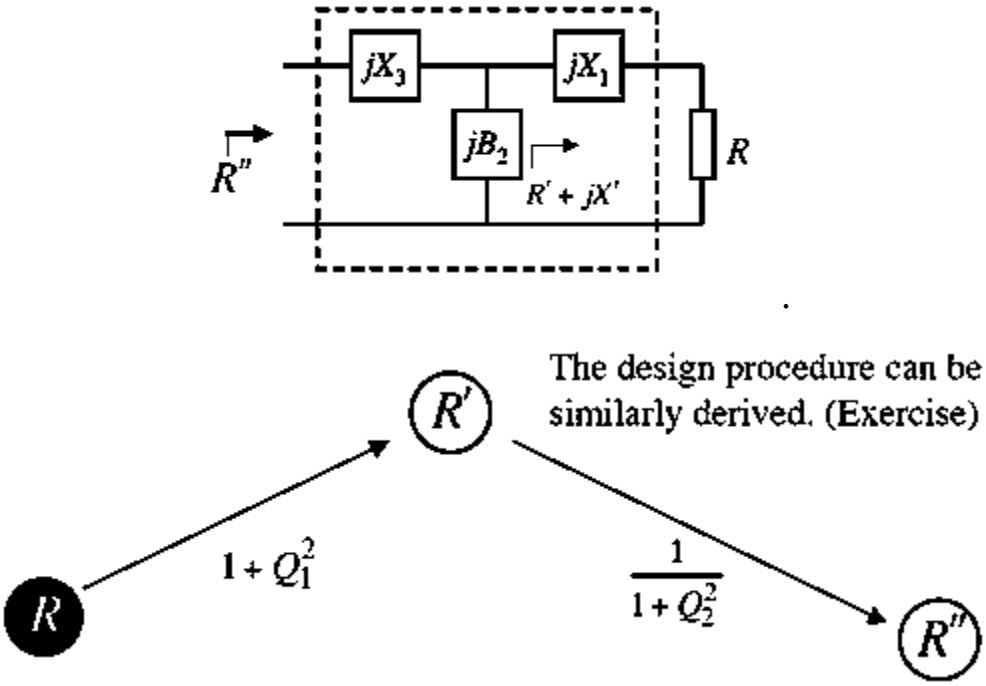


Figure 26: T matching circuit

Advantages of π, T and tapped C circuits:

• specify *Q* factor (sharpness of cutoff).

• provide some control of the bandwidth.

Disadvantage:

• No precise control of the bandwidth.

2.3.6 IC BIASING-CURRENT SOURCES, CURRENT MIRRORS AND CURRENT-STEERING CIRCUITS

Biasing in integrated-circuit design is based on the use of constant-current sources.

On an IC chip with a number of amplifier stages, a constant dc current (called a reference current) is generated at one location and is then replicated at various other locations for biasing the various amplifier stages through a process known as current steering.

This approach has the advantage that the effort expended on generating a predictable and stable reference current, usually utilizing a precision resistor external to the chip, need not be repeated for every amplifier stage. Furthermore, the bias currents of the various stages track each other in case of changes in power-supply voltage or in temperature.

The Basic MOS FET Current Source

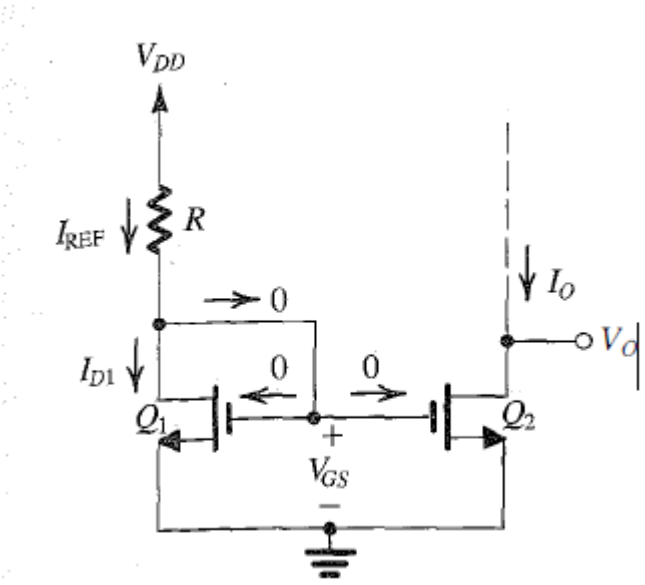


Figure 27: circuit for a basic MOSFET constant- current source

The heart of the circuit is transistor Q1, the drain of which is shorted to its gate, thereby forcing it to operate in the saturation mode with

$k_n'=\mu C_{ox}$

$I_{D1}=0.5kn'(W/L)_1(V_{GS}-V_{th})^2$ (equ1)

We have neglected channel-length modulation. The drain current of Q_l is supplied by VDD through resistor R, which in most cases would be outside the IC chip. Since the gate currents are zero,

ID1=IREF= (VDD-VGS)/R (equ2)

Where the current through R is considered to be the reference current of the current source and is I_{REF}• Equations (1) and (2) can be used to determine the value required for R.

Now consider transistor Q_2: It has the same VGS as Ql; thus, if we assume that it is operating in saturation, its drain current, which is the output current I0 of the current source, will be

$Io=I_{D2}=0.5k_n'(W/L)_2(V_{GS}-V_{th})^2$ (equ3)

Here, we have neglected channel-length modulation. Equations (1) and (3) enable us to relate the output current I0 to the reference current IREF as follows:

$I_o/I_{REF}=(W/L)_2/(W/L)_1$ (equ4)

This is a simple and attractive relationship: The special connection of Q_l and Q_2 provides an output current I_0 that is related to the reference current I_{REF} by the ratio of the aspect ratios of the transistors. In other words, the relationship between I_0 and I_{REF} is solely determined by the geometries of the transistors. In the special case of identical transistors, I0 $=I_{REF}'$ and the circuit simply replicates or mirrors the reference current in the output terminal.

This has given the circuit composed of Ql and Q2 the name current mirror, a name that is used irrespective of the ratio of device dimensions.

Figure 2 depicts the current mirror circuit with the input reference current shown as being supplied by a current source for both simplicity and generality. The current gain or current transfer ratio of the current mirror is given by Eq.4

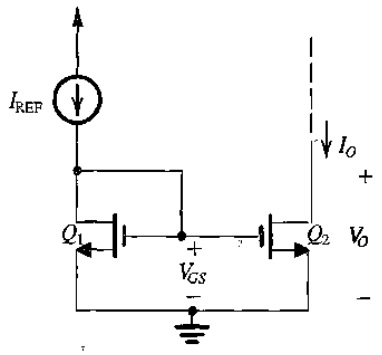


Figure 28: Basic MOSFET current mirror

Effect of V_o on I_0 In the description above for the operation of the current source of Figure 27.

we assumed Q2 to be operating in saturation. This is obviously essential if Q2 is to supply a constant-current output. To ensure that Q2 is saturated, the circuit to which the drain of Q2 is to be connected must establish a drain voltage **V0** that satisfies the relationship **V**o **≥ V**GS-**V**th

or, equivalently, in terms of the overdrive voltage Vov of **QI** and **Q2 V**o**≥ V**ov In other words, the current source will operate properly with an output voltage **V 0** as low as **Vov**, which is a few tenths of a volt.

Although thus far neglected, channel-length modulation can have a significant effect on the operation of the current source. Consider, for simplicity, the case of identical devices **Q1** and **Q2**. The drain current of **Q2**, **I0**, will equal the current in Q1, $\mathbf{l}_{REF}$, at the value of **Vo** that causes the two devices to have the same **VDS**, that is, at **Vo** = $\mathbf{V_{GS}}$. As $\mathbf{V_o}$ is increased above this value, **I0** will increase according to the incremental output resistance $\mathbf{r_{o2}}$ of $\mathbf{Q_2}$**.** This is illustrated in Figure 29, which shows $\mathbf{I_0}$ versus $\mathbf{V_o}$. Observe that since **Q2** is operating at a constant **VGS** (determined by passing $\mathbf{l_{REF}}$ through the matched device **QI**), the curve in Figure 29 is simply the $\mathbf{I_D}$-$\mathbf{V_{DS}}$ characteristic curve of **Q2** for VGS equal to the particular value **VGS**. In summary, the current source of Figure 27 and the current mirror of Figure 28 have a finite output resistance Ro

$$Ro=\Delta Vo/\Delta Io=ro2=V_{A2}/Io$$

Where lo is given by Eq. (6.6) and VA2 is the Early voltage of Q2. Also, recall that for a given process technology, VA is proportional to the transistor channel length; thus, to obtain high output-resistance values, current sources are usually designed using transistors with relatively long channels. Finally, note that we can express the current I_0 as

$$I_o= [(W/L)_2/(W/L)1]*I_{REF} (1+((Vo-V_{GS})/V_{A2})$$

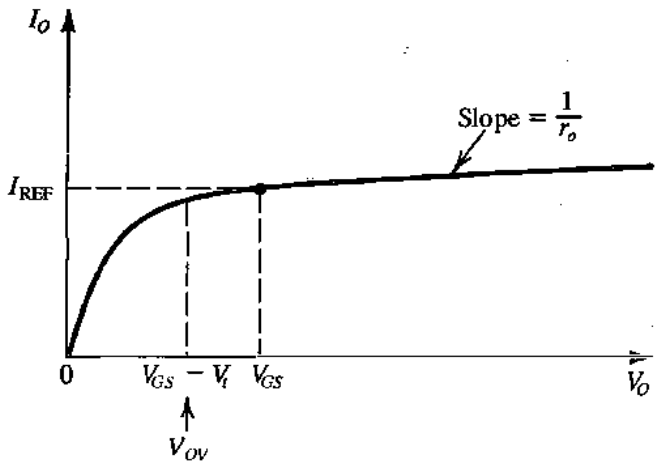


Figure 29: Output characteristic of the current source in figure 1and the current mirror of figure2for the case Q_2 is matched to Q_1.

MOS Current-Steering Circuits

As mentioned earlier, once a constant current is generated, it can be replicated to provide dc bias currents for the various amplifier stages in an IC. Current mirrors can obviously be used to implement this current-steering function. Figure 30 shows a simple current-steering circuit.

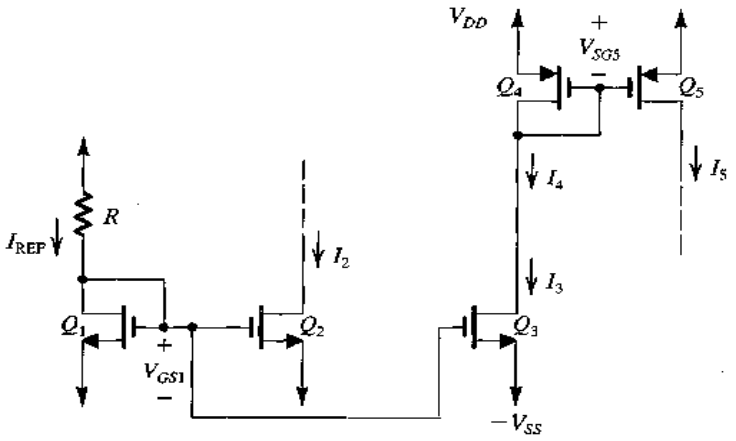


Figure 30: current steering circuit

Here Ql together with R determine the reference current IREF. Transistors Ql' ,Q2' and Q3 form a two-output current mirror,

$I2=I_{REF}*((W/L)_2/(W/L)_1)$

$I_3=I_{REF}*((W/L)_3/(W/L)_1)$

To ensure operation in the saturation region, the voltages at the drains of Q2 and Q3 are constrained as follows:

$V_{D2}, V_{D3} \geq -V_{ss}+V_{GS1}-V_{th}$

Or, equivalently,

$V_{D2}, V_{D3} \geq -V_{ss}+V_{ov1}$

Where V_{OVl} is the overdrive voltage at which Ql' Q2' and Q3 are operating. In other words, the drains of Q2 and Q3 will have to remain higher than -Vss by at least the overdrive voltage, which is usually a few tenths of a volt.

Continuing our discussion of the circuit in Figure 31, we see that current I3 is fed to the input side of a current mirror formed by PMOS transistors Q4 and Q5 . This mirror provides $I_5=I_4*((W/L)_5/(W/L)_4)$

Where I4=I3.To keep Q5 in saturation, its drain voltage should be

$V_{D5} \leq V_{DD}-|V_{ov5}|$

Where V_{ov5} is the overdrive voltage at which Q_5 is operating.

2.3.7 Chip inductors

Chip inductors are a type of inductor that is made from semi-conductor material. There are on –chip inductor and off- chip inductor. On-chip inductors are those integrated within the chip. Usually these on chip inductors consume a very large portion of chip area, usually in the range of nH. Off-chip inductors are those outside the chip.

Simulation of on-chip inductors saves lots of time and good enough for optimization only small final correction are necessary. On chip inductor are usually realized using Bond-wires or on-chip spirals.

Although bound wires exhibit higher quality factors (Q) than on chip spirals, spiral inductors exhibit good matching and are they permit a large range of inductance they possess smaller Q values.

On chip inductor option:

Table 1 : On-chip inductor options

Attribute	Bond wire	Planar spiral
Inductance	0.5-4nH	0.2-100H
Q	30-60	<10
Parasitic	$C_{Bond\text{-}pad}$	R_s, C_{ox}, C_{si}, R_{Si}
Fluctuations	Large	Small

On-chip spiral inductors are widely used due to their low cost and ease of process integration. The spiral shape may be square, Hexagonal, octagonal, circular.

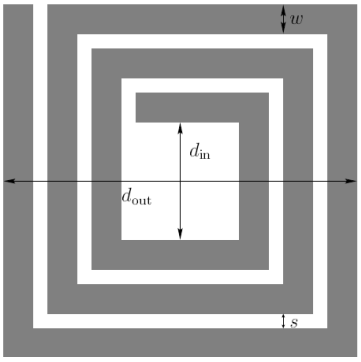


Figure 32 : Square spiral

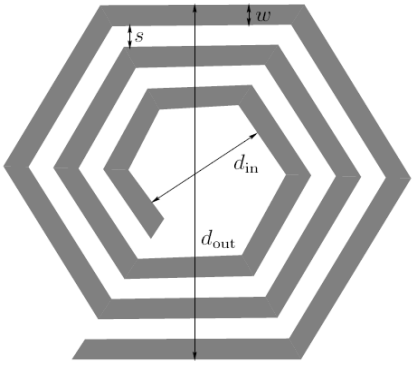


Figure 33: Hexagonal spiral

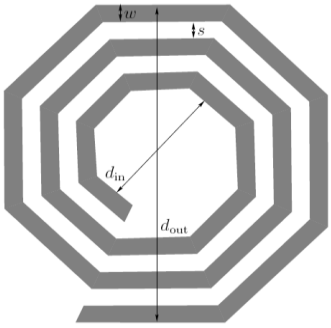


Figure 34: Octagonal spiral

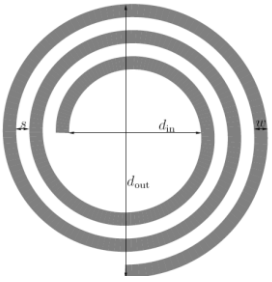


Figure 35: Circulator spiral

Square spirals are popular because of the ease of their layout.

The lateral parameters of a spiral are completely specified by the following:

- Shape: square, hexagonal, octagonal, etc.
- Number of turns, n
- Conductor width, w
- Conductor spacing, s
- d_{out} ,d_{in} , and d_{avg} .

$$d_{avg} = 0.5(d_{out} + d_{in})$$

or

$$P = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$$

d_{out}: is the outer diameter .

d_{in}: the inner diameter.

P: defined as the fill ratio.

The inductance of an on-chip spiral is determined primarily by its lateral dimensions.

On –chip inductor Modeling

- 3-D filed solver
- Segmented models
- Lumped , scalable models
- field solvers

Field solvers:

Solves Maxewell's equation numerically. It is accurate but slow.

field: $E = -j\omega A - \nabla \Phi$

$B = \nabla \times A$

Assumption: Linear and isotropic metal and substrate conductors.

Couloum guage ∇.A=0

$$\nabla^2 A = \mu(j\omega\sigma A - \omega^2 \varepsilon A + (\sigma + j\omega\varepsilon)\nabla\Phi - J)$$

Term# (1) (2) (3) (4)

(1) Magnetically induced eddy current in metal and substrate conductors.

(2) Dynamic radiation current (can be neglected here).

(3) Elestrically induced conductive and displacement current.

(4) Impressed current in the metal conductors.

Segmented circuit model:

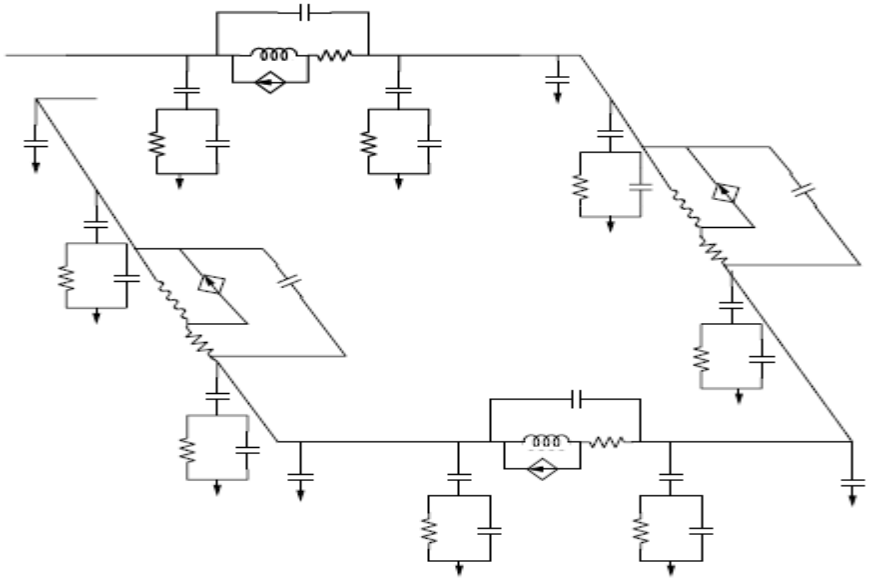


Figure 36: Segment model

Segmented model for one turn of a square spiral. Uses separated lumped π model for each segment of an inductor.

A square inductor with n turns will have 4n segment, each segment with its own lumped model .Each segment contain the conductor's self-inductance, series resistance, a dependent current source.

The number of segments is determined by the product of the number of turns and the number of sides per turn.

The segmented model is simpler than the field solver. however, it is very complicated .

Lumped, scalable model:

The disadvantage of 3-D simulators and segmented models indicate the need for a compact, lumped inductor model with the inductance and series resistance in the series branch and the spiral –to-substrate capacitances and the substrate parasitics in the shunt branches.

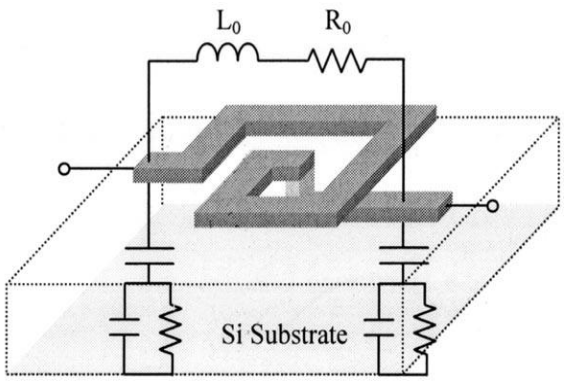


Figure 37: Lumped model.

This model is widely used, but it is not very accurate in high frequency.

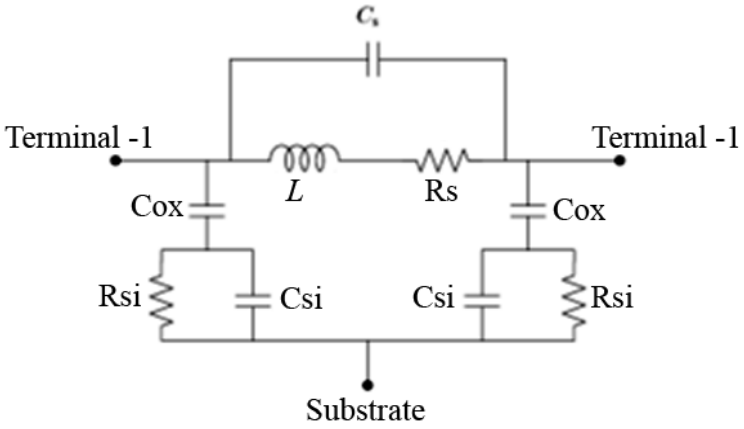


Figure 38: Lumped – element equivalent circuit model of single – layer Spiral inductor.

L: represent the spiral inductance.

R_s: Represent the series resistance.

C_S: is the capacitance between metal lines.

C_{ox}: is capacitive coupling between the spiral and the substrate.

C_{si}: the substrate capacitance

R_{si}: the substrate resistance

R_s : the series resistance of spiral is given by

$$R_s = \frac{l}{2\omega\sigma\delta(1 - e^{-\left(\frac{t}{\delta}\right)})}$$

Where σ is the conductivty , and t is the turn thickness

$\delta = \sqrt{\frac{2}{\omega\mu\sigma}}$ ω is the frequency, $\mu = 4\pi 10^{-7}$ H/ m

$$C_{ox} = \frac{1}{2}.l.w.\frac{\varepsilon_{ox}}{t_{ox}}$$

ε_{ox} =3.45*10^{-13} F/cm, t_{ox} is the oxide thickness between the spiral and the substrate.

$$c_s = n.w^2.\frac{\varepsilon_{ox}}{t_{ox\ M1-M2}}$$

Where $t_{ox,M1\text{-}M2}$ is the oxide thickness between the spiral and the underpass.

C_{si} : The substrate capacitance is given by,

$$\frac{1}{2} . l. w. C_{sub}$$

C_{sub} is the substrate capacitance per unit area.

R_{si} : The substrate resistance can be expressed as,

$$R_{si} = \frac{2}{l. w. G_{sub}}$$

G_{sub} is the substrate conductance per unit area.

Quality Factor

It describes how good an inductor can work as an energy-storage element. In the ideal case, inductance is pure energy-storage element (Q approaches infinity). While in reality, parasitic resistance and capacitance reduce Q. This is because the parasitic resistance consumes stored energy, and the parasitic capacitance reduces inductivity.

For a spiral inductor, it can be calculated by:

$$Q = \omega . \left(\frac{Energy\ stored}{Average\ power\ Dissipated} \right)$$

$$\frac{\omega l_s}{R_s} \times \frac{R_p}{R_p + ((\omega L_s / R_s)^2 + 1). R_s} \times \left(1 - \frac{{R_s}^2 \left(C_p + C_s\right)}{L_s} - \omega^2 L_s \left(C_p + C_s\right)\right)$$

Substrate loss factor self-resonance factor

$$R_p = \frac{1}{\omega^2 {c_{ox}}^2 R_{si}} + \frac{R_{si}(c_{ox} + c_{si})^2}{{c_{ox}}^2}$$

$$c_p = c_{ox} \cdot \frac{1 + \omega^2 \left(c_{ox} + c_{si}\right) c_{si} {R_{si}}^2}{1 + \omega^2 \left(c_{ox} + c_{si}\right)^2 {R_{si}}^2}$$

Inductance (L)

The L value of an inductor is frequency – dependent. The spiral inductor can be configured either in a “grounded” or in a “floating” form in integrated circuits.

When used in a “grounded “form, it operates in one – port mode with the other port grounded.

L is determined by:

$$L = \frac{Im(\frac{1}{Y_{11}})}{2\pi f}$$

Where Y_{11} is the input admittance converted from the measured two – port s-parameters.

When a spiral inductor is used as a two- port device

$$L = \frac{Im(\frac{1}{Y_{21}})}{2\pi f}.$$

Chapter 3:
3.IEEE 802.16 standard

The IEEE 802.16 Working Group is the IEEE group for wireless metropolitan area network.

The IEEE 802.16 standard defines the Wireless MAN (metropolitan area network) air interface specification (officially known as the IEEE Wireless MAN standard). This wireless broadband access standard could supply the missing link for the “last mile” connection in wireless metropolitan area networks.

The IEEE 802.16 designed to operate in the 10-66 GHz spectrum and it specifies the physical layer (PHY) and medium access control layer (MAC) of the air interface BWA systems. At 10-66 GHz range, transmission requires Line-of-Sight (LOS).

IEEE 802.16 is working group number 16 of IEEE 802, specializing in point-to-multipoint broadband wireless access.

The IEEE 802.16 Working Group created a new standard, commonly known as WiMAX, for broadband wireless access at high speed and low cost, which is easy to deploy, and which provides a scalable solution for extension of a fiber-optic backbone. WiMax base stations can offer greater wireless coverage of about 5 miles, with LOS (line of sight) transmission within bandwidth of up to 70 Mbps.

Table 2 : WiMAX standards specifications

Completion Date	802.16 Dec 2001	802.16a/ 802.16REVd 802.16a:Jan 2003 802.16Revd:Q3 2004	802.16e 2005
Spectrum	10 to 66 GHz	< 11GHz	<6GHz
Channel conditions	Line-of-Sight only	Non-Line-of-Sight	Non-Line-of-Sight
Bit Rate	32 to 134 Mbps	75 Mbps max 20-MHz Channelization	15 Mbps max 5-MHz Channelization
Modulation	QPSK 16QAM 64QAM	OFDM 256 subcarriers	Same as 802.16a

		QPSK 16 QAM 64QAM	
Mobility	Fixed	Fixed	Pedestrian mobility Regional roaming
Channel Bandwidths	20,25 and 28 MHz	Selectable between 1.25 and 20 MHz	Same as 802.16a with uplink subchannels
Typical Cell Radius	1 to 3 miles	3 to 5 miles (30 miles max based on tower height, antenna gain, and power transmit)	1 to 3 miles

3.1 IEEE 802.16m standard:

In December 2006 the IEEE launched an effort to further evolve the IEEE 802.16 Wireless MAN-OFDMA specification. This amendment, known as 802.16m, is designed to meet or exceed the requirements of IMT-Advanced (the 4th generation of cellular systems). With a number of stringent requirements for backwards compatibility, the 802.16m amendment will provide the basis for WiMAX System Release 2 and provide existing WiMAX operators a graceful migration path to gain performance enhancements and add new services. The IEEE 802.16m task group has more than 300 participating individuals from approximately 100 organizations from two dozen countries. As was the case for 802.16e-2005, 802.16m is designed to support frequencies in all licensed IMT bands below 6 GHz and include TDD and FDD duplexing schemes as well as half-duplex FDD (H-FDD) terminal operation to ensure applicability to the wide range of worldwide spectrum assignments.

3.1. Features of IEEE 208.16m Standard [2]:

1- Coverage and Spectral Efficiency

The IEEE 802.16m amendment provides an improvement in the link budget over WiMAX System Release 1 of at least 3 dB with the same antenna configuration. This will provide a 20-30% increase in cell coverage area in a typical non line-of-sight environment. Alternatively the improved link budget can be translated to increased cell edge user throughput resulting in a two times improvement over WiMAX System Release 1. Additional coverage benefits with 802.16m will be realized

with support for more advanced antenna systems and with enhanced support for *integrated multi-hop relay and femto-cells*. The latter capabilities provide a cost-effective means to extend cell coverage and fill gaps in coverage caused by obstructions and shadowing.

Several other enhancements included in IEEE 802.16m will improve spectral efficiency for data services. These enhancements include:

- Extended and improved MIMO modes with emphasis on multi-user MIMO (MU-MIMO) on both DL and UL to enable support for up to 8 data streams in the DL and up to 4 data streams in the UL.
- Improved open-loop power and closed-loop control
- Advanced interference mitigation techniques including fractional frequency reuse and inter-base station coordination
- More efficient use of pilot tones with new sub-channelization schemes and a cyclic prefix of 1/16 vs. 1/8 to reduce layer 1 overhead in both DL and UL
- Enhanced control channel design on both DL and UL with;
    - Reduced overhead
    - Improved coverage through power boosting and optimized channel coding
    - HARQ protection for control messages

The net result of these enhancements will provide more than **2 times** improvement in average channel spectral efficiency. The peak and average spectral efficiency performance for IEEE 802.16m is summarized in the following table[2] for a low user mobility scenario.

Table 3: Spectral Efficiency Performance for IEEE 802.16m

Parameter	Antenna Configuration	Performance
Peak DL Spectral Efficiency	(2x2) MIMO (4x4) MIMO	8.5 bps/Hz 17.0 bps/Hz
Average DL Spectral Efficiency	(4x2) MIMO	3.2 bps/Hz 0.32 bps/Hz/User
DL Cell-Edge User Throughput	(4x2) MIMO	0.09 bps/Hz
Peak UL Spectral Efficiency	(1x2) SIMO (2x4) MIMO	4.6 bps/Hz 9.3 bps/Hz
Average UL Spectral Efficiency	(2x4) MIMO	2.6 bps/Hz 0.26 bps/Hz/User
UL Cell-Edge User Throughput	(2x4) MIMO	0.11 bps/Hz/User

2- Increased Capacity for Data and VoIP

Data Capacity: The spectral efficiency enhancements described in the previous section lead directly to increased channel data capacity and increased peak data rates. The following charts provide a summary for the peak DL channel and peak UL channel data rates with a comparison of WiMAX System Release 2, based on IEEE 802.16m, and WiMAX System Release 1, based on IEEE 802.16e-2005 and 802.16e-2009.

In Figure 1, for cases where the mobile station is configured with a (1x2) SIMO antenna configuration, UL collaborative MIMO (CM) is assumed. This enables the output from each of two users with a single transmit antenna to be combined over the same time and frequency resource block to double the UL channel data rate.

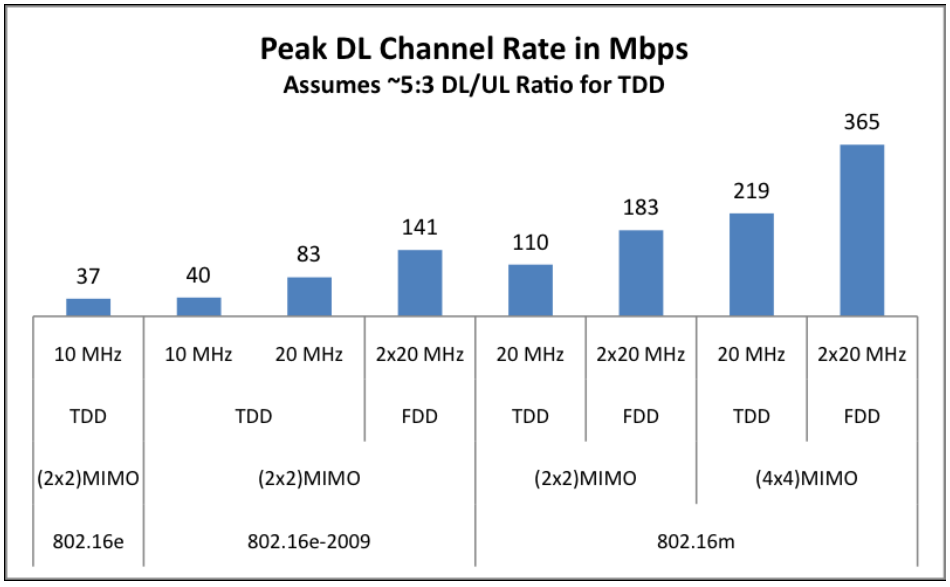


Figure 39: Peak DL Channel Data Rate Summary

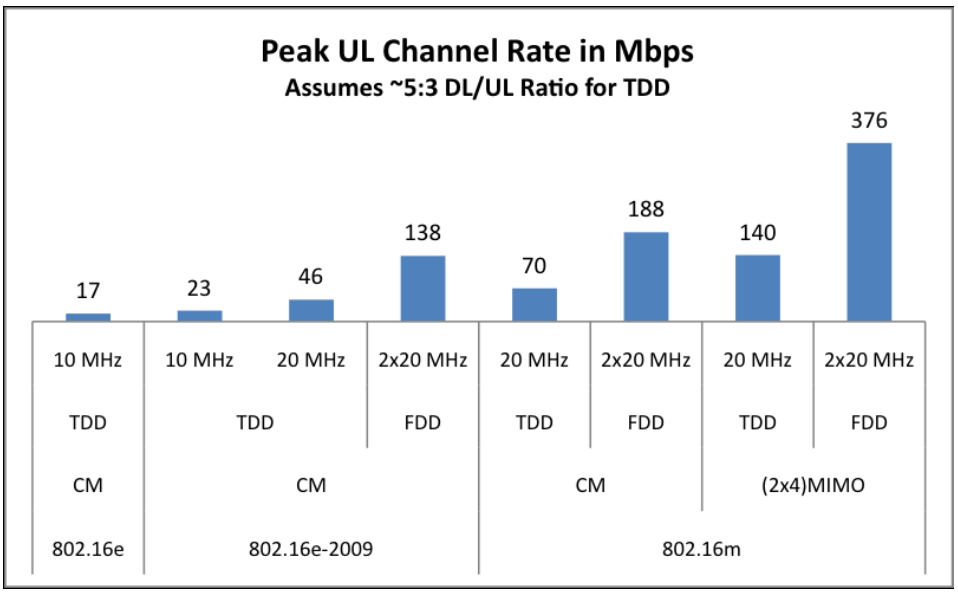


Figure 40: Peak UL Channel Data Rate Summary

3- Multi-Carrier Support:

The IEEE 802.16m amendment also supports channel aggregation of contiguous or non-contiguous channels to provide an effective bandwidth up to 100 MHz. The channels do not need to have the same bandwidth nor do they need to be in the same frequency band. This capability will enable operators with access to multiple channels or licenses to achieve significantly higher peak and average data rates than is achievable with individual channels. Aggregating several 20 MHz channels, for example, could support peak data rates exceeding 1 Gigabit/sec.

4- VoIP Capacity:

With persistent and group scheduling, faster HARQ retransmissions, rate matching, optimized QoS support, and the other spectral efficiency enhancements described in the previous section, VoIP capacity is significantly increased with 802.16m. The following chart summarizes the improvements for VoIP capacity assuming AMR 12.2 kbps speech codec[3] and the Urban Microcell test environment as specified by IMT-Advanced with user mobility of 3 km per hour. With (4x2) MIMO in the DL and (2x4) MIMO in the UL, WiMAX System Release 2 will be able to support 1600 bidirectional VoIP sessions per sector or 4800 sessions per 3-sector cell with an FDD system and a 2x20 MHz channel pair.

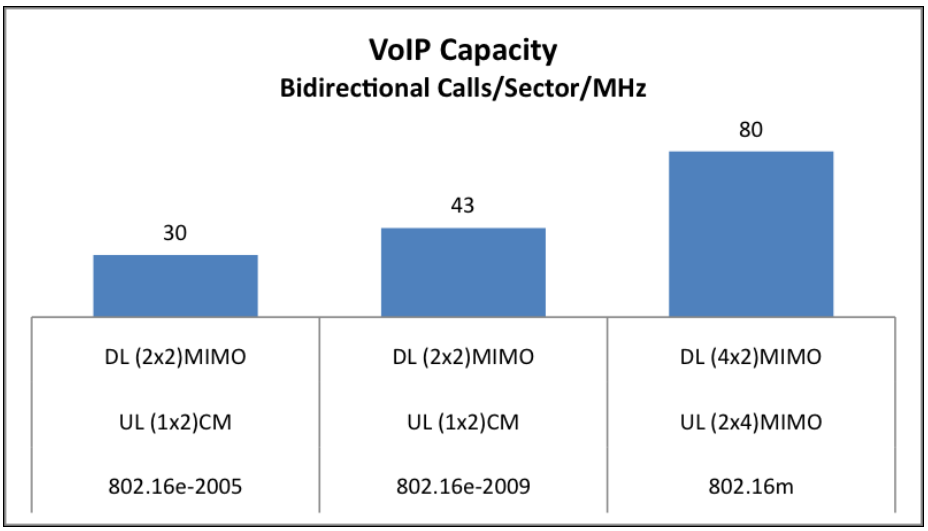


Figure 41: VoIP Capacity

Other features of IEEE 802.16m Standard:

5- Lower Latency and QoS Enhancements
6- Interworking with Other Wireless Networks
7- Power Conservation
8- Self-Organizing Network (SON) features to enable self-configuration and self-optimization.
9- Enhanced security with more advanced encryption schemes

10- Mobility: An IEEE 802.16m mobile station will maintain a connection up to 350 km/hr and in some cases 500 km/hr depending on the operating frequency band.

Chapter-4:
4. Integrated Low Noise Amplifier [LNA]

Low-noise amplifier (**LNA**) is an electronic amplifier used to amplify possibly very weak signals (for example, captured by an antenna). It is usually located very close to the detection device to reduce losses in the feedline. This active antenna arrangement is frequently used in microwave systems like GPS, because coaxial cable feedline is very lossy at microwave frequencies, e.g. a loss of 10% coming from few meters of cable would cause a 10% degradation of the signal-to-noise ratio (SNR).

Using an LNA, the effect of noise from subsequent stages of the receive chain is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system. A good LNA has a low NF (like 1 dB), a large enough gain (like 20 dB) and should have large enough intermodulation and compression point (IP3 and P1dB). Further criteria are operating bandwidth, gain flatness, stability and input and output voltage standing wave ratio (VSWR).

4.1. Specifications:

The most important specifications of LNA are:

1- Noise figure as high as possible [$NF=SNR_{out}/SNR_{in}$].
2- High gain with linearity.
3- IIP3.
4- Less power consumption.

4.2. Structure:

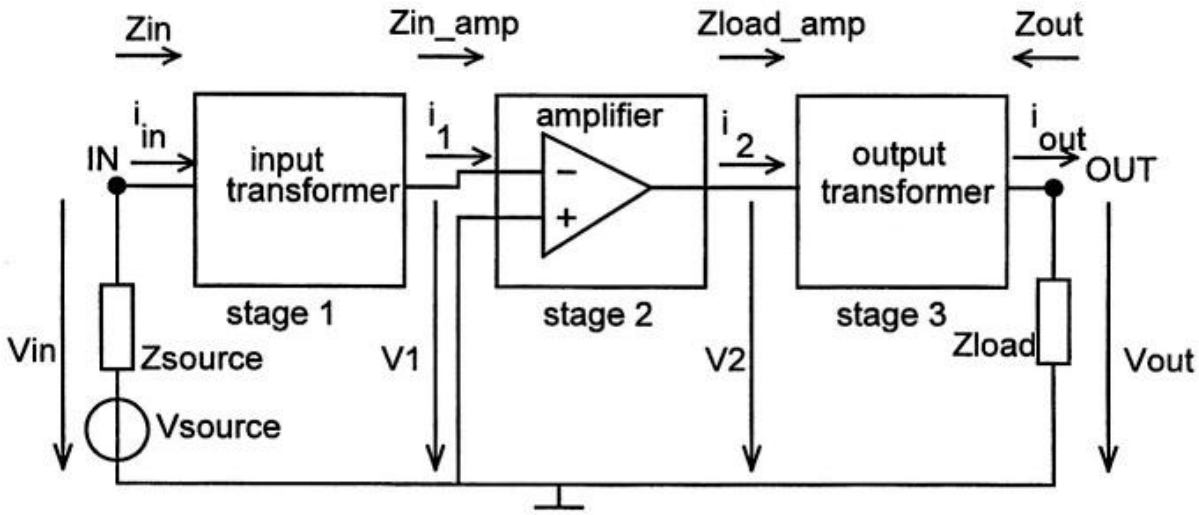


Figure 42: LNA internal structure

LNA is basically consists of two matching circuits in both input and output and a gain stage between them.

4.3. Gain:

1- Voltage gain:

$$(A_v = V_{Load}/V_1)$$

2- Power gain:

$$G_P = (P_{out,\ delivered})/(P_{in,\ delivered}) = \text{real}\ (P_{out})/\text{real}\ (P_{in})$$

4.4. Input matching transformer:

It consists of passive components, inductors and capacitors but no resistors as they add noise. It contains two matching networks, noise impedance matching and input impedance matching.

4.5. Why do we need to use input matching circuit (input transformer)?

Using input matching impedance reduces the bandwidth of the LNA; however, we need it to reduce both power consumption and CMOS transistor width. If we don't use matching impedance we would have LNA with noise figure about 1dB in 1GHz band between 1GHz and 2GHz, but with an extremely large transistor width and high power consumption for small frequency band.

The input transformer also keeps the level of the input within the range of LNA linearity, if the input signal level is greater it would be affected by the non-linear characteristics of the LNA components.

4.6. Using CMOS in RF application:

CMOS is used for RF applications to increase functionality and integrity. By using CMOS both RF front ends and Digital processing subsystem could be built in the same die. MOS transistors have similar performance in RF applications as BJT.

Due to noise reduction, we usually use single transistor in CMOS RF designs to reduce noise, the fewer transistors the better.

4.7. Design Steps:

There are some parameters that are required to determine before designing the LNA to obtain the required performance in noise figure, linearity and power consumption, they are:

1- Channel length **L** and channel width **W**.
2- Gate-source voltage ($\mathbf{V_{gs}}$).
3- Voltage supply ($\mathbf{V_{dd}}$).

These parameters are obtained for a given source and load impedances in a specified frequency band.

4.8. Choice of channel length:

The channel length is chosen to be the minimum length provided by the technology ($L=2\lambda$) to obtain better performance by reducing parasitic capacitance.

4.9. Choice of V_{gs}:

The smaller is the better, to achieve the lowest *NF*. V_{gs} of 0.7V is selected to achieve that.

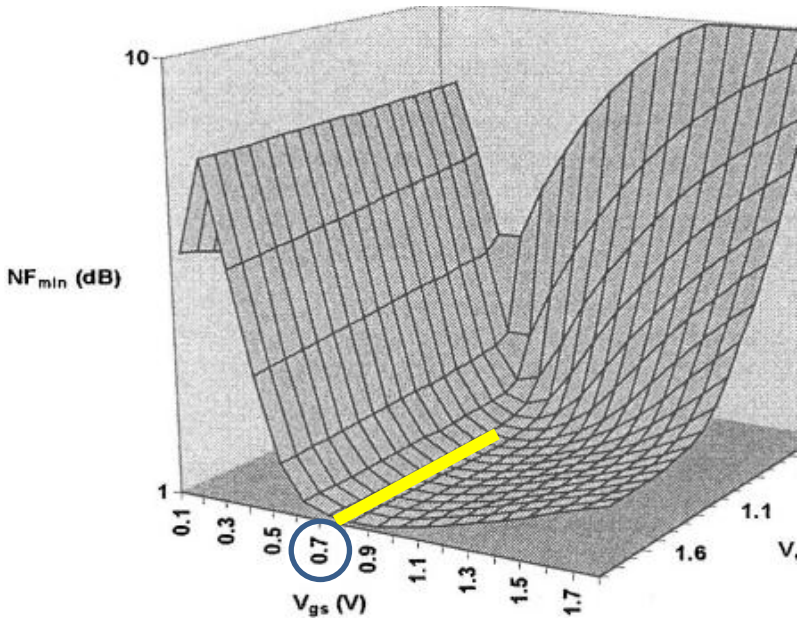


Figure 43: plot of minimum noise figure vs. V_{gs} and source voltage

4.10. Choice of transistor width:

The width of the transistor is selected according to the desired OIP_3, minimum transistor width means less current and power consumption as well, which means less noise. If impedance matching is going to be achieved on-chip, width is determined by both linearity and required input impedance.

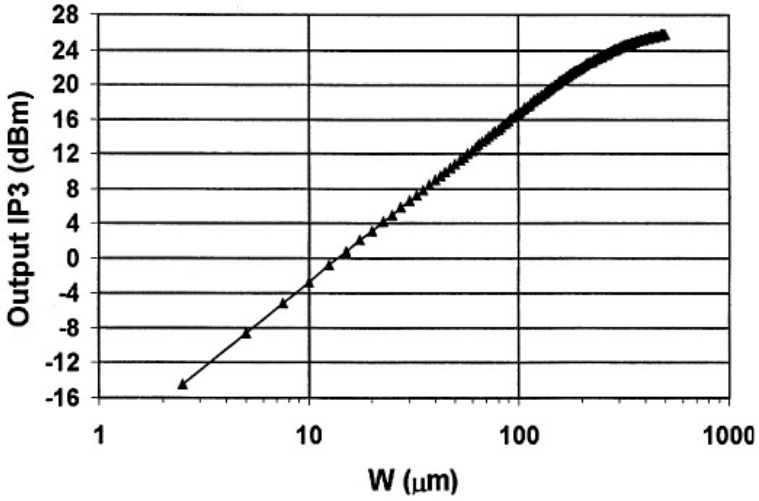


Figure 44: simulated OIP3 vs. width of a transistor biased with Vds=0.9V, Vgs=0.7V

4.11. Common LNA topologies:

4.12. Single ended LNA:

4.12.1.1. Common gate LNA

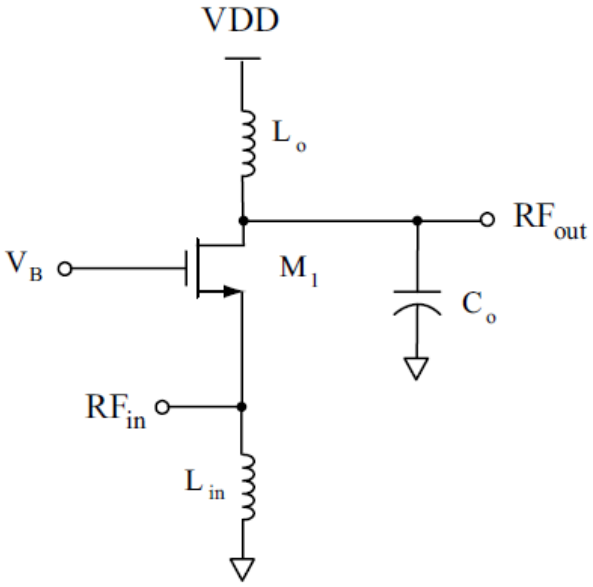


Figure 45: Common gate LNA with inductive source degeneration.

The most widely used LNA topologies in CMOS technology are common-gate and inductively degenerated cascade.

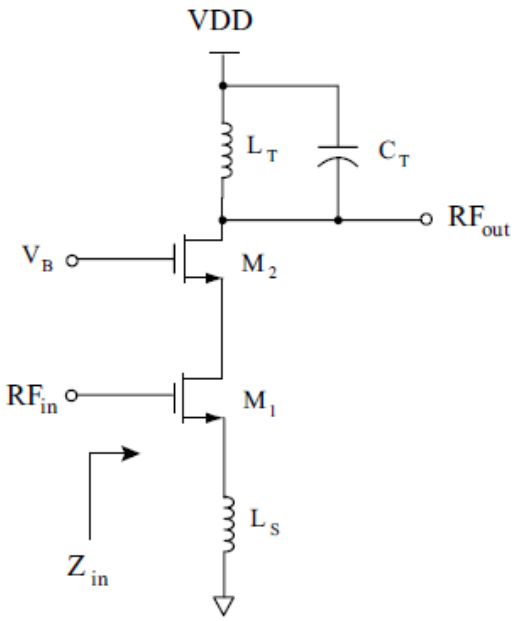


Figure 46: Inductively degenerated cascade LNA

Both of these topologies allow a high reverse isolation that helps with the LNA's stability. If the input matching and noise requirements are met, the IIP3 of both the common gate and cascode LNAs are typically better than -5 dBm. Therefore, in CMOS receiver implementation the linearity of the LNA will not be the limiting factor and the mixer and subsequent stages will limit the linearity of the receiver.

Matching of the input of the common-gate LNA is easier than the cascode LNA. The voltage gain (A_v) of a common-gate LNA is equal to

$$A_v = \frac{Q_i g_m Q_o}{\omega_o C}$$

Where Q_i and Q_o are the input matching and resonant load quality factors, respectively, g_m is the transcondutance of the transistor M1 and ω_o is the angular frequency of operation.

The minimum noise figure of the LNA can be written as:

$$NF = 1 + (\gamma / g_m) G_s$$

Here γ, the channel current noise factor, is a bias dependent factor that for long channel devices satisfies the inequality of

$$\frac{2}{3} \leq \gamma \leq 1$$

When the transistor is saturated, γ is equal to 2/3 and when the drain-source voltage is zero, it is equal to one.

$G_s = g_m$ when the amplifier is perfectly impedance matched.

4.13. Differential LNA

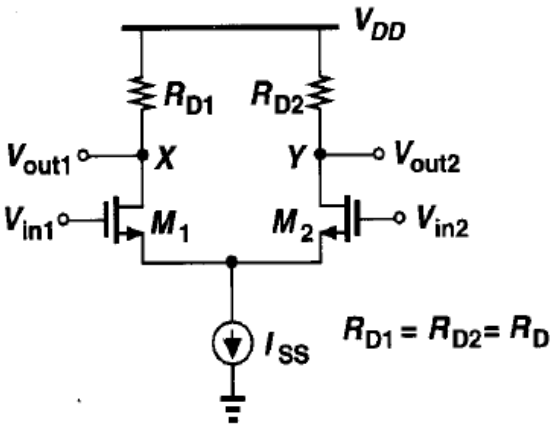


Figure 47: basic differential amplifier

- **Single ended and differential ended:**

A single ended signal is measured with respect to a fixed potential, usually the ground. A differential signal is defined as one that is measured between two nodes that have equal and opposite signal with respect to fixed potential.

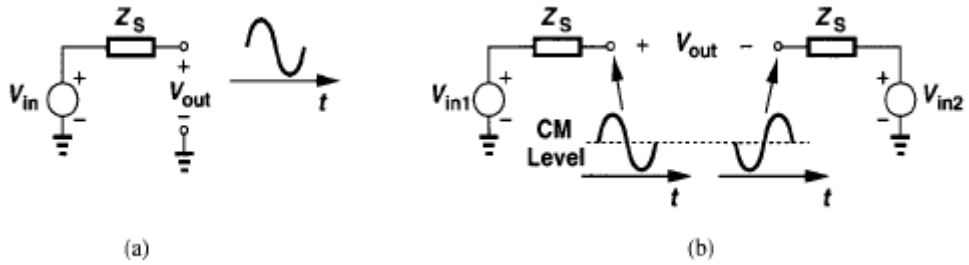


Figure 48: (a) Single ended, (b) differential signals

Features of differential LNA over traditional single-ended LNA:

1- Rejects any corruption to the signal due to the presence of another signal nearby, specially the clock in the mixed-signal ICs.
2- Provides twice the gain of a single-ended amplifier.
3- Reduce the effect of parasitic due to its symmetrical layout around the ground.
4- Reduce the noise added to the signal while amplification.

Drawbacks:

1- Larger layout area.
2- Higher power dissipation.

Differential inputs provide a more stable reading when EMI or RFI is present, and therefore, it is recommended to use them whenever noise is

generally a problem. Single-ended inputs are lower in cost and are easier to install.

To use the differential amplifier topology, a conversion stage is needed to convert the single-ended signal coming from the antenna to a differential signal and to perform impedance matching in the input.

Differential amplifier LNA is chosen to be our topology in this project because of its advantages over single-ended LNA.

Chapter- 5:
5. LNA implementation in 180nm and 130 nm technologies

The LNA was implemented using two different technologies and two different EDA, the first was TSMC 180nm using Cadence Virtuoso, the second was TSMC 130nm in Advanced Design System from Agilent.

5.1. Single-ended to differential signals conversion stage [balun]:

The problem in using differential LNA was to convert the single ended input from the antenna into differential signal. Most of the antennas in markets have single-ended output. This stage is required to perform impedance matching as well.

The basic idea is to use two different amplifiers to amplify the same signal, one of them has its output out of phase with the input, the other has its output in phase with the same input. Each of them should have the same gain.

5.1.1 Simple one MOSFET amplifier with resistive load:

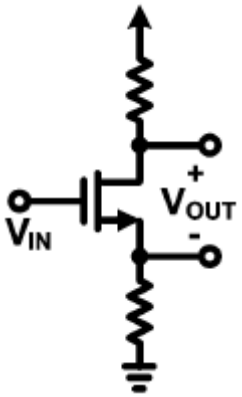


Figure 49: the resistively loaded CS amplifier with source degenerated resistor

By taking the output between the source and the drain, we get two signals out of phase, as the same current pass through the resistors:

$$V_{out}^{+} = V_{DD} - I_d R_D$$

$$V_{out}^{-} = I_d R_s$$

By choosing the values of both R_D and the biasing current, we get the out of phase signals with the same amplitude (or nearly the same).

5.1.2 CS stage with CG stage:

Common source stage provides an output with 180^{o} phase shift from the source. Common gate stage provides output in phase with the source, if we used both of them biased will to get the same gain we sill have a S-D converter.

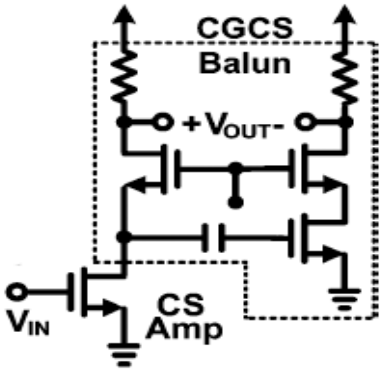


Figure 50: CS-CG single to differential converter

5.1.2 Differential amplifier with one terminals AC grounded:

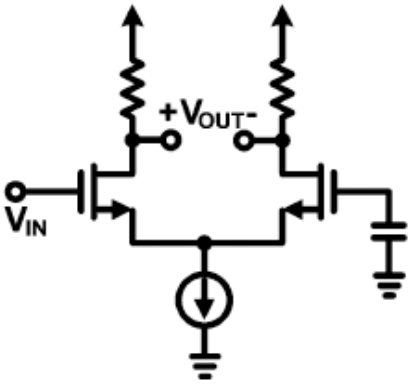


Figure 51: differential amplifier as balun

This circuit can perform as a balun if one terminal is grounded for AC signal. The derivative of the gain is i n the following:

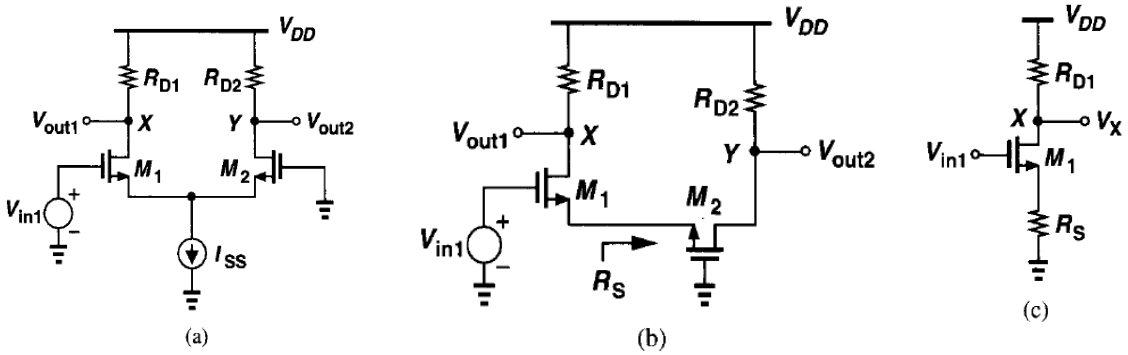


Figure 52: AC equivalent circuit for output X
(a) With AC grounded terminal,
(b) As a CS stage degenerated with M_2,
(c) Equivalent circuit.

Gain between output *X* and input is given by:

$$\frac{V_x}{V_{in}} = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

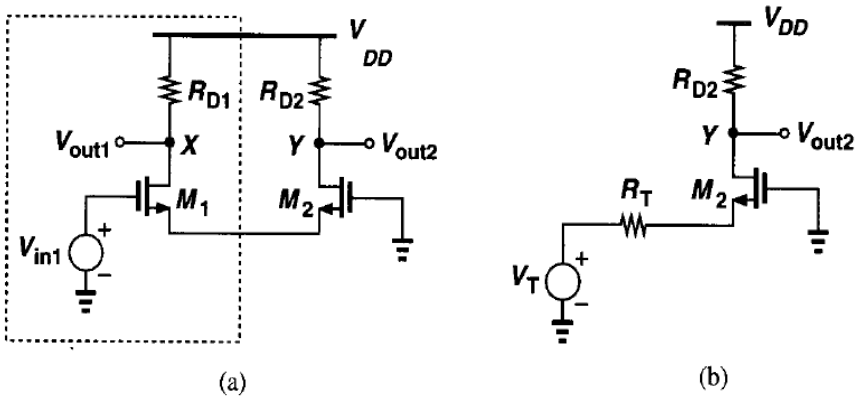


Figure 53: Replacing M1 by Thevenin equivalent

Gain between output *Y* and input is:

$$\frac{V_y}{V_{in}} = +\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

If $g_{m1}=g_{m2}=g_m$,

$$V_x/V_{in} = -R_D g_m \qquad \text{and } V_y/V_{in} = +R_D g_m$$

This topology was chosen in this design because it is simple in biasing and provides gain to the signal.

5.2. Differential stage

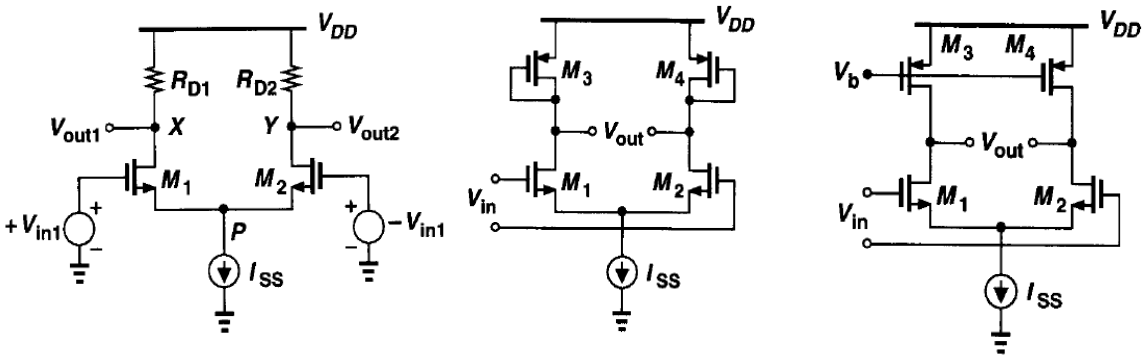


Figure 54: traditional differential stage
From left to right, resistive loaded,
diode connected load, current source load

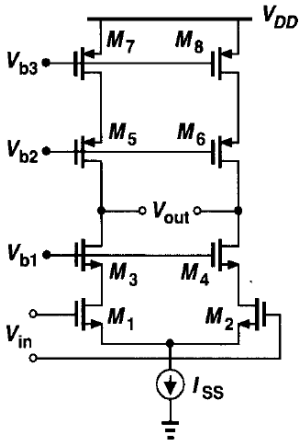


Figure 55: cascode differential pair

Figure 54 and 55 show different topologies for differential pair.

In RF LNA, the use of LC circuits is made to get better performance especially in biasing, gain and noise the following topology is chosen to simplify the biasing of the circuit and increase the isolation between input and output as well as increasing the gain.

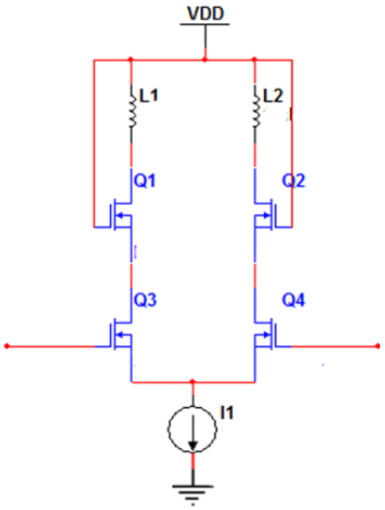


Figure 56: cascode LNA withinductive load

5.3. Implementation of the proposed LNA in TSMC 130nm, ADS2009:

5.3.1 Schematic diagram:

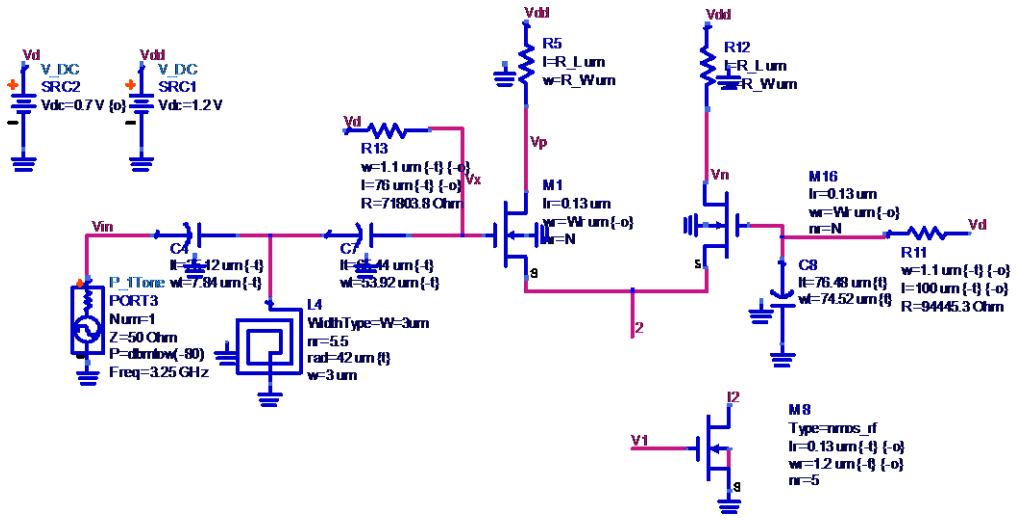


Figure 57: single to differential stage

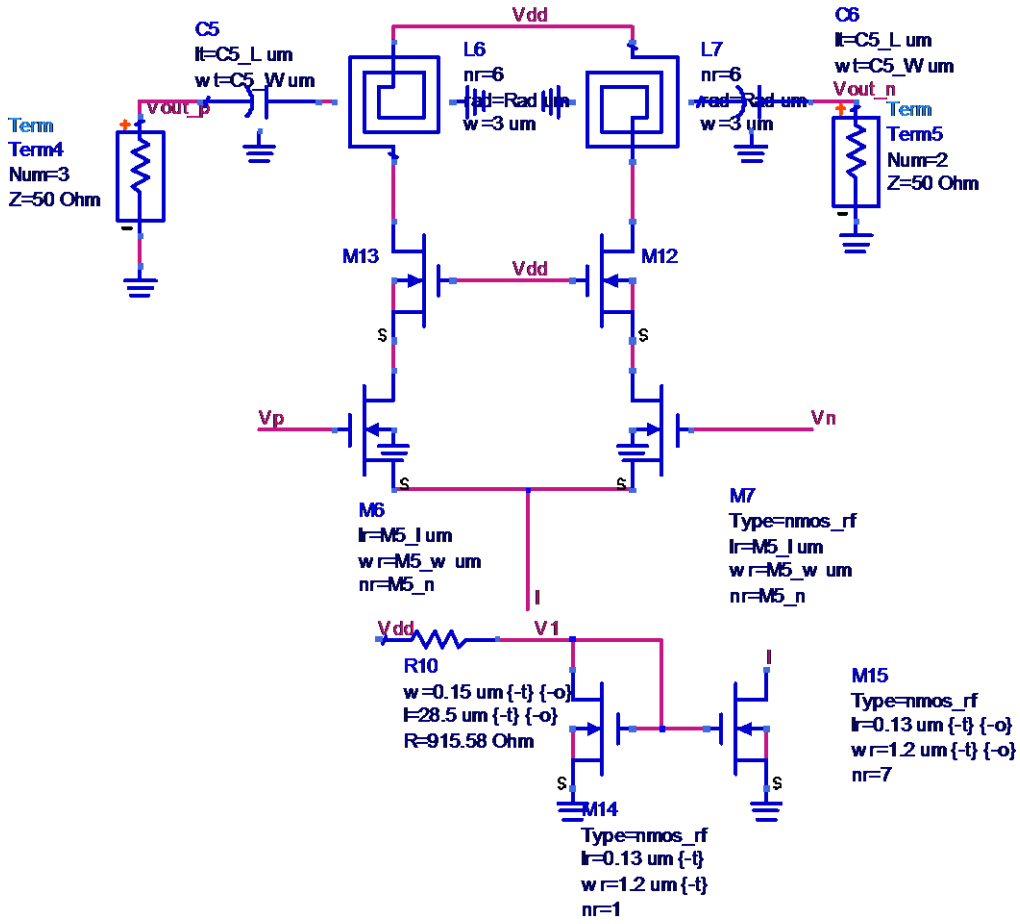


Figure 58: cascode differential pair

5.3.2 Simulation results:

a. S-parameters simulation:

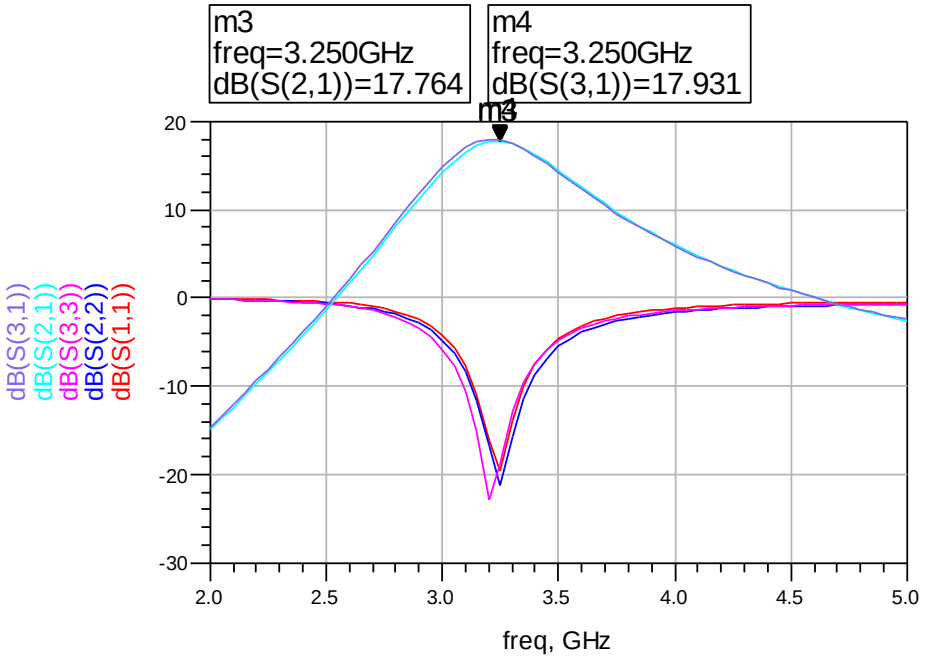


Figure 59: S-Parameters simulation results

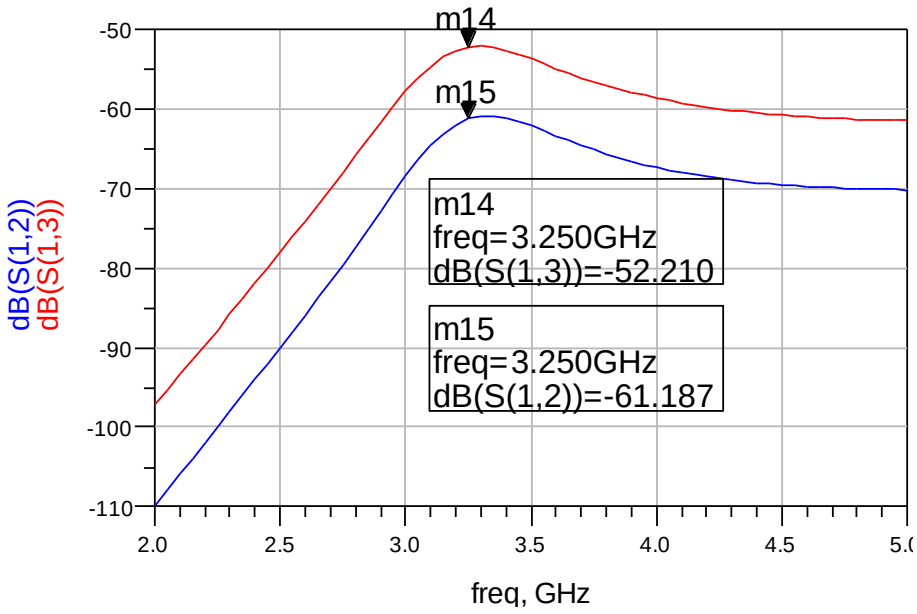


Figure 60: Isolation

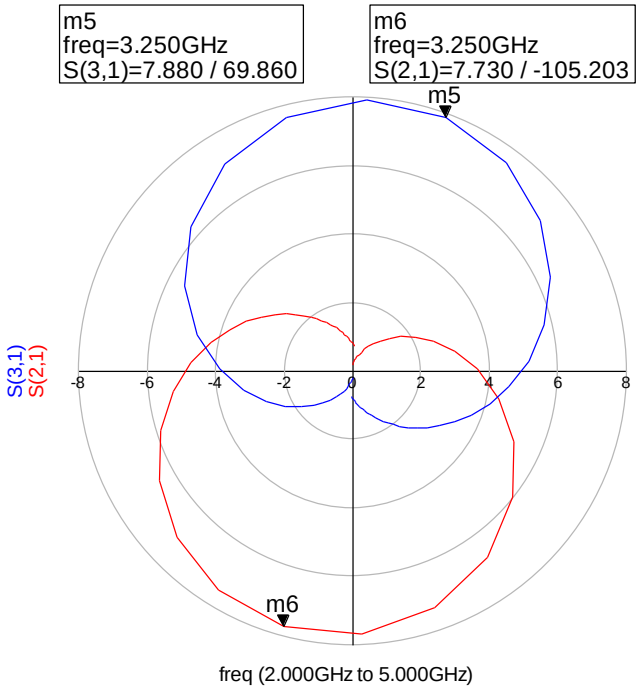


Figure 61: Polar plot of S-Parameters

b. Noise figure:

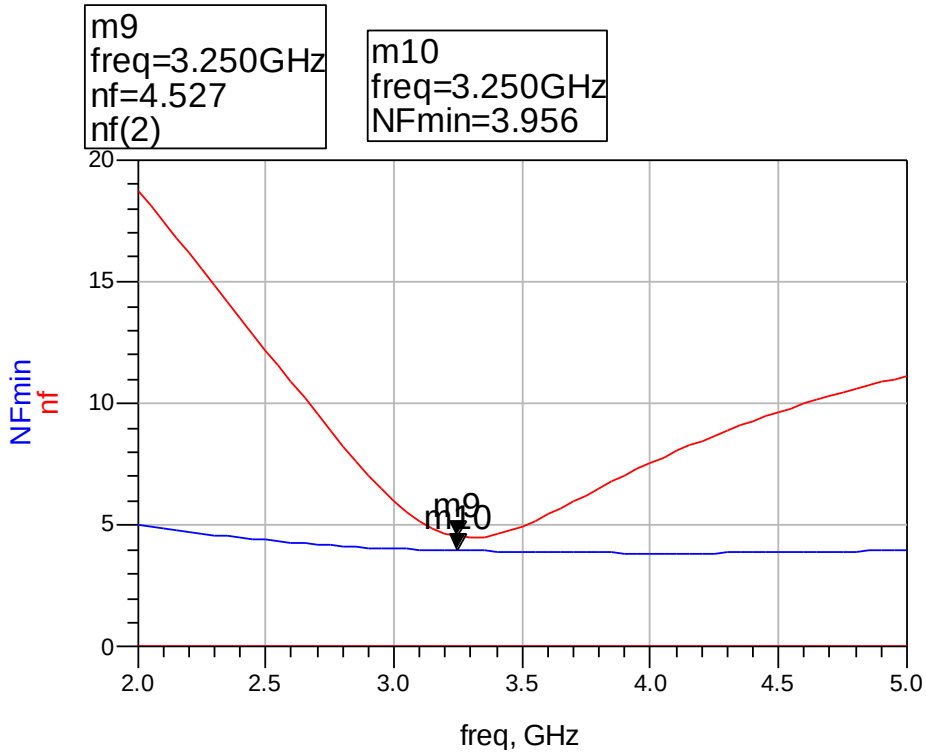


Figure 62: noise figure

c. Transient Simulation:

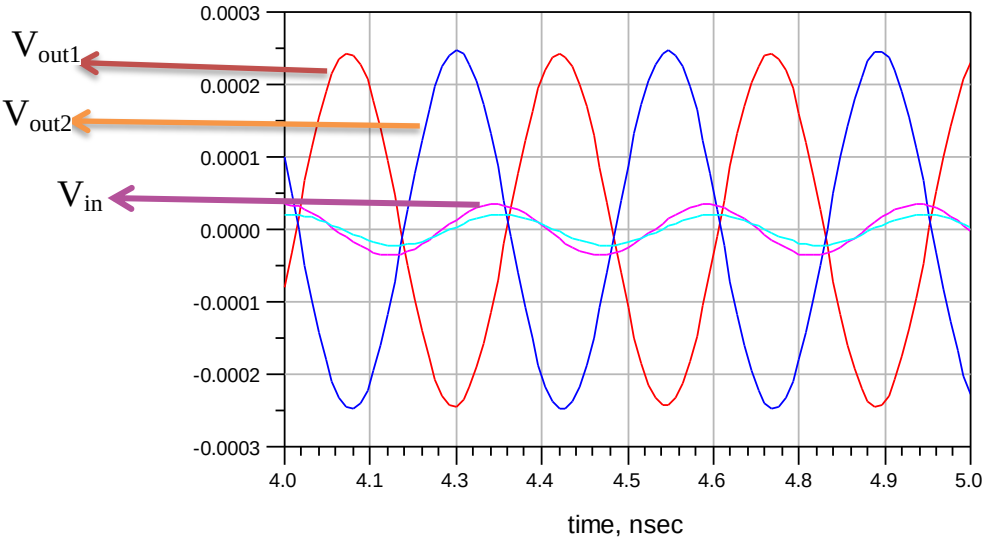


Figure 63: transient simulation results

d. Stability factor

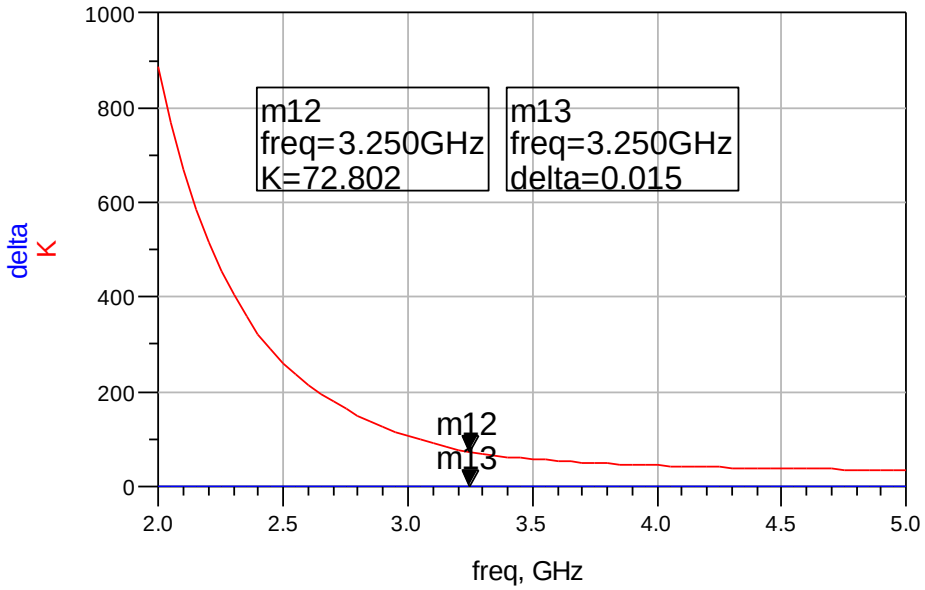


Figure 64: stability factor result

5.4. Implementation in TSMC-180nm in cadence virtuoso:

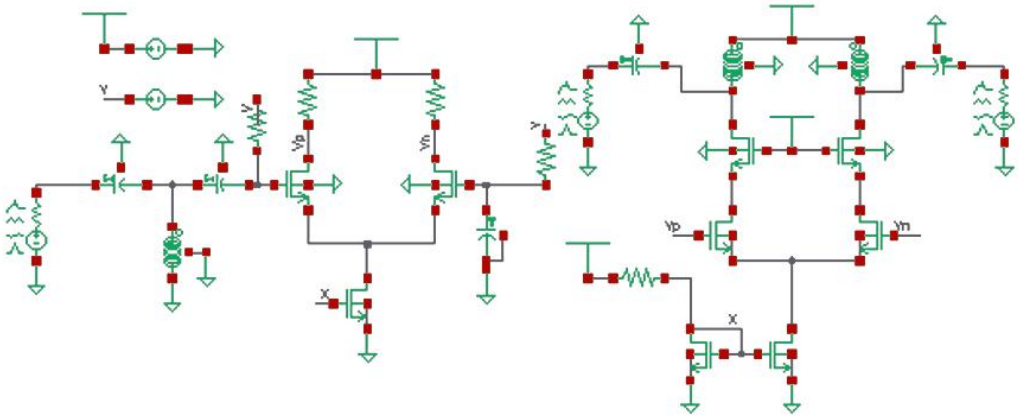


Figure 65: Schematic diagram

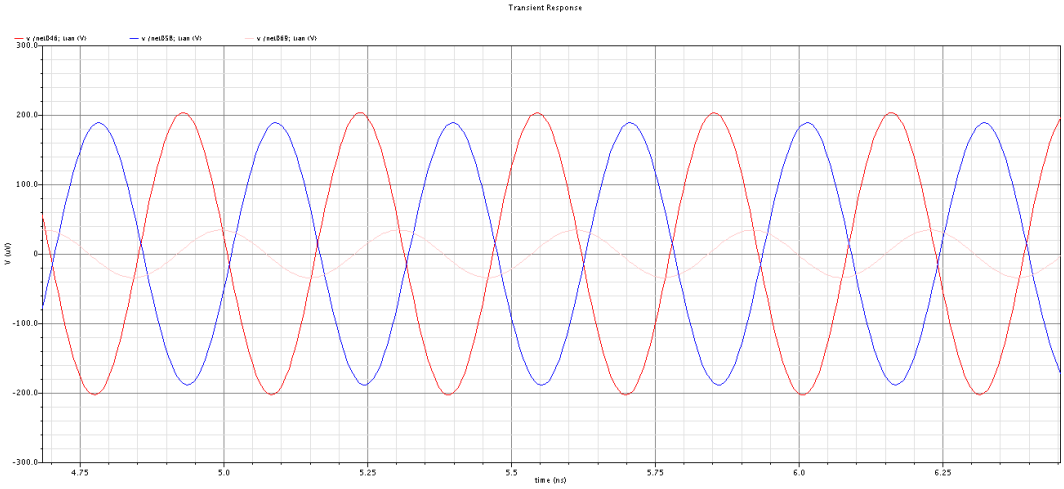


Figure 66: LNA 180nm transient simulation result

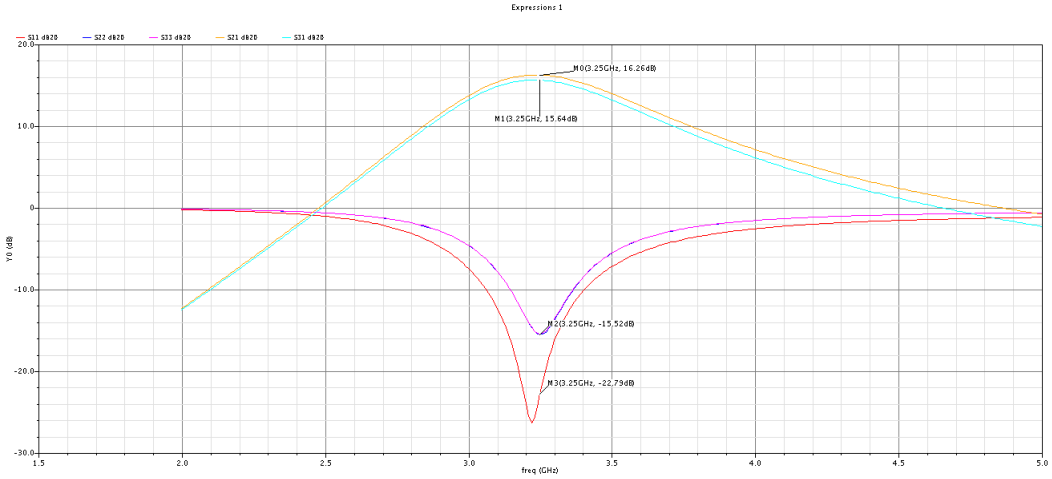


Figure 67: S-Parameters simulation

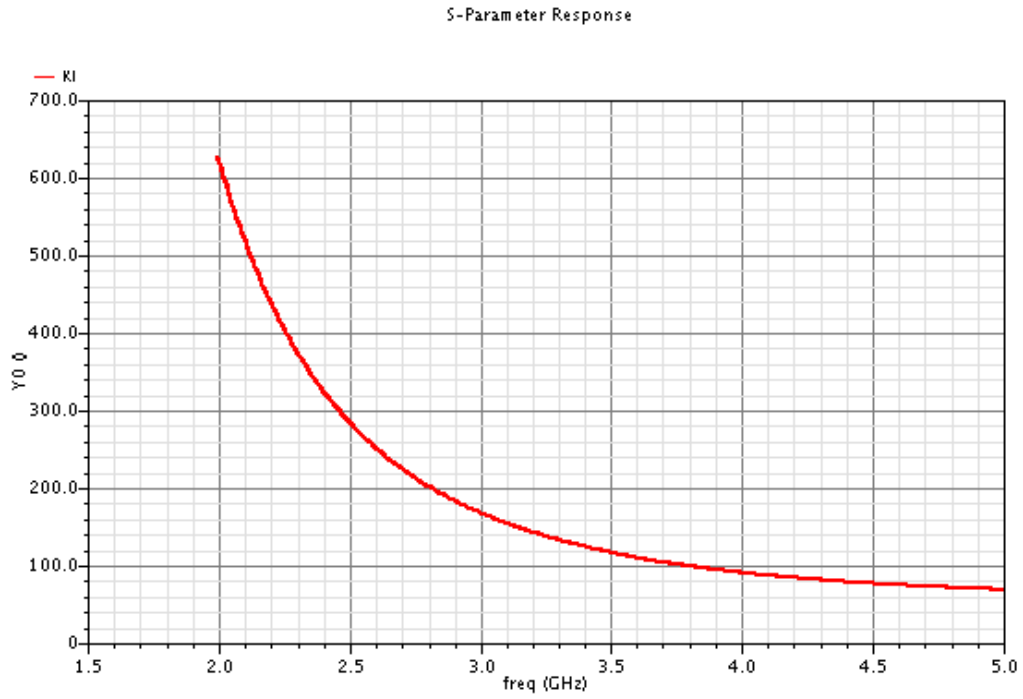


Figure 68: LNA stability factor

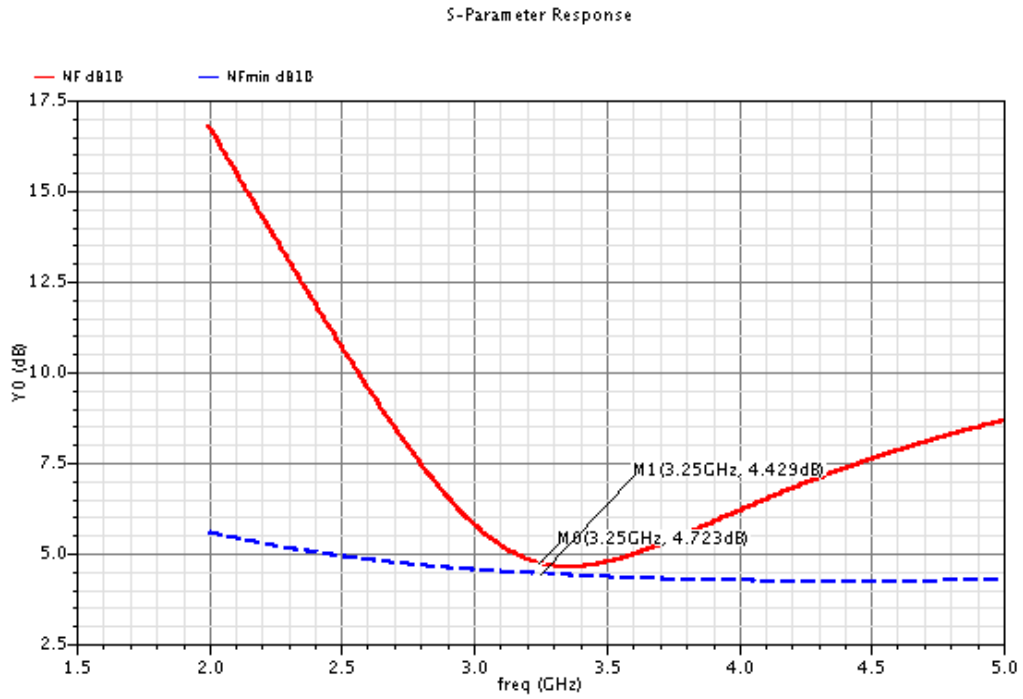


Figure 69: Noise figure

LNA Summary:

Table 4: LNA results in 130nm

Gain	17.7 dB
Input Matching	S_{11}= -19.6 dB
Output matching	S_{22}= -21.3 dB S_{33}= -22.9 dB
Input/output isolation	S_{12}=-61 dB S_{31}= -52 dB
Noise figure	4.5 dB
Stability factor	72.8
Delta	0.015

Table 5 : LNA results in 180 nm

Gain	15.6 dB
Input Matching	S_{11}= -22.7 dB
Output matching	S_{22}= -15 dB S_{33}= -15.5 dB
Input/output isolation	S_{12}=-61 dB S_{31}= -52 dB
Noise figure	4.7 dB
Stability factor	150

CHAPTER 6
6. Mixers

6.1. Introduction:

RF Mixers are 3-port active or passive devices. They are designed to yield both, a sum and a difference frequency at a single output port when two distinct input frequencies are inserted into the other two ports.

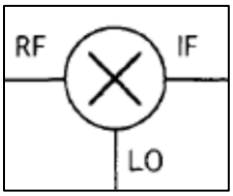


Figure 70: Mixer

The two signals inserted into the two input ports are usually the Local Oscillator signal, and the incoming (for a receiver) or outgoing (for a transmitter) signal. To produce a new frequency (or new frequencies) requires a nonlinear device.

The multiplication process begins by inputting two signals:

$a = A\sin(\omega_1.t + \varphi_1)$ and signal $b = B\sin(\omega_2.t + \varphi_2)$

The resulting multiplied signal will be:

$$a.b = AB\sin(\omega_1.t + \varphi_1).\sin(\omega_2.t + \varphi_2)$$

This can be multiplied out thus:

Using this trig identity …. $\sin A \sin B = \frac{1}{2}(\cos(A+B) - \cos(A-B))$

Where $A = (\omega_1.t + \varphi_1)$ and $B = (\omega_2.t + \varphi_2)$

$$a.b = -\frac{AB}{2}[\cos((\omega_1.t + \varphi_1) + (\omega_2.t + \varphi_2)) - \cos((\omega_1.t + \varphi_1) - (\omega_2.t + \varphi_2))]$$

$$a.b = -\frac{AB}{2}[\cos((\omega_1 + \omega_2)t + (\varphi_1 + \varphi_2)) - \cos((\omega_1 - \omega_2)t - (\varphi_1 - \varphi_2))]$$

Sum frequency

Difference frequency

In a mixing process if we want to produce an output frequency that is lower than the input signal frequency, then it is called *down-conversion* and if we want to produce an output signal that is at a higher frequency than the input signal, it is referred to as *up-conversion*.

6.2. A down-conversion system

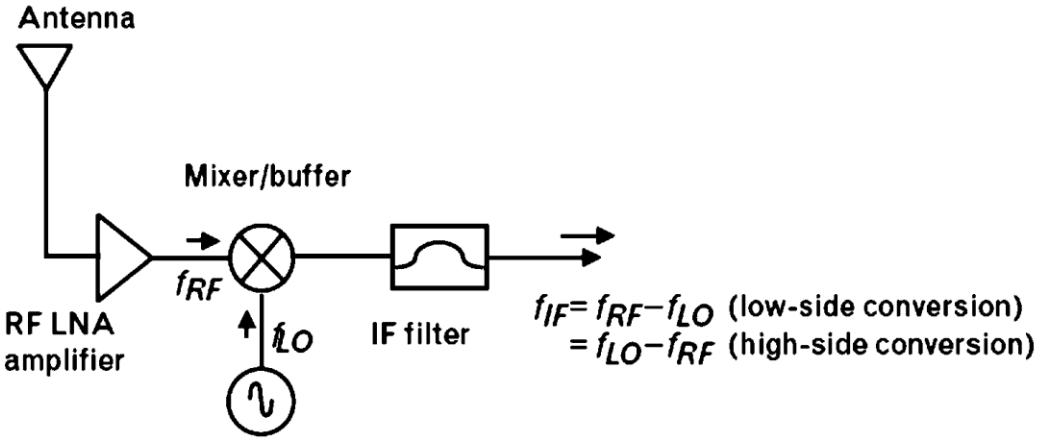


Figure 71: down-conversion system

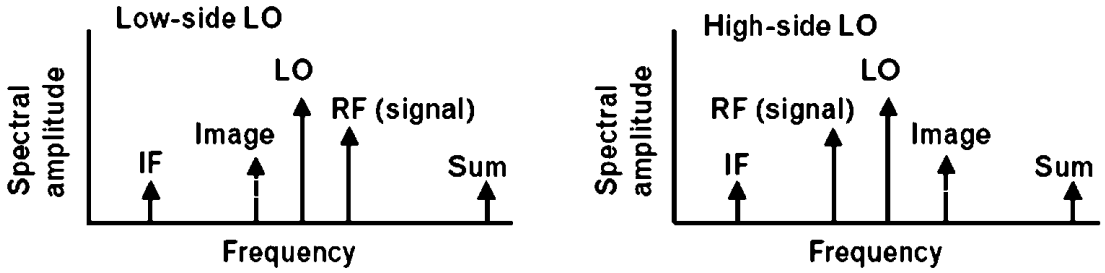


Figure 72: output of down-conversion

6.3. An up-conversion system

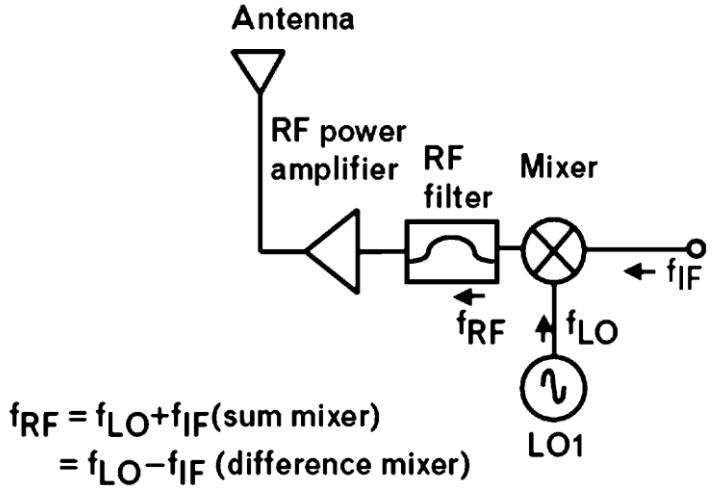


Figure 73: up-conversion system

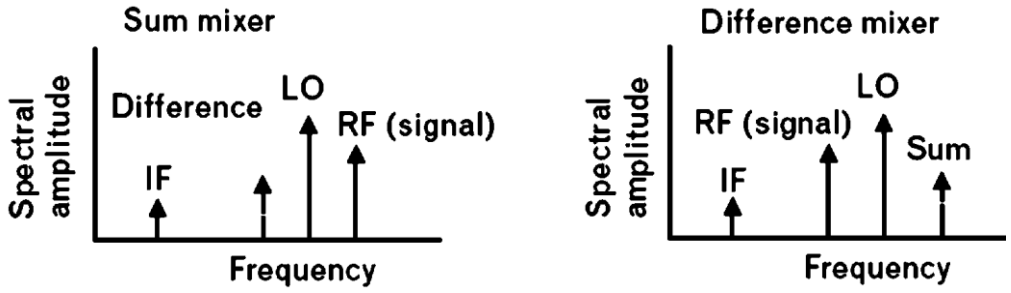


Figure 74: output of up-conversion system

A common misunderstanding about mixers is that a Mixer is only a nonlinear device. Actually an RF Mixer is fundamentally a linear device, which is shifting a signal from one frequency to another, keeping (faithfully) the properties of the initial signal (phase and amplitude), and therefore doing a linear operation.

In contrast to frequency multipliers and dividers, which also change signal frequency, Mixers theoretically preserve the amplitude and phase without affecting modulation properties of the signals at its ports.

- Up conversion mixers are used in the transmit path.
- Down-conversion mixers are used in the receiver path.

6.4. Important Mixer properties are:

1- Conversion Gain or Loss.
2- Intercept point.
3- Spurious products
4- Isolation.
5- Noise Figure.

6.4.1. Conversion Gain or Loss

The typical conversion gain of an active Mixer is approximately +10dB when the conversion loss of a typical diode mixer is approximately -6dB.

The Conversion Gain or Loss of the RF Mixer measured in dB is given by:

Conversion [dB] = Output IF power delivered to the load [dBm] – Available RF input signal power [dBm]

6.4.2. Input Intercept Point (IIP3)

is the RF input power at which the output power levels of the unwanted intermodulation products and the desired IF output would be equal.

From an RF System point of view, Mixer linearity is more critical than Noise Figure.

The Third-Order intercept point (IP3) in a Mixer is defined by the extrapolated intersection of the primary IF response with the two-tone third-order intermodulation IF product that results when two RF signals are applied to the RF port of the Mixer.

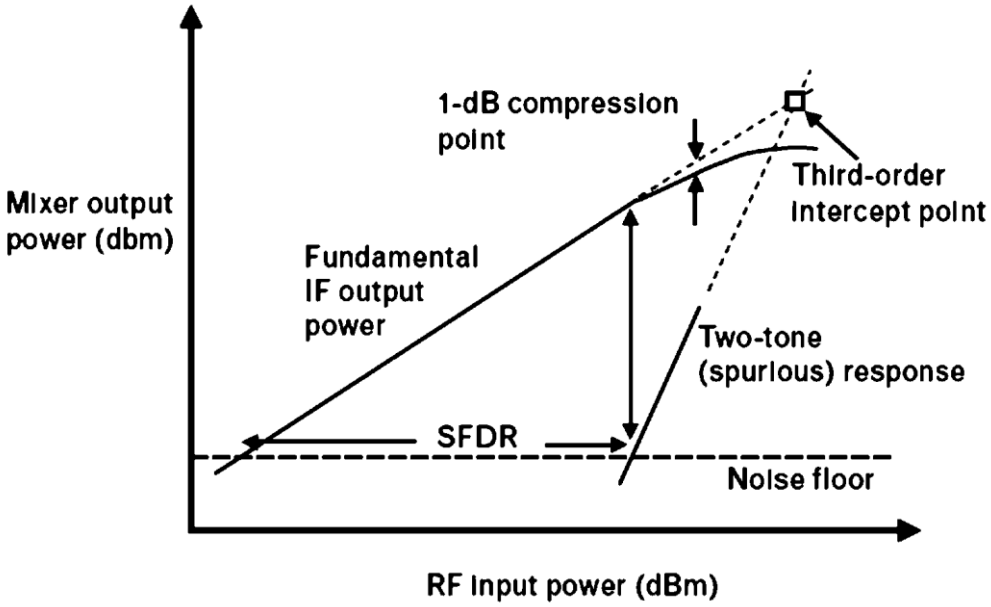


Figure 75: Input Intercept Point

6.4.3. Spurious products

in a Mixer are problematic, and Mixer vendors frequently provide tables showing the relative amplitudes of each response under given LO drive conditions.

Reducing the second or third harmonic of the local oscillator reduces its harmonic products by 20 to 25 dB and 10 to 15 dB, respectively.

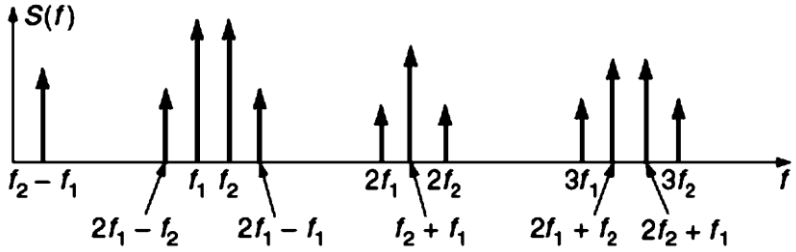


Figure 76: harmonic products

6.4.4. Isolation

is the amount of local oscillator power that leaks into either the IF or the RF ports. There are multiple types of isolation: LO-to-RF, LO-to-IF and RF-to-IF isolation.

6.4.5. Noise Figure

NF is defined as the ratio between the input and output S/N ratio.

$$NF = 10\log\left[\frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}}\right]$$

SSB and DSB NF: There are two definitions used for noise figure with mixers.

SSB NF:

It assumes signal input from only one sideband, but noise inputs from both sidebands. Measuring ***SSB noise figure*** is relevant for super heterodyne receiver architectures in which the image frequency is removed by **filtering or cancellation.**

With a SSB measurement, the mixer internal noise shows up at the IF output from both signal and image inputs, but the excess noise is only introduced in the signal frequency band.

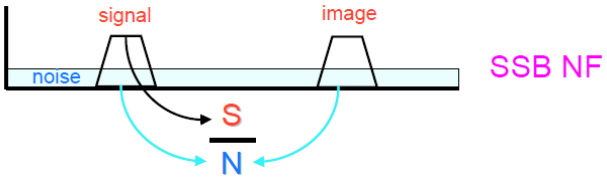


Figure 77: SSB NF

DSB NF:

1- It includes both signal and noise inputs from both sidebands. Appropriate for direct conversion architectures.
2- A DSB NF is easier to measure; wideband excess noise is introduced at both the signal and image frequencies. It will be 3 dB less than the SSB noise figure in most cases.
3- This is perhaps more relevant for direct conversion receivers where the image cannot be filtered out from the signal.
4- Either type of measurement is valid so long as you clearly specify what type of measurement is being made.

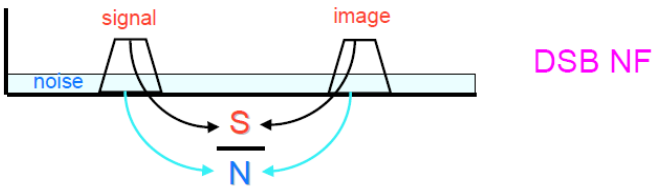


Figure 78: DSB NF

6.5. Mixer classes:

Mixers can be divided into several classes:

1. Single-device Mixer
2. Single Balanced Mixer
3. Double Balanced Mixer.

6.5.1 Single-device Mixer which is using one nonlinear component (one diode, or one transistor).

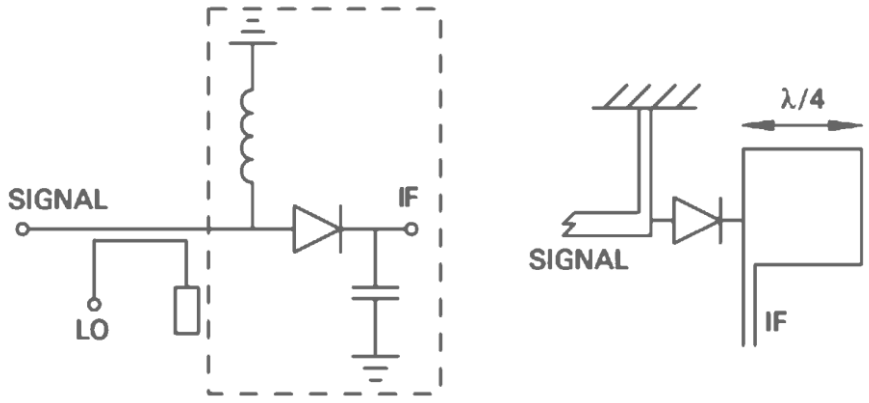


Figure 79: Single-device Mixer with diode

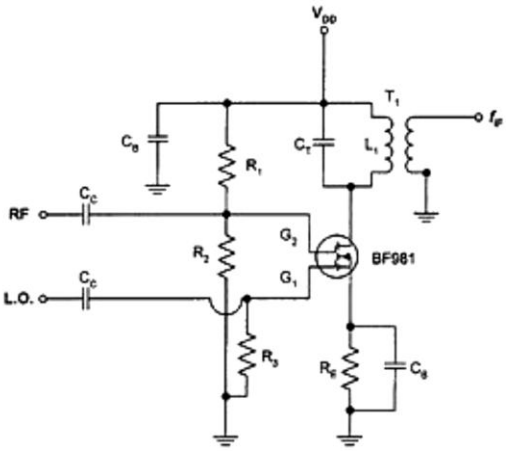


Figure 80: Single-device Mixer with FET

Advantages

They are cheap, require few components, and are relatively easy to design.

Disadvantages

- They are lower performing passive mixers.
- They have a relatively narrow bandwidth, poor port-to-port isolation, low intercept point.

6.5.2. Singly-Balanced mixers use two devices, and are usually realized as two single device mixers connected via a 180-degree or 90-degree hybrid.

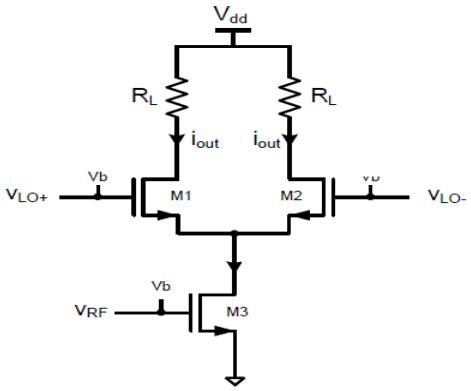


Figure 81: Singly-Balanced mixers

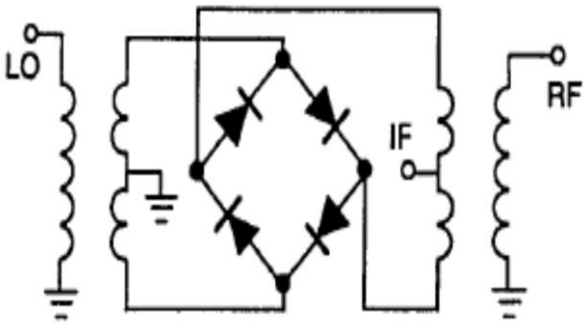
Advantages

- This mixer has good isolation between LO and IF, and also between RF and LO. But RF signals goes directly to the IF output.

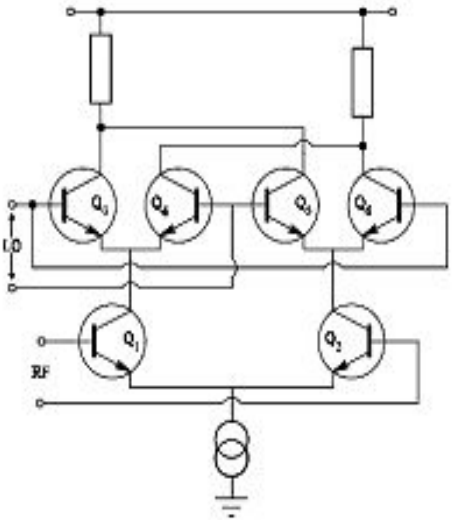
Disadvantages

- LO power must often be somewhat higher (which necessitates a more expensive and power hungry oscillator).
- Mixer products are suppressed to varying levels, strongly dependent on the quality of the diode match and the accuracy of the balun balance.

6.5.3. Double balanced mixers usually consist of four un-tuned devices interconnected by multiple hybrids, transformers or baluns.



A: Double balanced mixers with diode



B: Double balanced mixers with BJT

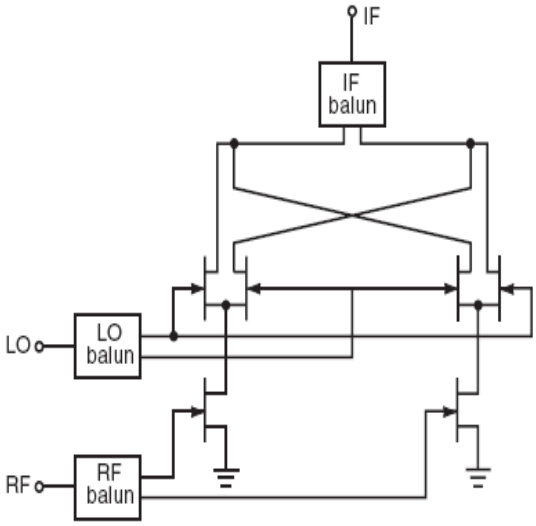


Figure 82: Double balanced mixers

Advantages

- Wider bandwidth.
- Higher intercept point.
- Good port to port isolation.

Disadvantages

- Because of the highly nonlinear nature of the diodes, the impedances at the three ports are poorly controlled, making matching difficult.
- This cannot provide conversion gain; there will be a conversion loss.
- A practical mixer will have higher losses, due to the resistances of the diodes and the losses in the transformers.

6.6. SPECIFICATION

The input signals in the receiver mixer are both RF signals. At the transmit side, on the other hand, the two input frequencies of the mixer are far apart, one RF signal coming from the oscillator and the other being an IF signal.

$$V_{RF}(t) = \sin(\omega_{RF}t + \omega_{bb}t)$$

Where the RF carrier frequency is 1 GHz and the signal information frequency F_{bb}= 1MHz. If the local oscillator (LO) frequency to 1.5 GHz and the mixer is ideal, except for linearity, i.e OIP3=-5 dBm,

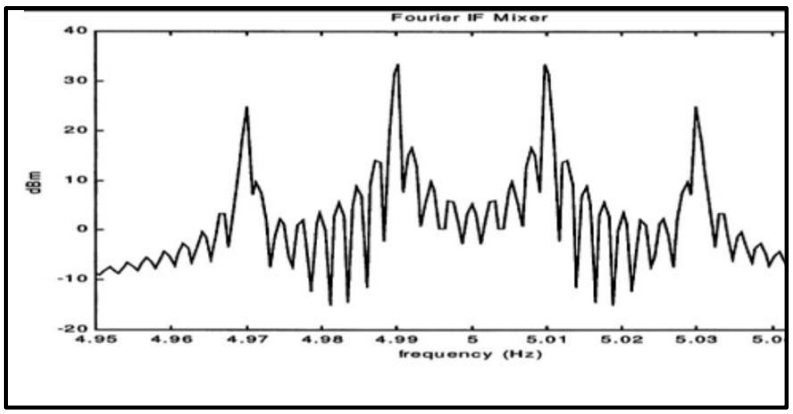


Figure 83: Fourier IF Mixer

If the IF filters following the mixer are not that good, harmonics will be present at the output of the receiver and will there by distorting the information signal .When a strong interferer is present in a co-channel or adjacent channel, it is clear that these signals will mix with the wanted tones, and an unwanted frequency spectrum arises.

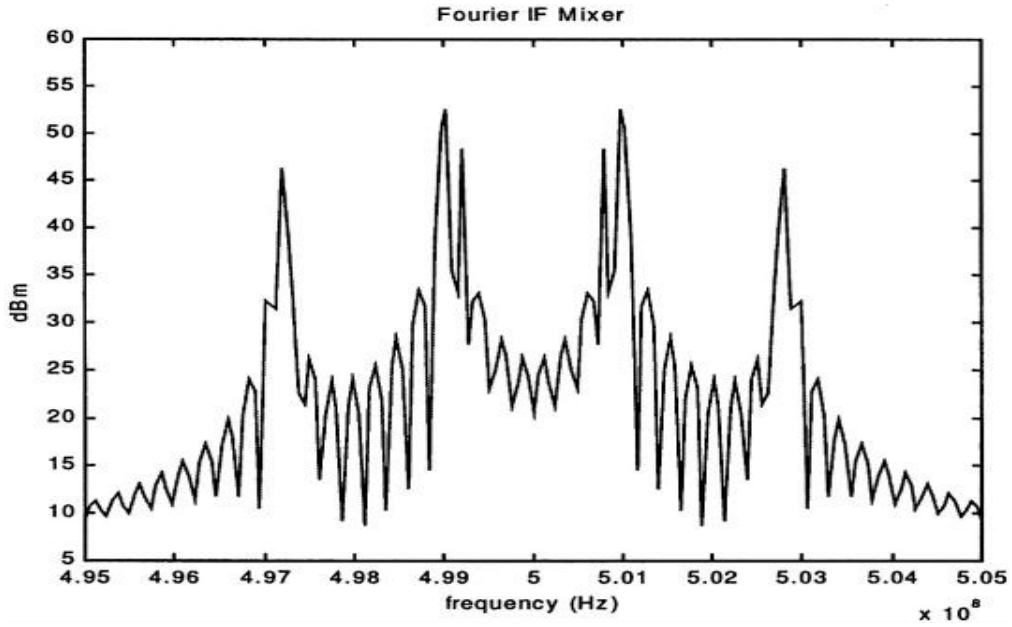


Figure 84: Output spectrum of the mixer when a strong interferer is present .The wanted tone at 499 MHz is difficult to distinguish from the unwanted tone at 499.2MHZ.

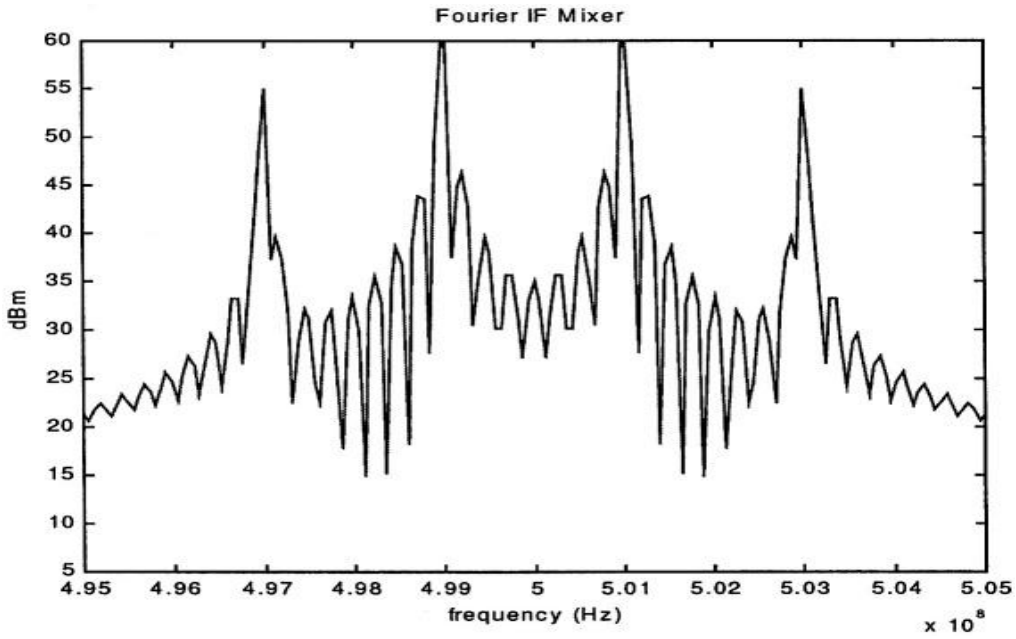


Figure16: Output spectrum at the IF port of the mixer when the mixer has a power gain of 10 dBm

Mixers can be divided into several classes, depending on the criteria used.The first commonly used criteria is the provided gain. The term "gain" often leads to confusion when considering a mixer.

The voltage conversion gain*:* is defined as the ratio of the rms voltage of the IF signal to the rms voltage of the RF signal.

The power conversion gain*:* of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source.

6.7. Types of mixer :(According to the Gain)

1-active mixer :(has high gain)

2-passive mixer: (has no gain)

6.8. Passive mixer

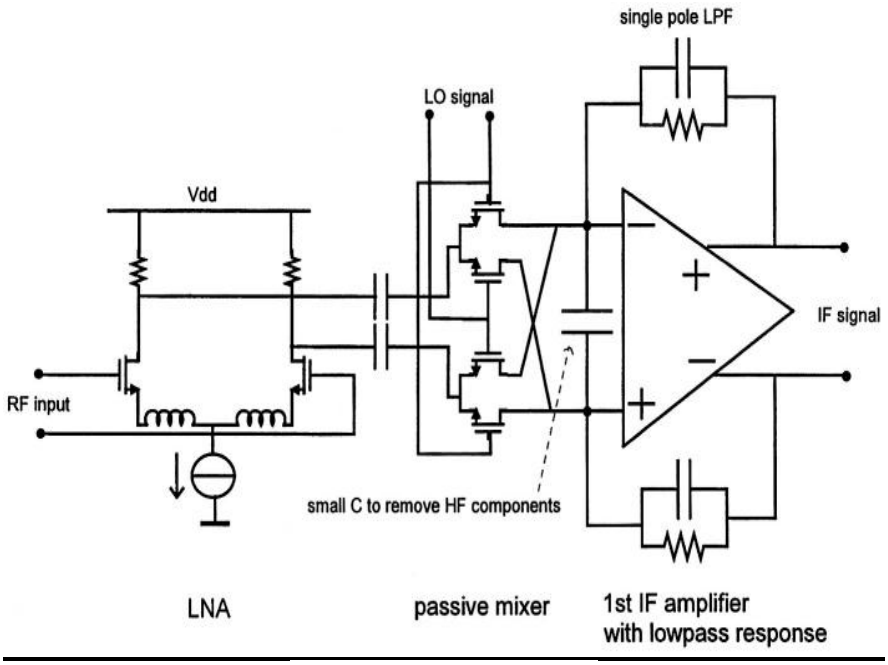


Figure 85: passive mixer

- The MOS devices are used as reversing switches in a series signal path connection.

Advantages

- The main purported advantages here are that there is no DC consumption, and that if the circuit is AC coupled,
- Therefore be no 1/*f*-noise present.
- There is no DC through the mixer transistors.

Disadvantages

- In practice it is difficult to reach the maximum conversion gain.
- the actual power conversion gain is usually below - 10 dB.

6.8.1. Gilbert or active mixers

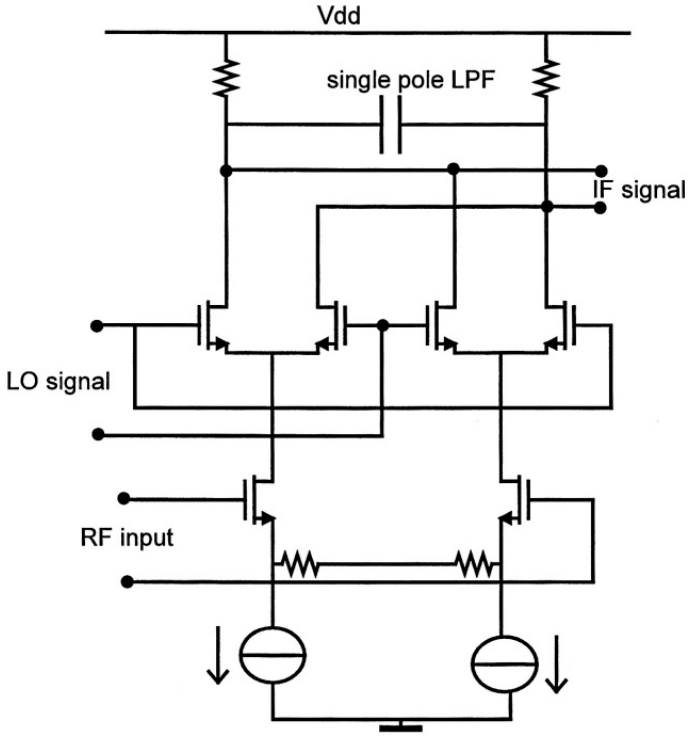


Figure 86: Gilbert mixer

The Gilbert type mixer is based on a transconductor converting the incoming RF into a current, followed by current steering transistors reversing the sense at the load as controlled by the LO drive.

- The load may be resonant, broadband, or in the case of a down-mixer, formed with a low pass pole.
- There is usually some modest signal gain through the circuit.
- Allowing a single stage LNA to be used.
- This type of mixer appears to have no obvious source of 1/*f*-noise.

Advantages

- A Gilbert mixer provides better isolation between LO and RF than a passive mixer because there is no direct signal path from LO to RF.
- Gilbert mixer can provide a smaller noise figure than a passive mixer. It can also have gain instead of loss, which together with LNA reduces the noise contribution from the IF stages, such as IF filters.

The disadvantages

- An active mixer needs a DC power supply.

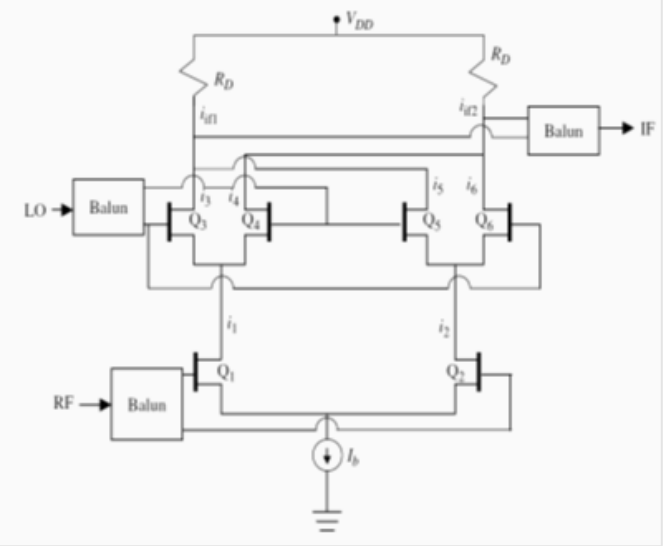


Figure 87 : Gilbert mixer

Conversion gain

The conversion gain consists of three parts, the transconductance of the RF input MOS (g_m, rf), the switching gain/loss of the Gilbert cell (Asw,) and the output impedance (R_o) . The voltage conversion gain is given by Equation

$$A\upsilon = \mathbf{g_m}, rf . R_o . Asw$$

Asw is a function of the shape and the amplitude of the LO drive and the overdrive voltage of the switching pair (V_{od}, sw). The overdrive voltage of the switching transistor depends on the drain current of the RF input transistor and the size of the switching transistor. (V_{od},sw) can be estimated by a long channel device I-V equation as is shown in Equation

$$\boldsymbol{V_{od}}, sw_0 = \sqrt{I_d, rf/(\mu_n C_{ox} * (\frac{W}{l}))}$$

When the channel of the switching transistor become short enough so that the short channel equation has to be applied, V_{od},sw is then given by Equation 3, where ρ_0 gives the measure of velocity saturation effect as in Equation 4.

$$\boldsymbol{V_{od}, sw} = \boldsymbol{V_{od}, sw_0}[\rho_{0/2} + \sqrt{\mathbf{1} + \frac{\rho_0}{2}}] \qquad \text{Equation 3}$$

Equation 4 $\qquad \rho_0 = V_{od}, \frac{sw_0}{LE_{sat}}$

Noise

There are three major noise sources in a down-conversion mixer: the noise generated in the RF input transistors, the switching noise and the

noise from the output loads. The noise generated in the input transistors is primarily from two parts. First is the drain thermal noise,

$$i^2{}_d, nois = \frac{8}{3} kT g_m, rf$$

The input referred drain noise voltage of this source can also be given by Equation 5

$$V^2{}_{in}, thermal\ noise = 8\ \text{kT/3}\ g_m, \text{rf}$$

The second noise source in the input transistor is the induced gate noise, Whose input referred value is given by Equation 6

$$i^2{}_g, noise = 4kT\delta g_g$$

$$\boldsymbol{g_g = \frac{\omega^2 C^2{}_{gs}}{5 g_{do}}}$$

Where ω is the operating angular frequency, Cgs is the gate-to-source capacitance and 9α0 is the drain conductance when V_{ds}equals zero.

Linearity

The linearity of the Gilbert mixer is often limited by the transconductance of the RF input MOSFETs. The linearity of the RF input transconductance can be expressed in term of IIV3 or IIP3. The IIV3 of a common source MOSFET is given by Equation

$$IIV3 = \sqrt{\frac{8}{3\alpha} * V_{od} * (1 + 0.5\alpha V_{od})(1 + \alpha V_{od})^2}$$

Where a is a measure of the channel velocity saturation and the mobility degradation. V_{od} is the over-drive voltage.

Chapter 7
7. The design of gilbert mixer using ADS with 130n technology

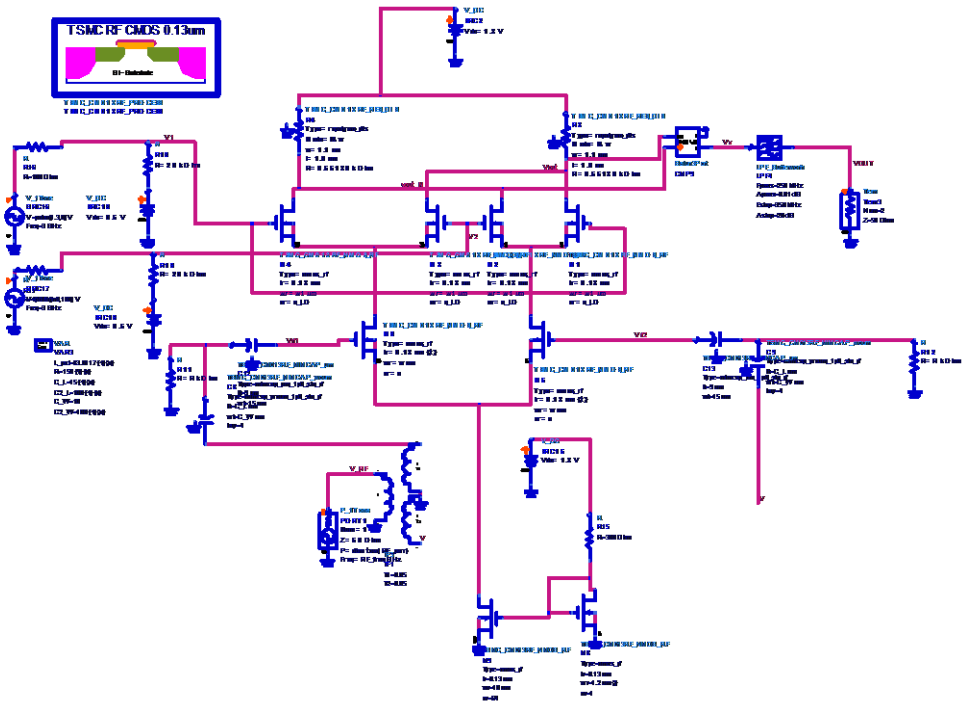


Figure 88: The design of gilbert mixer

figure 83 illustrates the gilbert mixer is obvious that, the figure consists of several stages , Current mirror , LNA part, LO part, sources, Balun and Simulation .

7.1. LNA part: consist of

a- Two transistor with W=1.5um,L=0.13um ,n= 20.
b- Matching circuit :to match the input with the circuit.
c- Balun (transformer): to convert the input from single to differential.
d- AC source as input (which output from LNA) properties of the circuit:
$I_s = I_1 + I_2$
$I_1 = I_2$
M5and M6 should be in saturation.
The matching circuit output impedance is 50Ω.
The input to this circuit is differential.

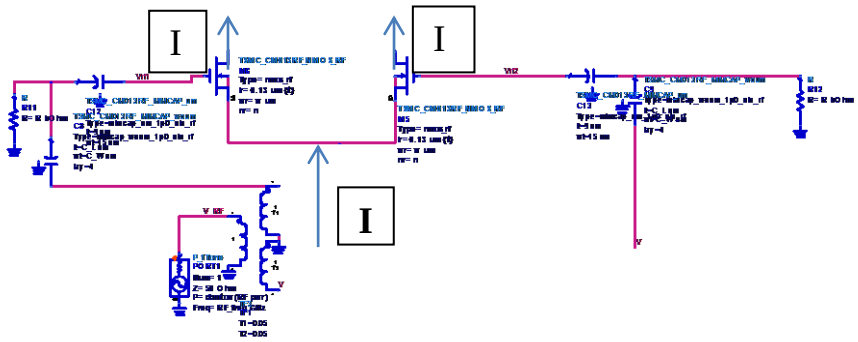


Figure 89: LNA part

LO part: consist of:

1- Four transistor Similar in width, length and no of finger (W=1.35um, L=0.13um, n=30).
2- Two resistances as load, which have the same value (R=0.55136 kohm).
3- DC source: to insure the transistors on (for biasing) .
4- AC source (as input signal witch output from LO).
5- Balun (at the output).

properties of the circuit:

1- M_1, M_2, M_3 and M_4 are working as switching, When M_1 and M_4 are on M_2 and M_3 are off, when M1 and M4 are off M2 and M3 are off.
2- $I_2 = I_1$
   $I_2 = I_3 + I_4$
   $I_1 = I_5 + I_6$
   $I_3 = I_4 = I_{5=}I_6$
3- The input is differential.
4- The output of the circuit take from the drain of M_4 and drain of M_1

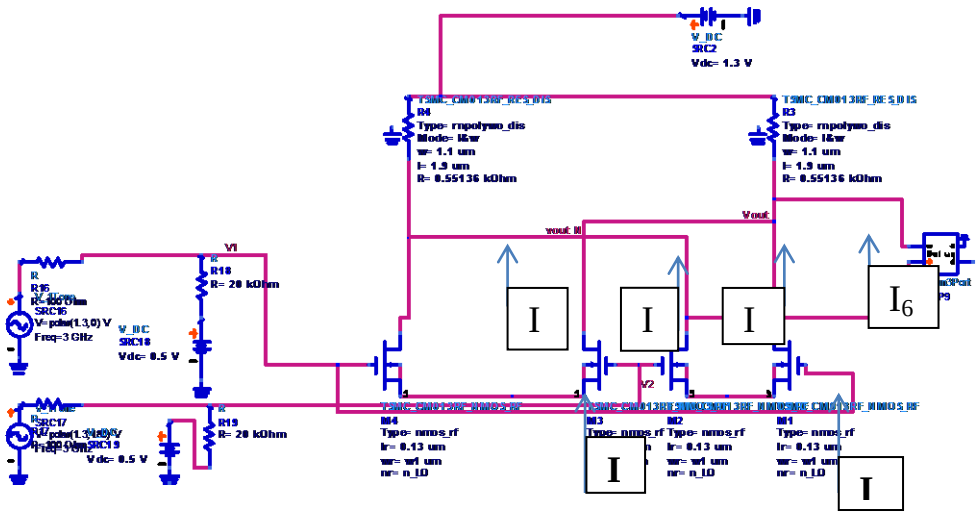


Figure 90: LO part

7.2. The result of simulation

7.11.1 The result before the filter:

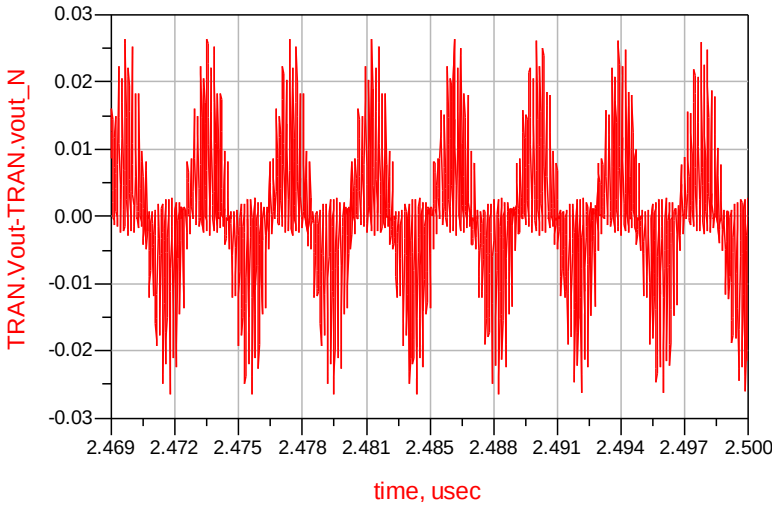


Figure 91: the output signal

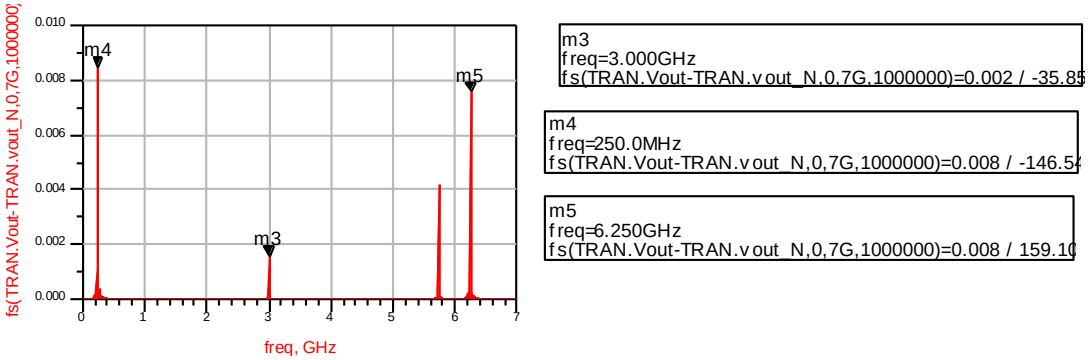


Figure 92: Fourier series

7.11.2 The result after filter:

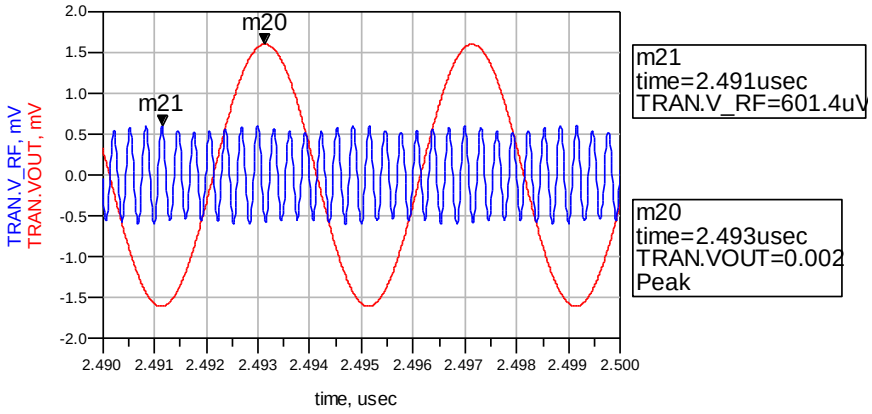


Figure 93: input and output signal

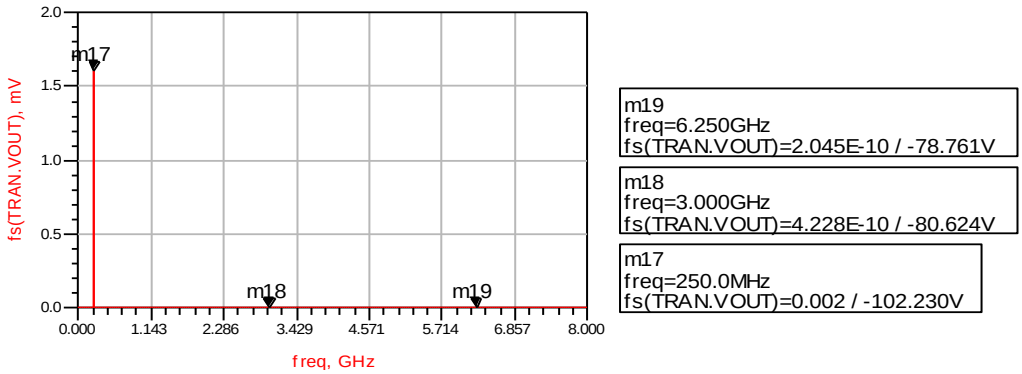


Figure 94: Fourier series

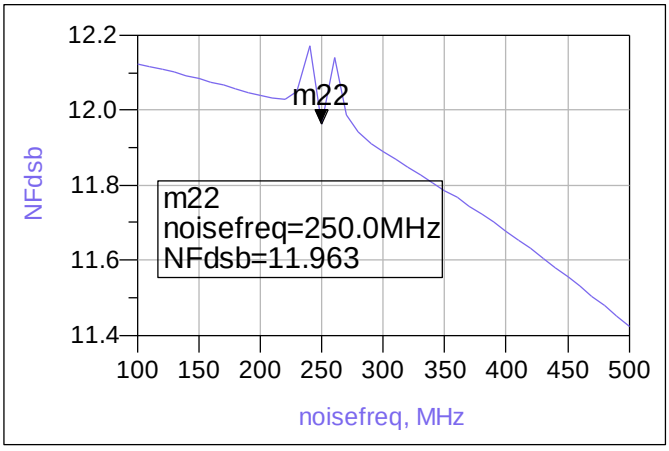


Figure 95: NF-DSB

7.3. The design of gilbert mixer using Cadence with 180n technology

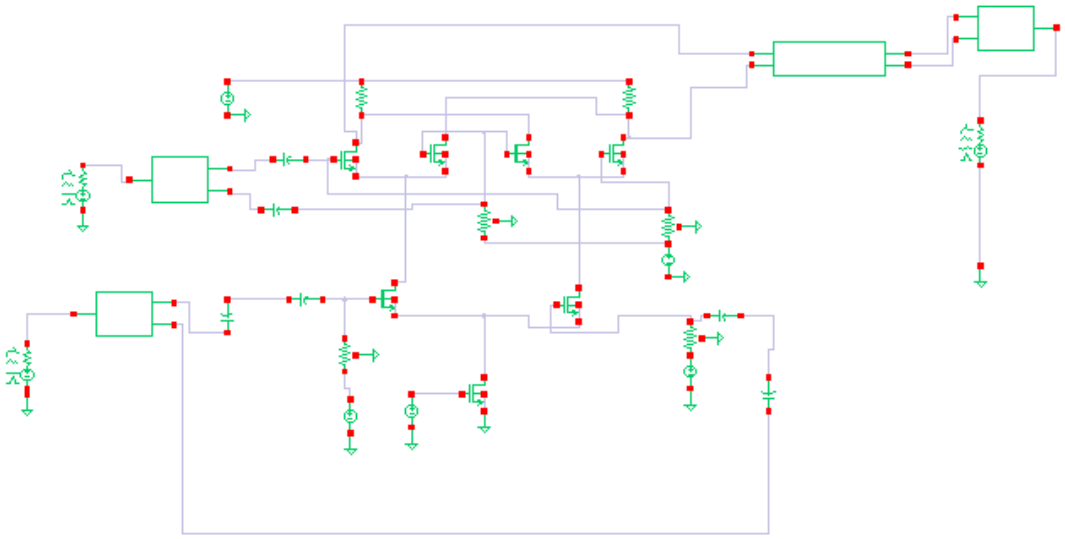


Figure 96: schematic

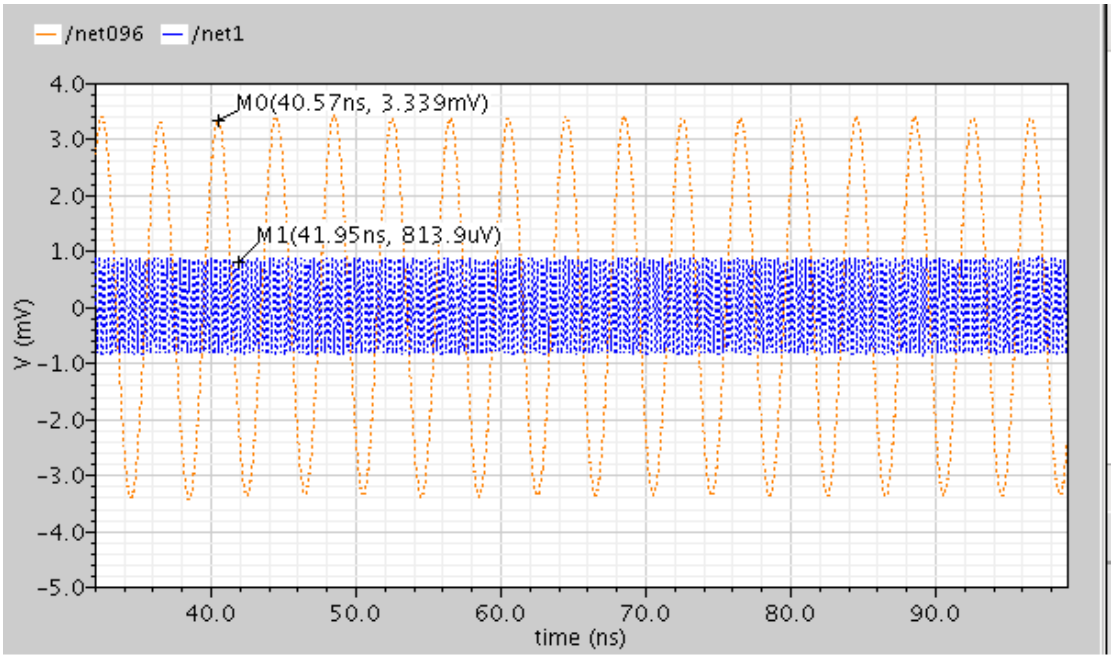


Figure 97: transient simulation

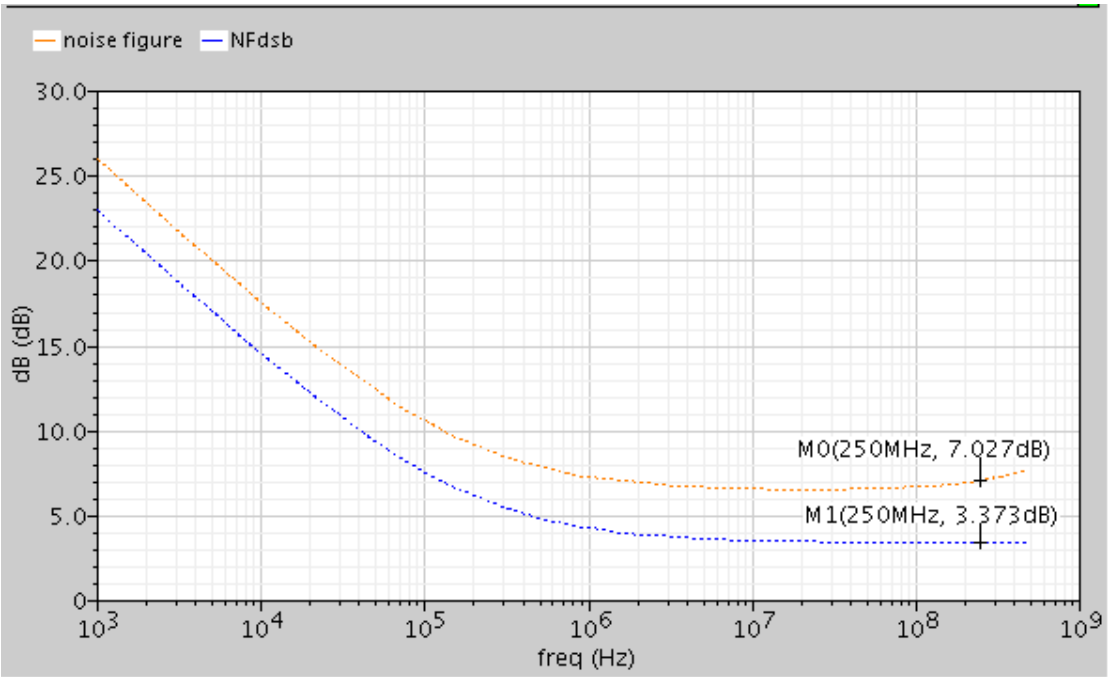


Figure 98: noise figure

References

1- Domine Leenaerts, Johan van der Tang and Cicero S. Vaucher, CIRCUIT DESIGN FOR RF TRANSCEIVERS,CH4 , 2003 .
2-Behazd Razavi, RF Microelectronics, CH6,1998 .
3- *J P Silver*, E-mail: john@rfic.co.uk,www.rfic.co.uk, Gilbert Cell Mixer Design Tutorial

Chapter -8
8. Oscillator

8.1. Oscillators:

- Are electronic circuits that generate an output signal without the necessity of an input signal. The output voltage can be either sinusoidal or no sinusoidal, depending on the type of oscillator.
- Different types of oscillators produce various types of outputs including sine waves, square waves, triangular waves, and saw tooth waves.

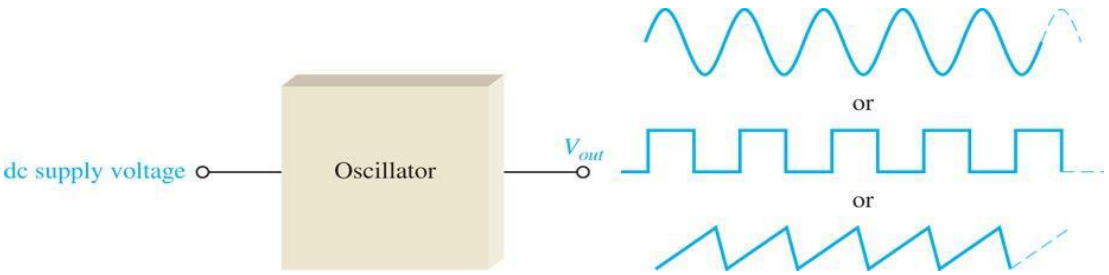


Figure 99: VCO output

8.2 Feedback Oscillators:

One type of oscillator is the feedback oscillator, which returns a Fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal.

After oscillations are started, the loop gain is maintained at 1.0 to Maintain oscillations.

A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation.

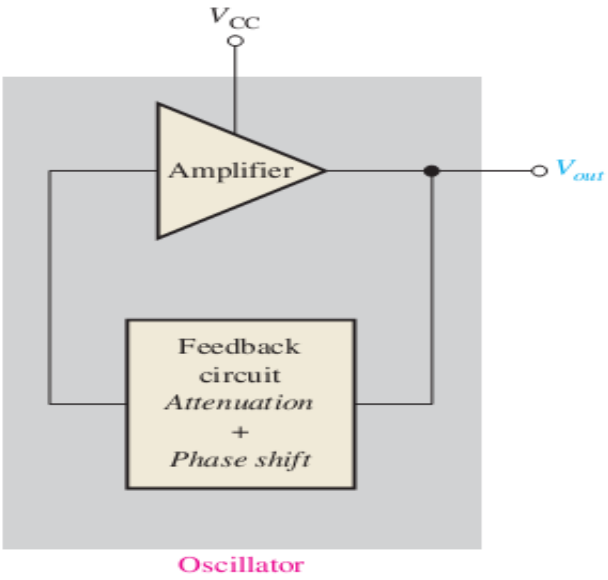


Figure 100: VCO structure

8.3 Positive Feedback:

In **positive feedback,** a portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a strengthening of the output signal.

This basic idea is illustrated in the following figure:

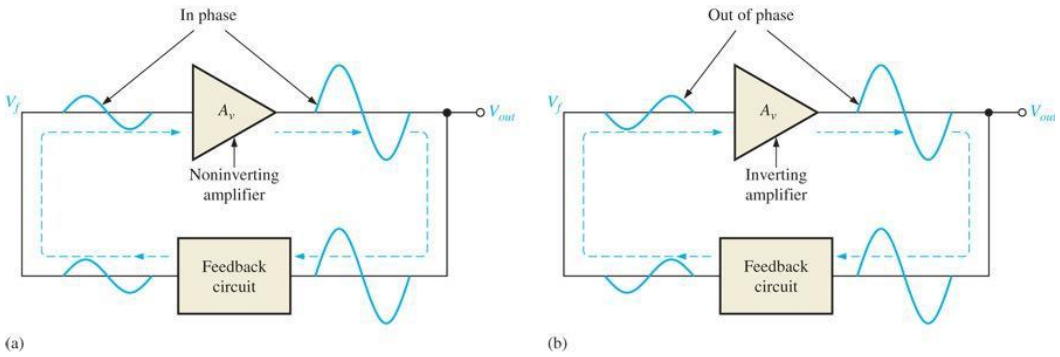


Figure 101: positive feedback produces the oscillation

In some types of amplifiers, the feedback circuit shifts the phase and an inverting amplifier is required to provide another phase shift so that there is no net phase shift.

8.4 Start-Up Conditions:

For oscillation to begin, the voltage gain around the positive feedback loop must be **greater than 1** so that the amplitude of the output can build up to a desired level.

The gain must then **decrease to 1** so that the output stays at the desired level and oscillation is sustained.

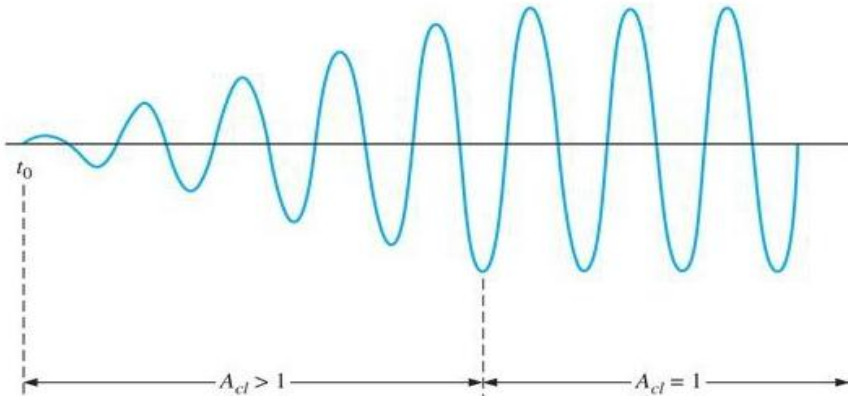


Figure 102: Start up

When oscillation starts at $\boldsymbol{t_0}$, the condition $\boldsymbol{A_{cl} > 1}$ causes the sinusoidal output voltage amplitude to build up to a desired level. Then $\boldsymbol{A_{cl}}$ decreases to 1 and maintains the desired amplitude.

8.5 The necessary conditions for steady-state oscillation:

1. The first condition is referred to as the "phase condition". This condition states that the total open loop phase shift must be k times 360 degrees, where k is an integer value including zero.

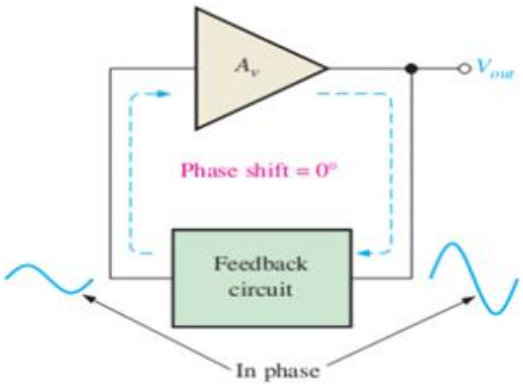


Figure 103: The phase shift around the loop is 0^0

2. The second condition is called the "gain condition" and the voltage gain,A_{cl}, around the closed feedback loop (loop gain) must equal 1 (unity).

The voltage gain around the closed feedback loop,A_{cl} , is the product of the amplifier gain, A_v, and the attenuation,B , of feedback circuit.

$$A_{cl} = A_v B$$

If a sinusoidal wave is the desired output, a loop gain greater than 1 will rapidly cause the output produce unacceptable distortion.

To avoid this, some form of gain control must be used to keep the loop gain at exactly 1 once oscillations have started.

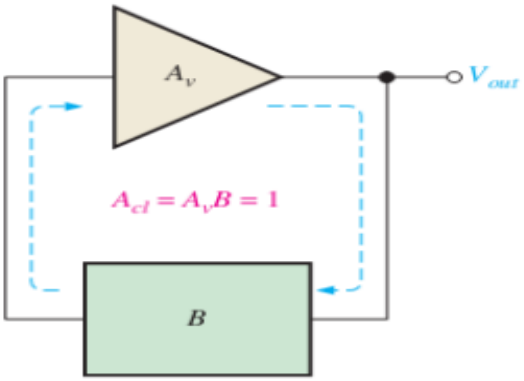
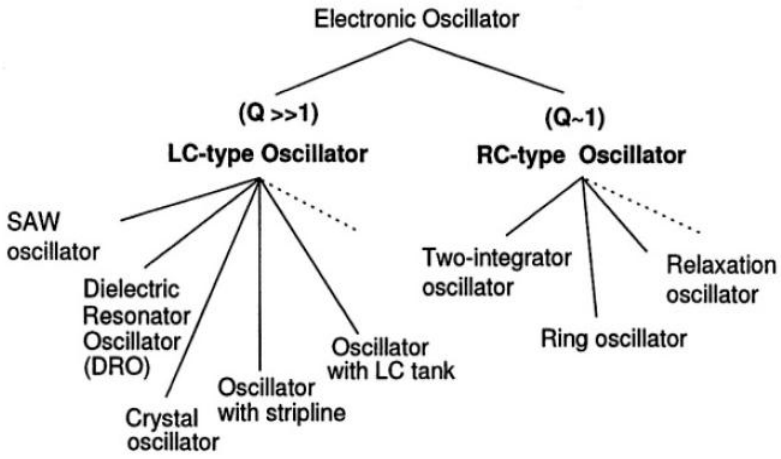


Figure 104 :The closed loop gain is 1.

8.2. Major Types of oscillator



Losses are always present, in both in LC and RC oscillators.

RC oscillators: no inductors are present. Only resistors (R) and capacitors(C) are used together with the active devices. "Quality factor" Q is close to unity for RC oscillators.

LC oscillators: are constructed using inductors (L) and capacitors (C), or passive devices which can be modeled with equivalent circuits using inductors and capacitors "Quality factor" Q is normally much larger than unity for LC -type oscillators

SAW oscillator's advantage is that it has very low phase noise at fixed frequencies through about 3 GHz. high quality factor (Q). SAW oscillators have several disadvantages, including a limited operating temperature range and limited tuning range. It widely used in wireless applications

8.3. LC VCO:

VCOs have become one of the most important components of today's communication systems. They are among the key building blocks of RF systems.

Its output frequency is stabilized or controlled with a Resonator.

In view of the continuous development and wide improvements in CMOS VCOs, it is now generally recognized that they still remain the most critical part of RF transceivers. Tuning range, and phase noise are the important characteristics of a VCO.

In general, low phase noise is preferred in the VCO.

LC oscillator is the most common type of oscillator used in RFIC design due to the reasons mentioned above. They can be designed for a fixed frequency and variable frequency operation (with the use of the varactor).

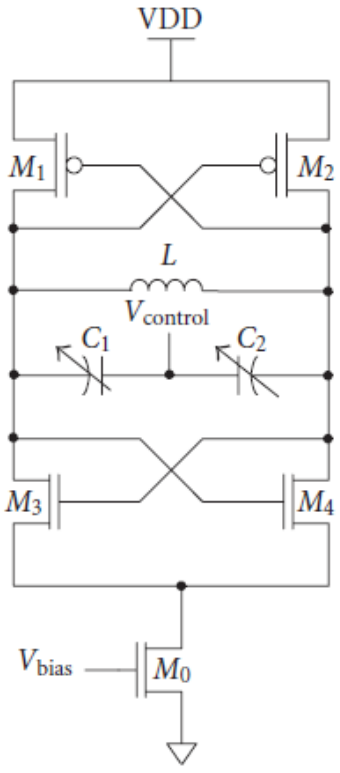


Figure 105 shows the standard LC-VCO design.

The Figure shows the standard LC-VCO design. The implemented VCO uses a complementary cross-coupled topology.

It consists double crossed coupled (NMOS & PMOS) , resonant circuit that feeds back signal to the input and nMOS current source.

The oscillator starts oscillating, usually by noise. Noise components contributed by the oscillator's elements (as well as supply and substrate), there are other sources of noise resulting from the losses in nonideal passive elements (inductors and varactors).Any noise in the circuit gets amplified and the output voltage begins to increase due to the positive feedback.

8.3.1 LC tank circuit of VCO:

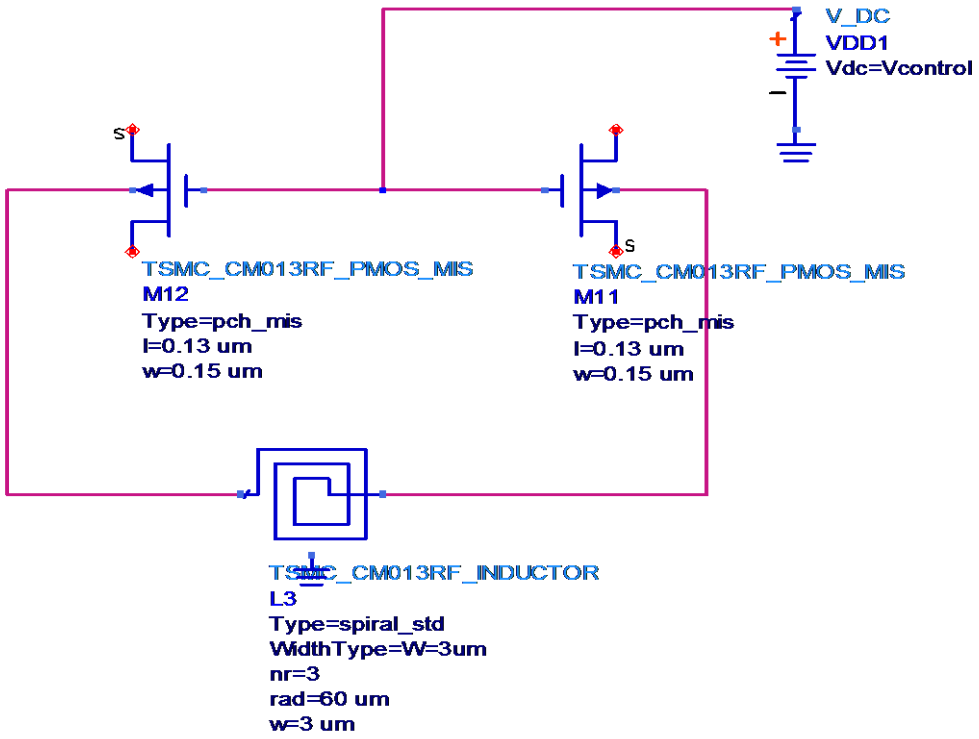


Figure 106:LC tank of the oscillator

The LC tank will filters out signals at frequencies other than the frequency at which the tank resonates. Therefore only the oscillation frequency is present at the oscillator output due to its band pass characteristics.

LC tank act as a resonator to control and tune the output frequency.

8.3.2 Capacitor:

Varactor (variable capacitance) or inductor can be used In order to tune the output frequency, which by tuning that the oscillation frequency will be tuned. This is according to the following equation:

$$\mathbf{f_{osc}} = \frac{\mathbf{1}}{\mathbf{2\pi\sqrt{L_{tank}C_{tank}}}}$$

Changing in the inductor mean change in number of turns or changing in its radius or changing in its width and the result changing in its cross section area. So it is preferred to change in capacitor.

The MOS varactors (variable capacitance) are better than diodes as it is more linear and wider tuning range, lower resistance.

The MOS capacitor has a structure that is analogous to a parallel plate capacitor, with the drain, source unconnected and bulk of a PMOS transistor connected realizing one plate of the capacitor, while the polysilicon gate constituting the other.

Such this varactor is called Accumulation varactor.

For PMOS varactor: increasing the $V_{control}$ increase the voltage across the gate and this make the electron in the substrate to move to word the gate, this cause d to decrease

$$C = \frac{\varepsilon_0 A}{d}$$

So the capacitance increase and the result is decrease in output frequency.

The value of C_{max} is determined by the geometry of the varactor:

$$C_{max} = \frac{3.9.\varepsilon_{0}.W.L}{T_{ox}}.N$$

Where $\varepsilon_o = 8.84542 \times 10^{-12} F/m$
$T_{ox} = 9.6E^{-9} m$
N Number of gate fingers

The minimum value of the varactor is approximately given by:

$$C_{min} \approx C_{gdo}.W$$

Where $C_{gdo} = gate - drain\ capacitance$

$$= 9E^{-11}F/m$$

Q of the varactor by using the following approximate expression:

$$Q_{mos} = \frac{12\,.K_{p.}(V_{gs} - |V_T|)}{\omega.C_{ox}.L^2}$$

$$K_p = 13.9E^{-3}.3.59E^{-3} = 48uA/V^2$$

$$\omega = 2\pi f$$

$$C_{ox}\ or\ \frac{3.9.\varepsilon_o}{T_{ox}} = \frac{3.9\times8.84542\times10^{-12}}{9.6E^{-9}} = 3.59E^{-3}F/m^2$$

To maximize the Q of the varactor we need to keep L as short as possible.

8.3.2 The crossed coupled

The NMOS and PMOS cross-coupled transistors are used in the positive feedback to provide negative resistance to cancel this loss.

This negative resistance makes the circuit unstable as a result the oscillation starts, with the increase in the oscillation amplitude, the –Gm drops until it gets equal to the parasitic resistors in the circuit which will limit the oscillation amplitude of the oscillator.

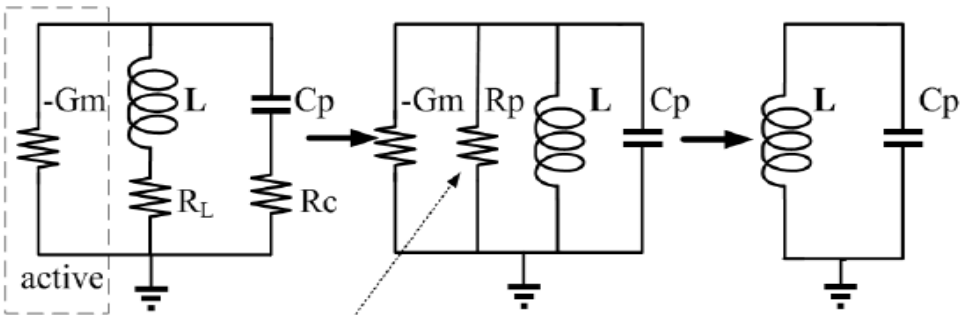


Figure 107: compensating the losses of LC tank using the crossed coupled

The parallel resistance *R* models the loss due to the metal resistance in the inductor and the varactor.

The double crossed coupled configuration has some advantages:

1) With the addition of the crossed coupled, it is possible to compensate the loss of the resonant circuit with less current consumption.

2) The complementary cross-coupled oscillator shows a better phase noise performance when compared to the NMOS- or PMO only cross-coupled oscillators for the same supply voltage and bias current. Using both ratio between nmos and pmos transistor help minimizing the 1/f noise.

Another way to reduce 1/f noise is to increase the size of CMOS devices

3) A double cross-coupled provides twice the differentia swing of that in a n-MOS only structure due to the pMOS
pair, for the same bias current. The total negative resistance of the CMOS pair can be expressed as a parallel combination of the NMOS an PMOS pair's negative resistance, R_N andR_P

$$\boldsymbol{R_{negative} = R_n \,/\!/\, R_P = -\frac{2}{G_{mn} + G_{mp}}}$$

The negative transconductance of the parallel cross- couple pair is given by the relation

$$\boldsymbol{G_m = (\frac{G_{mn} + G_{mp}}{2})}$$

In order to maintain the symmetry of the oscillator Outputs G_{mn} should be equal to G_{mp}

$$G_{\mathrm{mn}} = \mu_{\mathrm{n}}.\mathrm{C_{ox}}.\frac{\mathrm{W}}{\mathrm{L}}.(\mathrm{V_{GS}} - \mathrm{V_{th}})$$

$$G_{\mathrm{mp}} = \mu_{\mathrm{p}}.\mathrm{C_{ox}}.\frac{\mathrm{W}}{\mathrm{L}}.(\mathrm{V_{GS}} - \mathrm{V_{th}})$$

An initial loop gain magnitude greater than one is typically designed and then nonlinearities in the amplifier will reduce the magnitude to exactly one in steady state operation.

Startup requires:

$$G_m R_P > 1$$

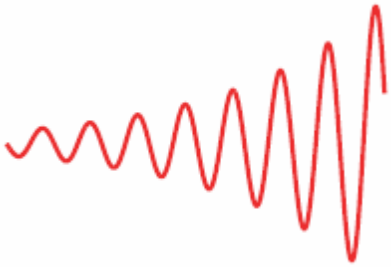


Figure 108 : start up oscillation

For oscillation:

$$G_m R_p = 1$$

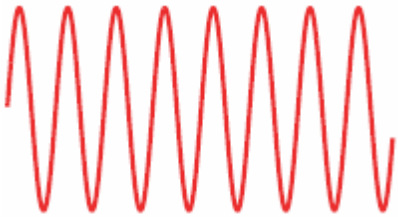


Figure 109: oscillation

8.4 Tail current

A tail current device is added to the *VCO* circuit, in order to have a greater control over the oscillator's output voltage swing. A change in the tail current modifies the negative resistance presented to the tank circuit, and hence modifying the oscillator output voltage swing.

The tail current provides oscillation amplitude control but it adds noise.

8.5 Phase noise

Phase noise is an important characteristic of any oscillator and an important performance metric of RF VCOs Characterized in frequency domain; it is an important indicator of an oscillator's frequency stability.

Ideal oscillator in time domain, the output voltage of any oscillator can be quantified as

$$V_{out}(t) = Asin(\omega_0 t + \phi)$$

With *A* the amplitude, ω_0 the frequency and ϕ the fixed phase.

In the frequency domain, this is equivalent to a discrete spectral line with height at angular frequency

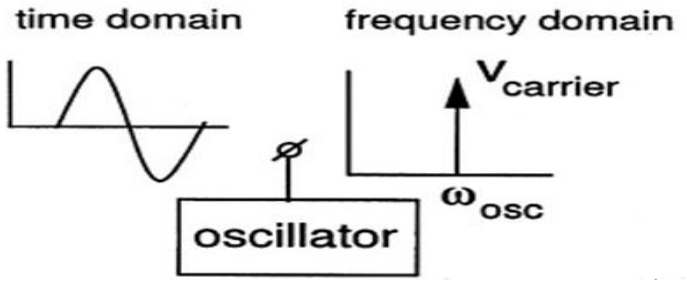


Figure 110: ideal output for oscillator

However, in actuality, real world oscillators are implemented using inherently noisy devices. The output of a real oscillator can be better expressed as:

$$V_{out}(t) = Asin(\omega_0 t + \phi(t))$$

Where *A(t)* and φ (*t*) are functions of time

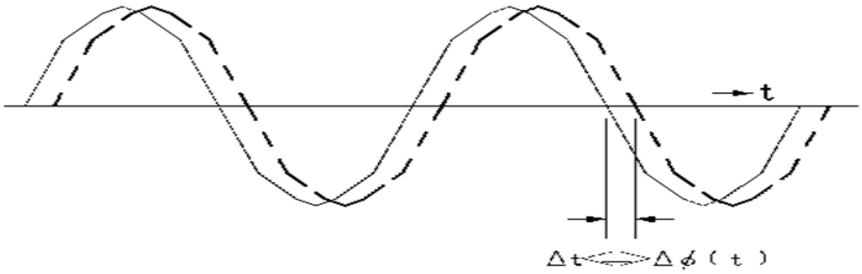


Figure 111: phase noise representation in time domain

The frequency spectrum has power distributed around the desired oscillation frequency ω_o ,In addition to power located at harmonic frequency. In other word the frequency spectrum of the output voltage, V_{out} , consists of noise sidebands in proximity of the oscillation frequency, ω_0. This phenomenon is called the *phase noise*.

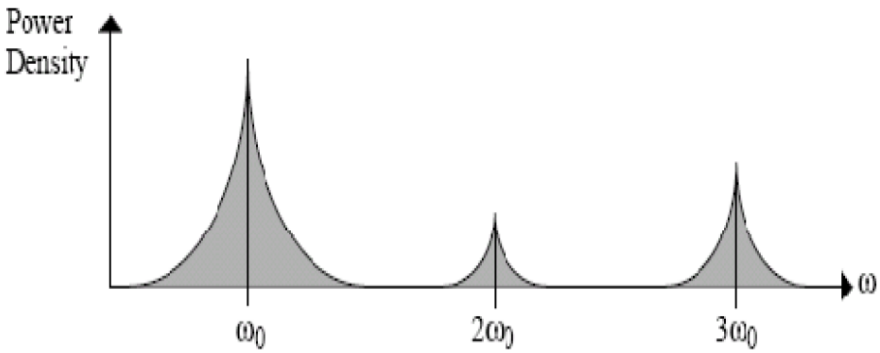


Figure 112: output spectrum with phase noise

The phase noise is computed as the ratio of the noise power in the side band to the carrier power. It is calculated in dBc/Hz and expressed as:

$$L(\Delta\omega) = 10 * log\left(\frac{noise\ power\ in\ unit\ bandwidth\ at\ frequency,\omega_o+\Delta\omega}{carrier\ power\ at\ frequency\ \omega_o}\right)$$

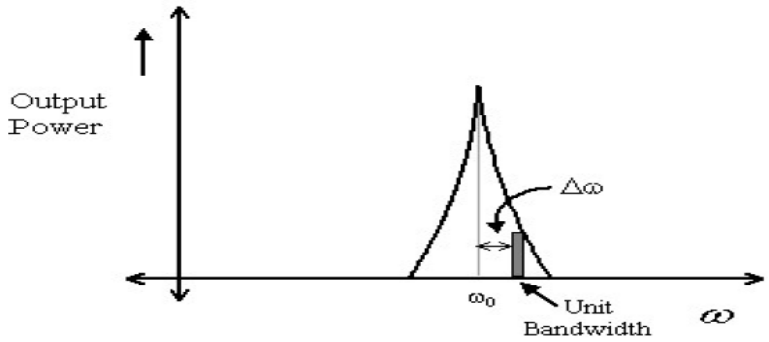


Figure 113: Illustration of the phase noise in the oscillator's output spectrum

In general, the phase noise sidebands of oscillators can be divided into three regions with different slopes as indicated in the following figure

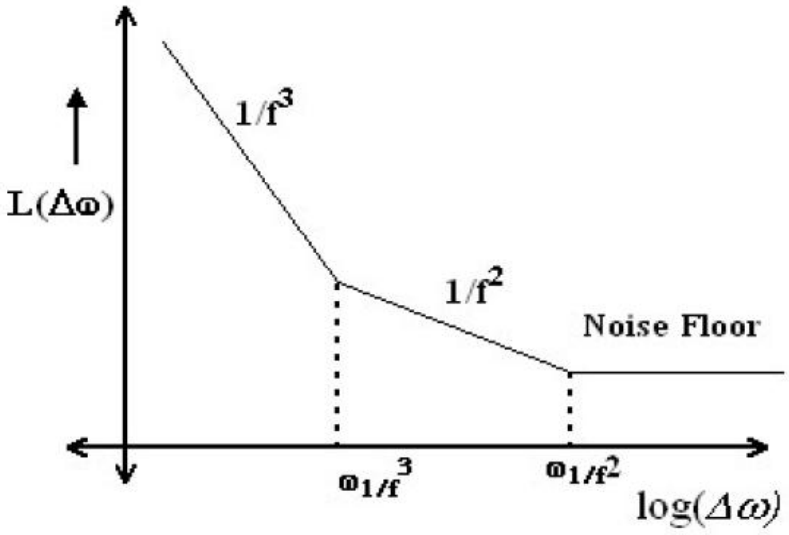


Figure 114: Typical phase noise plot for an oscillator

The lowest frequency is dominated by *flicker noise(1/f)* which is device flicker noise . This has a slope of $1/f^3$. The region, with a slope $1/f^2$, normally the biggest part of the oscillator sideband and called *White FM noise.*

White PM noise is simply white noise that mixes up to the oscillation frequency. This has the typical flat white- noise floor.

Chapter 9
9. VCO design implementation:

We should simulate VCO using the ADS tool by employing the models of transistors 0.13µm CMOS technology.

9.4.1 Schematic of the VCO:

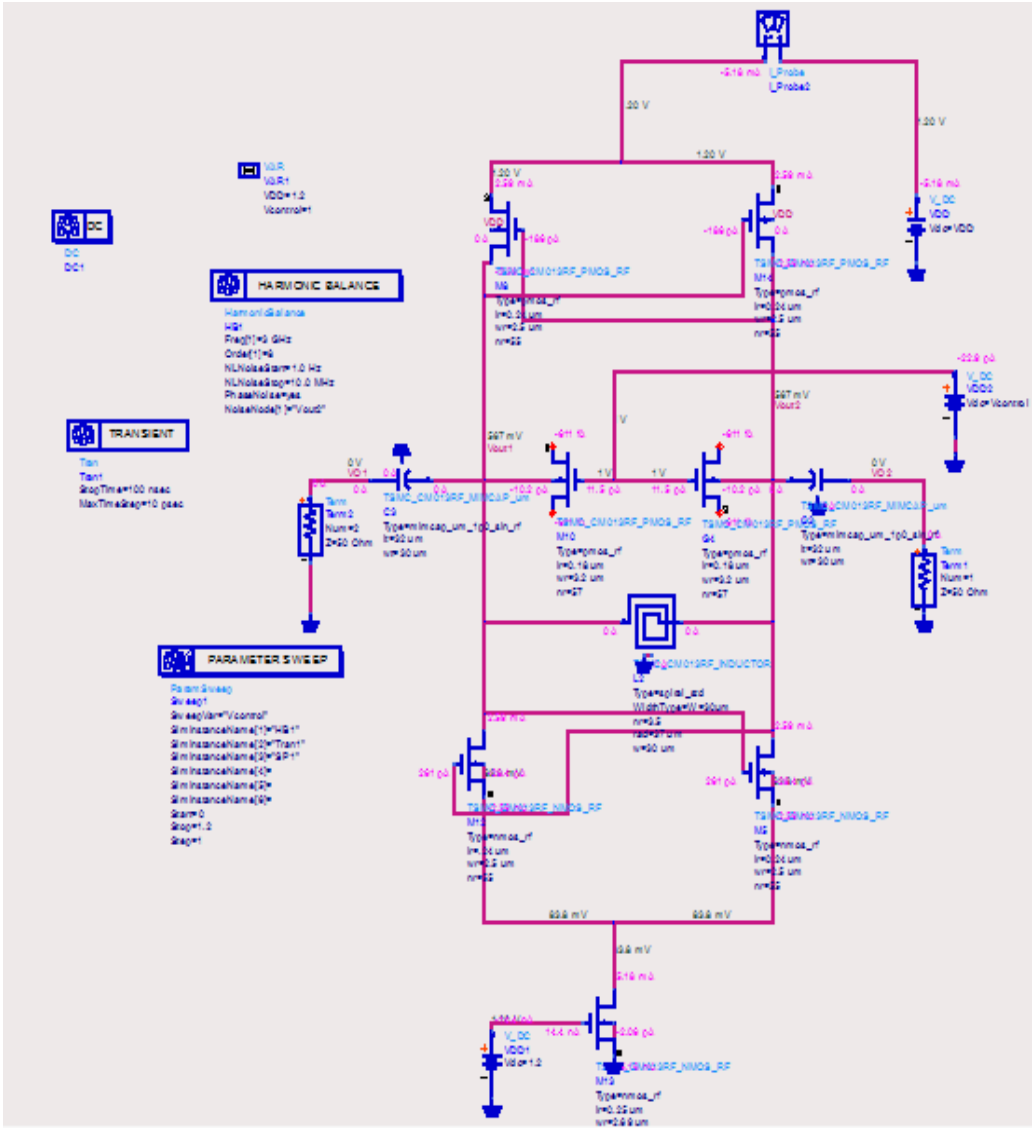


Figure 115: VCO schematic in ADS

9.4.2 simulation result:

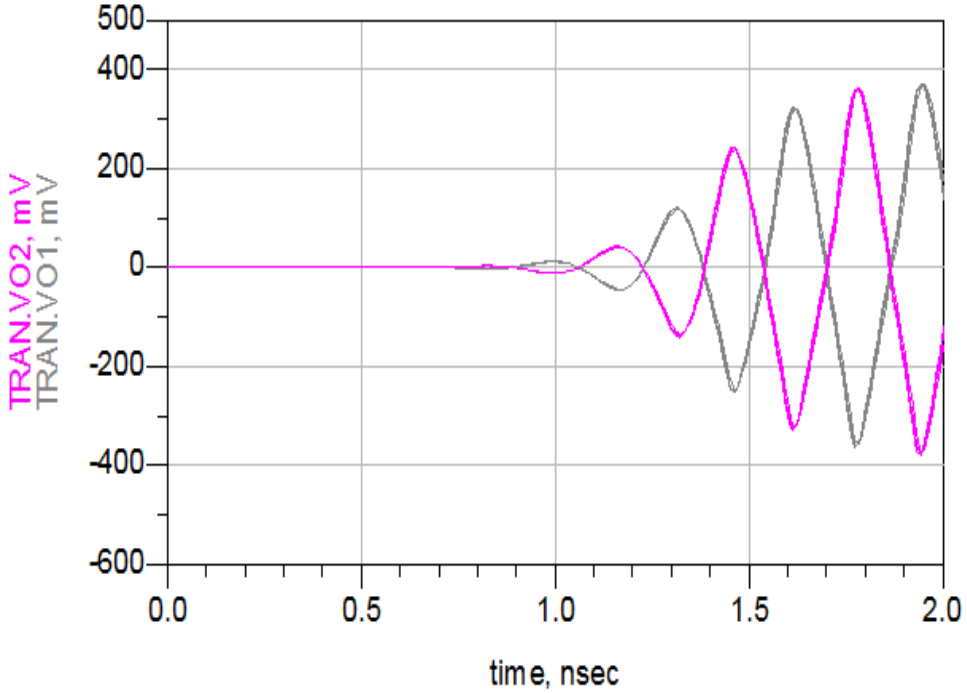


Figure 116: start up oscillation

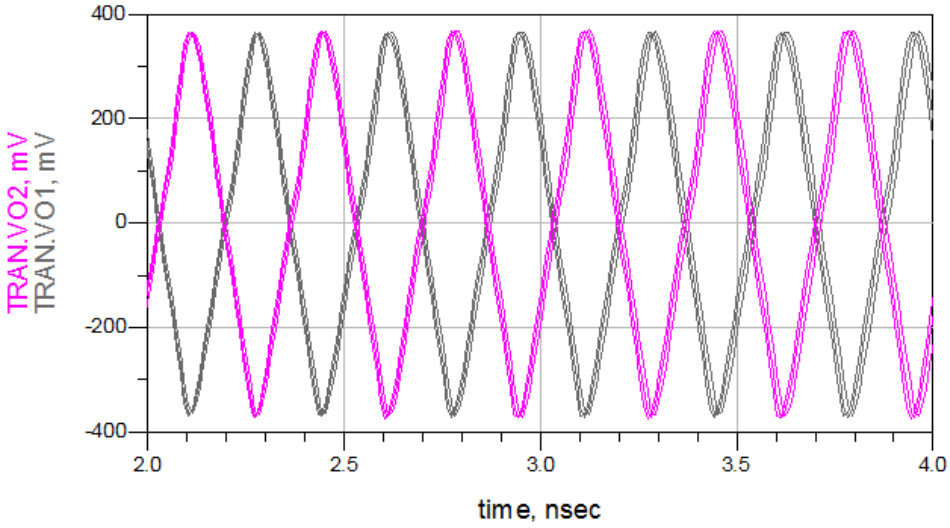


Figure 117: steady state oscillation

harm index	HB.freq		
	...trol=0.000	...trol=1.000	...trol=1.200
0	0.0000 Hz	0.0000 Hz	0.0000 Hz
1	3.009 GHz	3.000 GHz	2.989 GHz
2	6.018 GHz	6.000 GHz	5.979 GHz
3	9.028 GHz	9.000 GHz	8.968 GHz
4	12.04 GHz	12.00 GHz	11.96 GHz
5	15.05 GHz	15.00 GHz	14.95 GHz
6	18.06 GHz	18.00 GHz	17.94 GHz
7	21.06 GHz	21.00 GHz	20.92 GHz
8	24.07 GHz	24.00 GHz	23.91 GHz

Figure 118: The frequencies of the oscillation with the control voltage

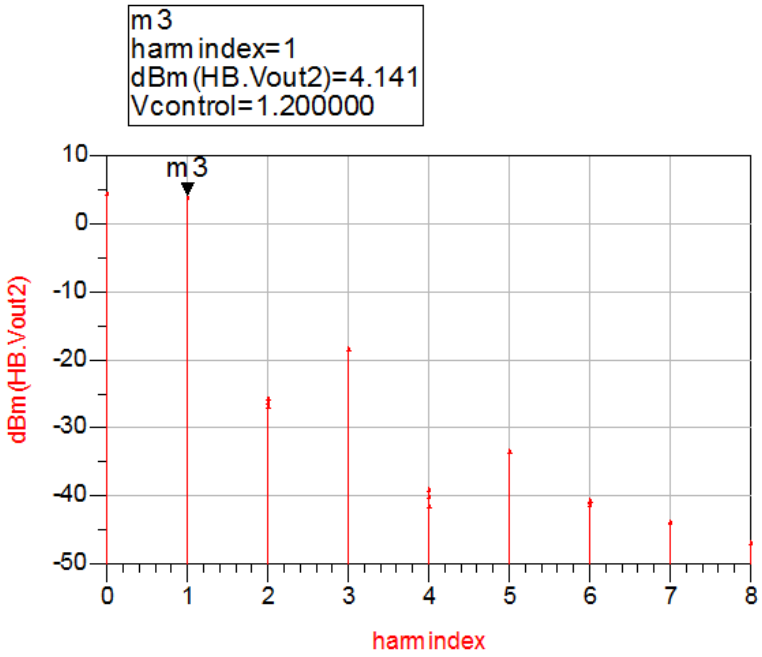


Figure 119: The output Power

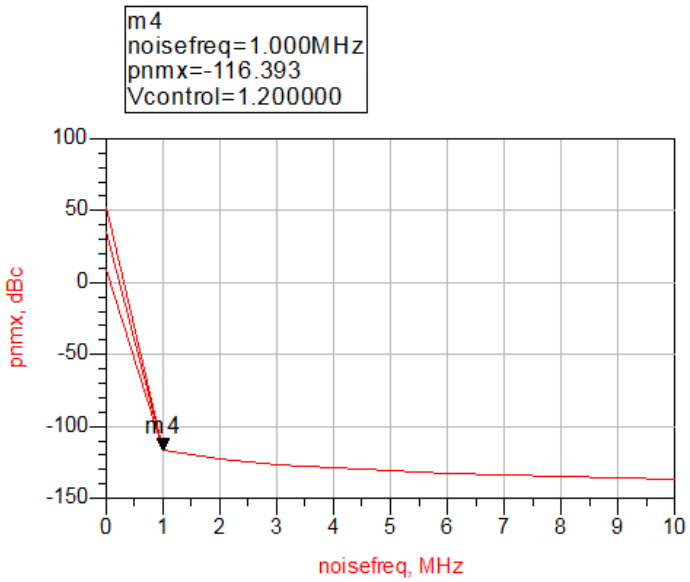


Figure 120: The phase noise in VCO

freq	DC.I_Probe2.i
0.0000 Hz	-4.767 mA

Figure 121: DC current

9.5 final results:

Table 6: VCO final results

Parameter	**Specification**
Centre frequency	3GHz
Band width	21MHz
Phase noise	-116.747 dBc/HZ at 1MHz
Output power	4.007dBm
DC Current	4.767 mA
Tuning voltage	0 – 1.2 V

9.6 VCO design in Cadence:

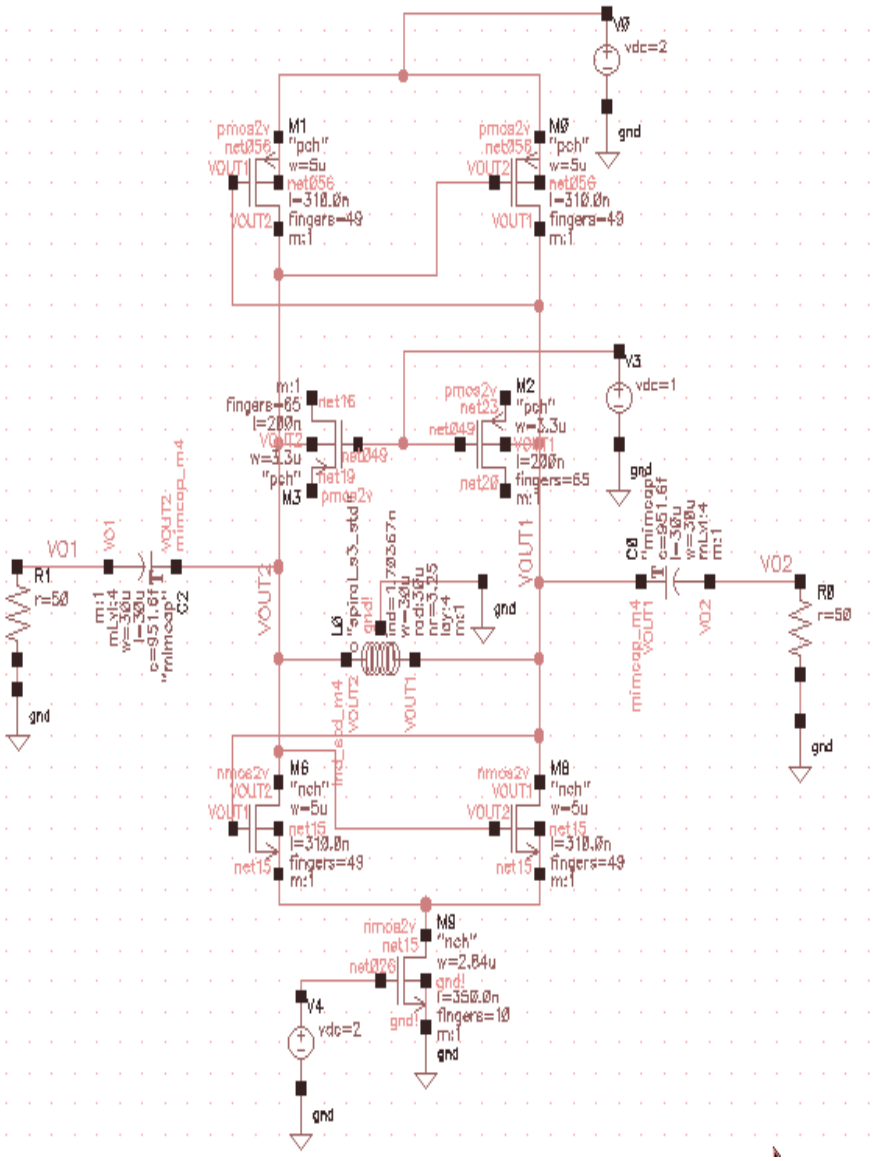


Figure 122: VCO schematic in cadence

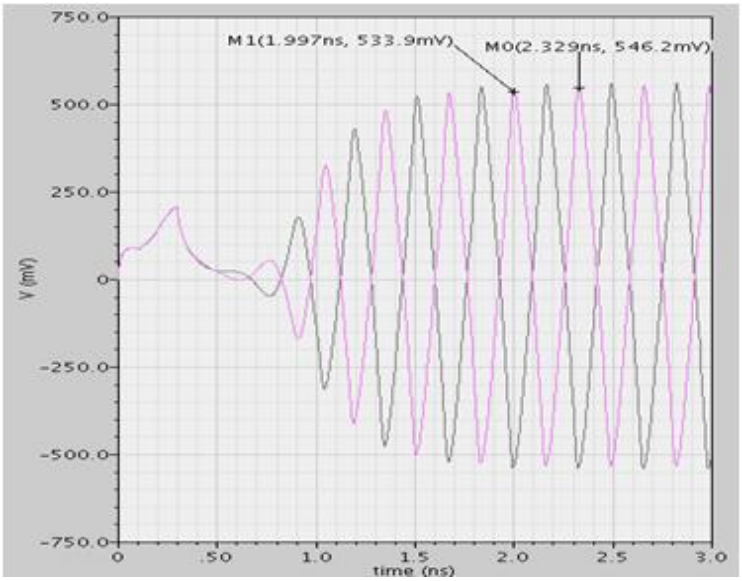


Figure 123: start up and steady state oscillation

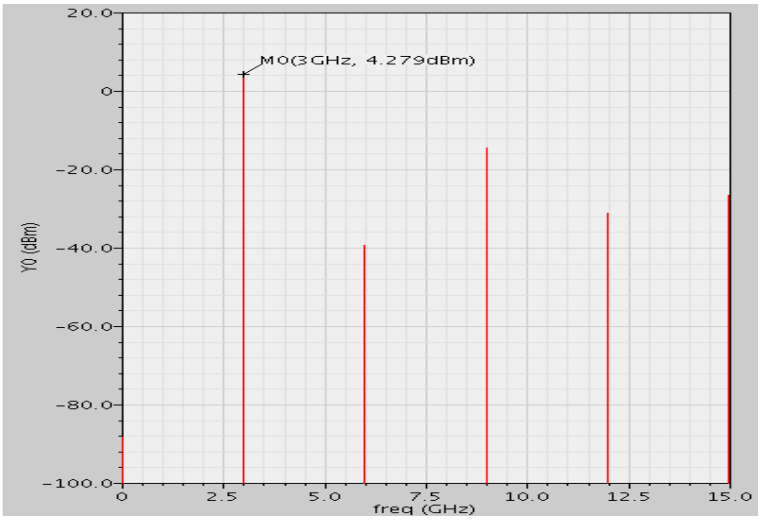


Figure 124: output power

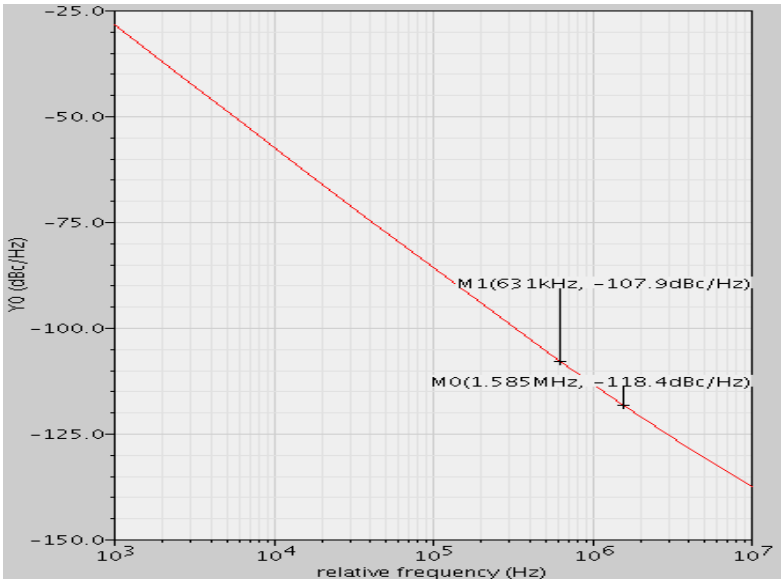


Figure 125: phase noise

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