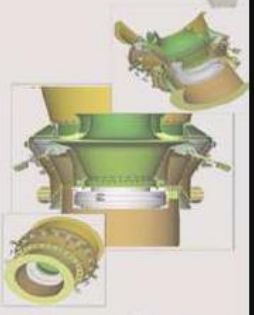
Faculty of Engineering - Cairo University
Credit Hour System Programs

Communication and Computer Engineering
(CCE)

Graduation Project Report
Spring 2013



Digital TV Tuner Front End Design

“Part A : LNA and Mixer “

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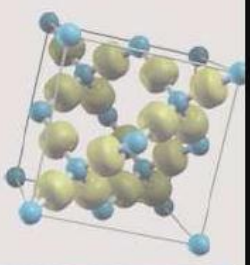

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Acknowledgement

The success and final outcome of this project required a lot of guidance and assistance from many people. So, we would like to express our very great appreciation to Dr. Faisal El-Seddek for his guidance during the project, his efforts to make us learn how to make an RF Design. He also provided us lots of papers and researches that helped us to figure out main RF techniques without it our Design can't be made.

We would like to thank also Dr. Mohamed Abou-Dina for his support during our first steps in the project. He made us learn some analogue basic concepts that helped us in our circuit design. He also made some Tutorials to learn how to use cadence in an efficient way. Also , we can't forget how the Academic Assistants , specially Eng. Mohamed el Sawaby, in our Faculty helped us to install Calibre which is used in our Layout Design.

Finally, we would like to thank everyone who had helped and encouraged us to finish this hard Task Project during these few months. This Project belongs to all of you.

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Executive Summary

In this report, we are going to discuss how to make an RF Design of an LNA and a Mixer for a wide band TV-Tuner. We are going to focus on each block, the main challenges in each block and several designs will be proposed, then based on the results and the specifications desired we are going to compromise between the Designs to figure out our Final Design.

After settling on the design, we are going to provide a layout design of the schematic. We are going to magnify the main layout challenges and how to produce an effective layout, similar to the ideal circuit before making the layout.

To Conclude our Work , RF Design isn't an easy job, due to the high Frequency which we deal with , and also the Parasitics associated with the RF Components . Also, wide band design is a challenging design, in which there are many factors that dominate the Frequency response of the design. To make a good design , all factors must be taken into consideration and their effects must be well known and defined .

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1 Introduction

Wide Band Wireless Communication has been an essential Part of our life. On the very beginning, it was just utilized to send data through the wireless channel, then voice, then images then Digital video Broadcasting. These are only examples from the desired signal which is sent over the wireless channel. Due to that, there exist many wireless channels. The ITU has divided then total bandwidth used into small areas of Bandwidth in which only a certain type of data is being transmitted and under some specific conditions.

Therefore, each wireless communication system now has its system Requirements. Depending on different requirements on the transmission speed and operating range, standards are defined such that a unique communication channel could be dealt with for the same Application [Type of data transmitted]. There are different standards we can choose when dealing with the wireless channel but in this report, we are going to Focus on the Digital Video Broadcast since we are designing an LNA and a Mixer for a TV-Tuner.

1.1 A Brief of TV Broadcast History

1.1.1 Difference between analog TV and Digital TV

There exist various analog/digital terrestrial or cable TV standards. The Digital standards differ from the analog ones depending on many factors. The Main Difference between them is that the digital Sends audio and video after being digitized over a digital channel. To clarify the main differences, let us consider the following aspects:

- ✓ Digital Transmission is more immune to noise
- ✓ digital television is more flexible and efficient than analog television
- ✓ digital channels take up less bandwidth
- ✓ Digital television may also permit special services, including the multiplexing of signals

Now it is clear that the world is directed to the Digital Television, that's why we are going to some of the main Standards of Digital Television

1.1.2 Digital TV Broadcasting

It is a new service that represents an evolution in television technology. Many countries are replacing broadcast analog television with digital television to allow other uses of the television radio spectrum. Several regions of the world are in different stages of adaptation and are implementing different broadcasting standards. There are four different digital television **terrestrial** broadcasting

1. Advanced Television System Committee (ATSC)

- ✓ Adapted in USA and other countries

2. Digital Video Broadcasting-Terrestrial (DVB-T)

- ✓ Adapted in Europe, Australia and New Zealand.

3. Terrestrial Integrated Services Digital Broadcasting (ISDB-T)

- ✓ Adopted in Japan and most of South America

4. Digital Terrestrial Multimedia Broadcasting (DTMB)

- ✓ adopted in the People's Republic of China (PRC)

All these Standards, differs from each other depending on the wireless channel they work in. the changes are in the PHY-Layer (Modulation, encoding, decoding …. etc) and also the overall system requirements. There are also other systems in the Digital Video Broadcast like : 1- Digital Video Broadcast Cable (DVB-C) and 2- Digital Video Broadcast Satellite (DVB-S).

1.2 Generic TV- Tuner Receiver

Now it's clear that there are many standards for DTV, but there are main blocks that such each system must have it in its receiving structure. We are going now to discuss a brief summary for each block:

1) **LNA :**
   - ✓ Low-noise amplifier (LNA) is an electronic amplifier used to amplify possibly very weak signals (for example, captured by an antenna). It is usually located very close to the detection device to reduce losses in the feed-line
   - ✓ Main challenge in LNA is to achieve higher with very low **NOISE FIGURE** because the noise figure of the first block affects 1 to 1 the total noise figure of the system.
   - ✓ Another challenge to achieve a reliable linearity with higher gain.
   - ✓ Also, we have to make input impedance matching to maximize the power.
   - ✓ LNA can be by passed if the signal to noise (SNR) is acceptable

2) Tunable Band Pass RF/Filter :

- ✓ It's main task is to select the working band
- ✓ Due to its functionality at high frequency , it's hard to design a high selective filter (High Q) , so some unwanted harmonics will pass throw it , which will cause problems during down conversion (mixing)
- ✓ One important job of RF/Filter and the Mixer is the harmonic rejection.

3) Mixer :

- ✓ It's main function is to convert the RF signal into the required working frequency
- ✓ There is 2 types of down conversion:
    1. Zero IF (intermediate frequency where IF=LO-RF):
        - Easy to achieve higher image rejection ratio
        - But problems with noise at DC (example, Flicker noise =1/f)
    2. Low IF :
        - No problem of noise at DC
        - But we have to use complex techniques to improve the image rejection ratio , for example :
            I. Using Hartley architecture
            II. Using weaver architecture
            III. Using complex polyphase filter after the mixer
- ✓ Concerning the harmonic rejection, different techniques could be used :
    1. Up conversion➔ using high frequency mixer , so that the harmonics of the mixer is out of the band

2. Using a complex mixer(negative frequency) which will suppress some harmonics of the mixer
3. Using double quadrature mixer (same frequency with different phases)

4) Frequency Synthesizer

- ✓ The goal is to generate the required local oscillator , and there is 3 different ways :
  - Use different crystal for each frequency , which is not practical
  - Use a single crystal oscillator and use a division by n to achieve required frequency
  - The best and most efficient way is to use a PLL
    - Using negative feedback with the VCO to achieve the stable required Local oscillator.

5) Channel select filter :

- ✓ Select the required channel and improve image rejection ratio
- ✓ TRADE OFF :
  - ➢ User higher LO will relieve the channel select filter but will push us to make a high selective RF/Filter , which is very hard and not practical.

6) VGA :

- ✓ Its main goal is to provide different gain steps to the signal, so that the level of the input signal to the ADC is acceptable.

7) ADC :

- ✓ Convert the received signal to Xbits digital signal depending on the requirements

1.3 Example of TV-Tuner Receiver architecture

In the following section, we are going to discuss an already Designed TV-Tuner Receiver. We are going to focus on the main aspects that define the system, how the signal is being processed till the baseband and how the Noise and signal images are being suppressed. In the Following (Figure 1.1) we can see the main architecture of a Cable TV-Tuner Receiver.

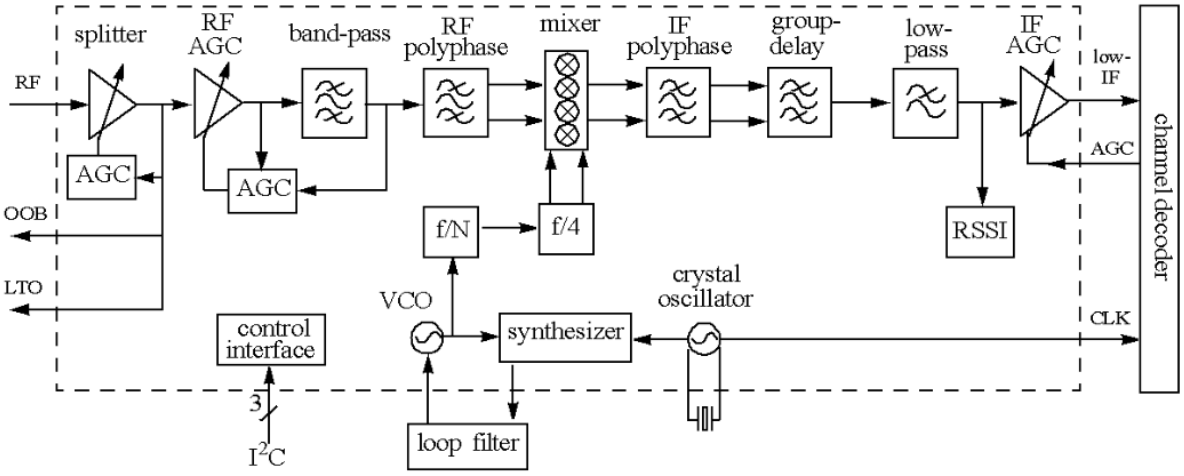


Figure 1.1 [12] Cable TV Tuner Receiver architecture

As a general overview, this architecture employs a single conversion, low-IF architecture with an acceptable input range 48-860MHz with a Power Consumption of 1.5W with a 3.3V supply. This Architecture is mainly characterized by a high image rejection by using a suitable Double quadrature mixer.

The First Blocks are a wideband splitter amplifier with adequate linearity with and Automatic Gain Control Feedback Circuit such that the gain is adjusted based on the received signal level compared to the Sensitivity of the receiver. After this Blocks , the signal is passed through a Band pass select Filter to increase the ability of image rejection of the Receiver .

Now, let's talk about the Intermediate Frequency (IF) Selection. The Zero IF may seem attractive but it has lots of drawbacks such that the DC components associated with the Received signal and the Flicker Noise near DC is high. So, A Low IF architecture is used (Channel Center Frequency at 4 MHz). The VCO Range frequency is between (1.8 Ghz –3.6Ghz) with Frequency Divider N=(2,4,8,16) and a Fixed Division by 4 . When Choosing IF lower, the image rejection is being removed by the Double Quadrature architecture and The Channel Select Filter is Being Relaxed. The Double quadrature architecture is implemented to reach Image rejection of 50dB instead of 40dB.

Now the Last stages of the Architecture, The group-delay equalizer corrects for the delay errors caused by the IF polyphase and low-pass filter, and is implemented as an active polyphase filter. The RSSI (Received Signal Strength Indication) measures the level of the wanted signal after the low-pass filter and then gives a feedback for the gain stage to adjust its gain such that the signal could be received at the correct level

1.4 The Essential Question

After having a general overview on the TV Tuner Receiver architectures and specifications, what will be our main goal during This Report? During our work, our main task will be how to make a challenging design for a wideband Low Noise Amplifier (LNA) and a Mixer for a wide Band TV-Tuner Receiver . In our design, the challenge is to achieve perfect specification using minimum power consumption. We have read lots of papers concerning LNA and Mixer's Design for TV Tuner and we have set specifications such we could achieve better system requirements with lower power consumption.

After we could reach a suitable Design, we will make a Layout Design for the circuit we reached. Layout rules and tricks will be shown in the Layout chapter but the main challenge is to maintain a compact size for the design, because when dealing with High Frequency, the wire length are large compared to the wavelength of the signal which make a huge parasitics and increase Signal Deterioration. Then, a suitable layout design has to be taken into consideration such we decrease the Signal Deterioration as much as we can .

1.5 Engineering Approach

Our main approach was to search and find papers that design LNAs and Mixers for TV-tuner. Our main goal was to learn wideband design techniques for LNA and various Mixers Topologies. Then after we have a nice background on the main architectures and techniques, we could compromise our design such we can reach the specifications we desire.

1.6 Road map to the sections of the report

Our Report is divided into 4 main sections. In Our First Section, we will discuss how to design a wideband LNA beginning from a narrowband LNA. This could be done by learning wide band design techniques like (gate inductive peaking, Resistor Feedback,… etc). Then we will discuss the main challenges that we faced during our Design. After That, the design results will be shown and a critical analysis will be made on the results to check what is the bottleneck in our Design.

In Our second section, we will discuss some Mixers Topologies indicating the main types of a mixer (passive and active, single Balanced and Double Balanced, Gilbert Cell Mechanism). Then we will talk about the main factors that will affect our Design such we could reach to the Required Specifications. Then, we will discuss our Design describing the circuit and the Results we reached.

In our Third Section, we will talk about how make a good layout for the LNA and the Mixer. We will discuss how to use Calibre for Design Rule Check (DRC) , and Layout Versus Schematics (LVS) ending up with the Parasitic Extraction(PEX) to test the Final Layout. We will discuss the main layout tricks and techniques used in RF Design for layout.

Finally, we will conclude our work, indicating what we have learned and the modifications that should be done such we can increase the performance of our design.

2 Wide Band LNA Design for TV-Tuner

In This Chapter we are going to discuss how to design a wideband LNA for a TV Tuner. We will begin by a narrow Band LNA Design, then we are going to explain main Wideband Design Techniques then we will end up by the steps of our design and then the Final Results.

2.1 LNA Main Parameters

As the first active stages of receivers, LNAs play a critical role in the overall performance of the system and their design is generally governed by the following Parameters:

a) **Noise Figure:**

The Noise Figure of the LNA adds 1:1 to the overall Noise figure of the system, therefore we have to design carefully the LNA such that its Noise figure is at minimum as possible (generally between 2 to 3 dB)

b) **Gain:**

The Gain of the LNA must be large enough to minimize the noise contribution of the blocks in the subsequent stages. But, here becomes a problem, higher gain makes the nonlinearity of the subsequent stages more appeared. Therefore, a suitable gain has to be chosen, and a mixer with high linearity requirement must be taken into consideration for better performance. For more details, let us consider the following figure (Figure 2.1, Razavi)

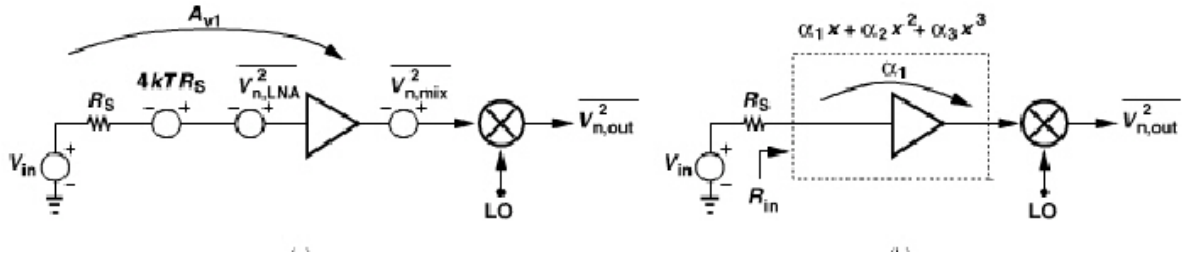


Figure 2.1 [1] the Effect of the LNA Gain on the Mixer NF and Linearity

The Total Noise Figure will be Shown in Equation 2.1

Noise Figure = $$\frac{N0}{G * Ni} = \frac{Av1^2\,(\,V_{nLNA}^2 + 4KTR_S\,) + V_{nin_{mix}}^2}{Av_1^2 * 4KTR_s} \qquad \text{Equation 2.1}$$

$$= NF_{LNA} + \frac{V_{nin_{mix}}^2}{A_{v1}^2} * \frac{1}{4kTR_s}$$

In Other words, the NF of the Second Stage is divided be the Gain of the First Stage , but let us now consider the IIP3 Total in Equation 2.2

$$\frac{1}{IIP3_{total}^2} = \frac{1}{IIP3_{LNA}^2} + \frac{\alpha_1^2}{IIP3_{Mixer}^2} \qquad \text{Equation 2.2}$$

Where α_1^1 Denotes the Voltage Gain of the LNA . Thus we can Conclude the higher Gain will improve the overall NF of the System but will degrades the IIP3 .

c) Input Return Loss:

In other words, it is called input matching. There are two main techniques used in Design , the First one is to make a Conjugate matching with the Antenna for maximizing the Power Transferred and the Second one is to make an input matching seeking for a minimum noise Figure. Deciding which technique will be used depends on the Application and the System Specifications that are required.

d) Linearity

Linearity is how higher order Harmonics and their Combinations are affected in the output with respect to the Main tone we want. Linearity in the LNA isn't a main problem because it is the first block and all the harmonics aren't amplified yet . But the LNA Gain affects the overall Linearity of the Following Blocks.

e) Power Dissipation

Power Dissipation limits the LNA from achieving the required Specifications . As more Current flows , the Trans-conductance (gm) increase which yields to the Increase of the Gain and respectively Decrease the Noise Figure. But , the Design isn't as easy as we see . Power Requirement becomes the Bottle-neck in some architecture in which we can't achieve what we desire

2.2 LNA Design and Analysis

For Designing an LNA for a TV Tuner , we need the LNA to work Correctly in the whole Band of the TV. The word wide Band means wide Band Matching , Gain, NF …etc. which means , all the specifications are being realized over the Band . But this isn't an easy Job. So, we started first to study and learn How to Design a Narrow Band LNA then after that we can use some RF Techniques to achieve the Specifications in the whole Band. In the Following Pages , we are going to discuss some LNA Topologies indicating the main Advantages and Disadvantages of Each one of them.

2.2.1 Common Source-LNA with Resistive Feedback

As we can see in (Figure 2.2 ,Razavi) , a Resistive Feedback between the Drain and the Gate exists . This makes Rin = $\frac{1}{gm_1}$, which can be used in wide band matching .

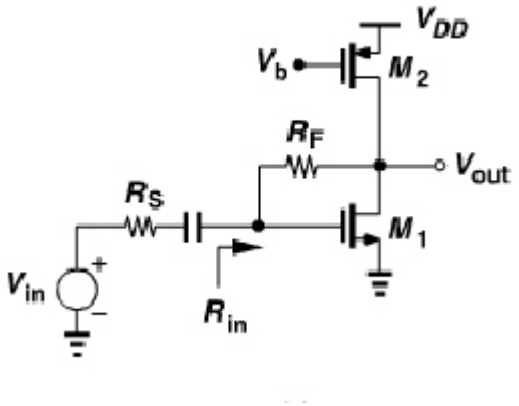


Figure 2.2 [1] 2 CS-LNA with Resistive Feedback

Now, let us calculate the Gain and the Noise Figure from(Figure 2.3)

Gain is Described in Equation 2.3**:**

$$Vx - gm_1 VxRf = Vout$$

$$\frac{Vout}{Vx} = 1 - gm_1 Rf = 1 - \frac{RF}{Rs}$$ Equation 2.3

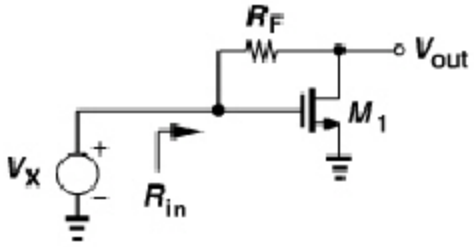


Figure 2.3 [1] Simplified Circuit for Calculations

In Practice, Rf is Much greater than Rs and the Voltage gain from Vin to Vout = 0.5

Then The Voltage Gain = $Av = 0.5 * \left(1 - \frac{Rf}{Rs}\right) \cong \frac{-RF}{Rs}$

Noise Figure Calculations:

First, let's Calculate Rout .As we can see in (Figure 2.4)

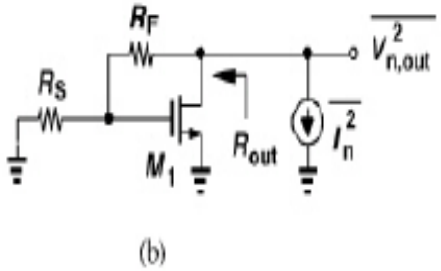


Figure 2.4[1] Calculating Rout

$$\boldsymbol{Rout} = \left[\frac{1}{gm_1}\left(1 + \frac{Rf}{Rs}\right)\right] || (Rf + Rs) =$$ Equation 2.4

$$0.5 * (Rf + Rs)$$

Now, Noise Figure Calculations can be calculated in Equation 2.6 :

$$V_{nout}^2 M1, M2 = 4KT\gamma(gm1 + gm2)\frac{(Rf + Rs)^2}{4}$$ Equation 2.5

$$NF = 1 + \frac{4RF}{Rs\left(1 - \frac{Rf}{Rs}\right)^2} + \frac{\gamma(gm1 + gm2)(Rf + Rs)^2}{Rs\left(1 - \frac{Rf}{Rs}\right)^2}$$ Equation 2.6

$$\approx 1 + \frac{4Rs}{Rf} + \gamma(gm1 + gm2)Rs$$, which exceeds 3dB

2.2.2 Common Gate LNA

What makes a (CG) LNA attractive for design is it's input impedance. Most of the (CG LNA's) input impedance is considered to be (1/gm) without using any addition resistances. This may be used in wide band matching and also we don't suffer from the resistive load headroom. Now let us consider a Simple CG LNA in the shown (Figure 2.5). The Gain equation is shown in (Equation 2.7)

$$Rin = \frac{1}{gm1} \rightarrow \quad gm1 = \frac{1}{Rs}$$

$$\frac{Vout}{Vx} = gm1 * R1 = \frac{R1}{Rs}$$

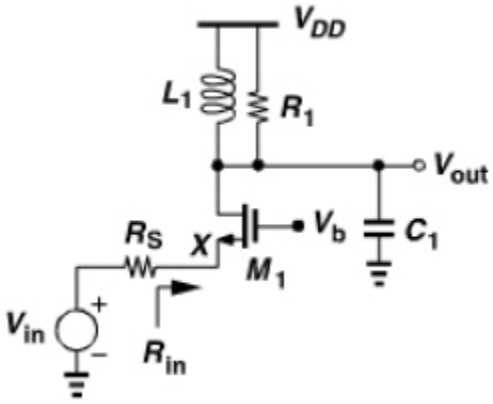


Figure 2.5[1] CG LNA with Inductive Load

Gain = $\frac{Vout}{Vin} = \frac{R1}{2Rs}$ Equation 2.7

It is clear that if we want to increase the Gain, the only way is to increase R1 which increases the headroom (trade-off) . Now let us calculate the **Noise Figure as in the following equations** :

Noise of M1 in output = $\frac{4KT\gamma}{gm}\left(\frac{R1}{Rs+\frac{1}{gm1}}\right)^2 = KT\gamma\frac{R1^2}{Rs}$

Noise Due to R1 in output = $4KTR_1$

Noise due to Input = $4KTR_s$

Then the Noise Figure

$$= \frac{Nout}{G * Ni} = \frac{KT\gamma \frac{R1^2}{Rs} + 4KTR_1}{\frac{R1}{2Rs} * 4KTR_S} + 1 \approx 1 + 4\frac{Rs}{R1} + \gamma$$ Equation 2.8

It is clear that the CG LNA can achieve better NF by increasing (gm) but with lower Gain.

2.3 Narrow Band LNA Design:

Now, we have a solid background on the Basic LNA topologies and the main design variables, so we began by designing a "Narrow **Band Common Source LNA with Degeneration** "

As we can see the schematic in (Figure 2.6), it is clear that there are two MOSFEts (M1 and M2) **M1** is responsible for the Gain Stage and **M2** is put for the isolation (reverse gain) from output to input.

Now, let us go to the Design Procedure

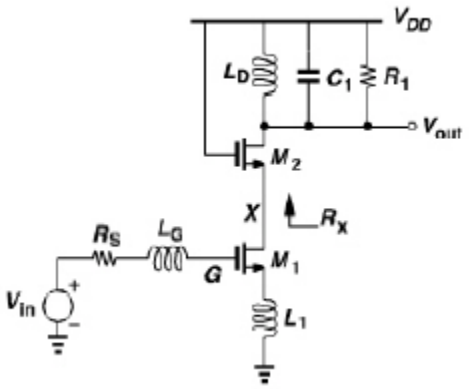


Figure 2.6 [1] CS - LNA with Degeneration

- L1 is assumed first
- $\frac{1}{(Lg+L1)(C_{gs1})} = w_0^2$, get Lg
- $Rs = L_1 * \frac{gm1}{C_{gs1}}$, by analysis , gm1 and cgs1 could be determined
- NF is inversly proportional to gm1
- $LD\ has\ to\ Resonate\ with\ R1\ , C1\ at\ w_0\ such\ that\ \ w_0 = \frac{1}{\sqrt{LD*C1}}$
- $R1\ Determines\ the\ Gain$, but we have to take into consideration the output resistance Parallel with R1 which lowers the Gain

The requirements of the Design are shown in the Following Table :

Gain	**15 dB**
NF	<3dB
IIP3	>0dBm
RF range	2.4G to 2.48G
S11	< -15 dB
Vdd	1.8V
C @ output	100f F

Table 2.1 narrow Band Specifications

The Schematic of the Design is shown in (Figure 2.7) (**Note** : The Resistance inserted with the inductor is due to the Non ideality , Calculated using a Suitable Quality Factor)

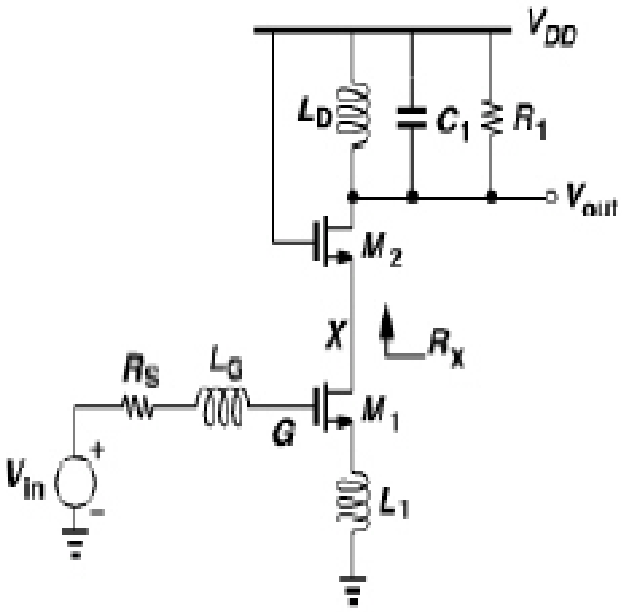


Figure 2.7[1] Schematic of CS-LNA with Degeneration

The Design Values are being shown in Table 2.2:

Design Parameter	Value
M1	W= 24u , L=300n, Multiplier=2
M2	W= 24 u , L=300n , Multiplier=2
L1	0.9 n H
Lg (Gate Indcutor)	11.8n H
Cgs	185f F
R1 (at Load)	80 ohms
Ld (at Load)	42.8n H

Table 2.2 Narrow band LNA Design parameters

The Results of our Design are shown below in the following figures.

1) Gain Curves

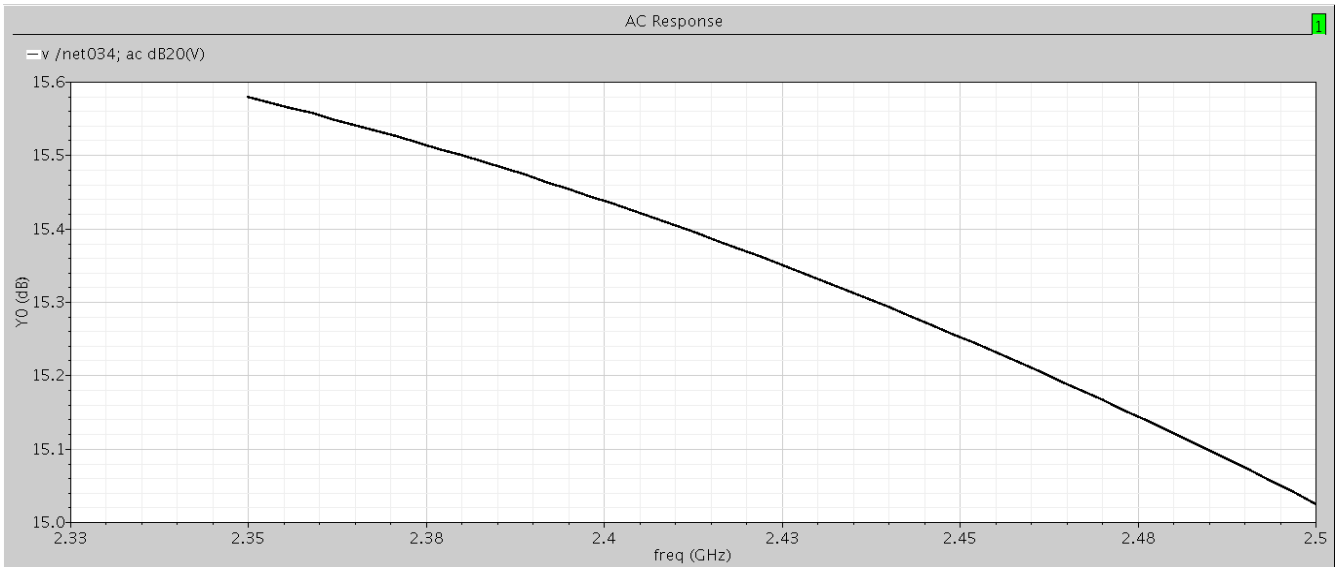


Figure 2.8 Ac_ Response (Gain in dB)

The Graph shown in (Figure 2.8 Ac_ Response (Gain in dB)) describes the AC response of our LNA. It is clear the Gain covers our Desired Band (2.4Ghz till 2.48 Ghz) with a minimum variation than the desired value(15 dB).

2) Noise Figure (around 1.4dB)

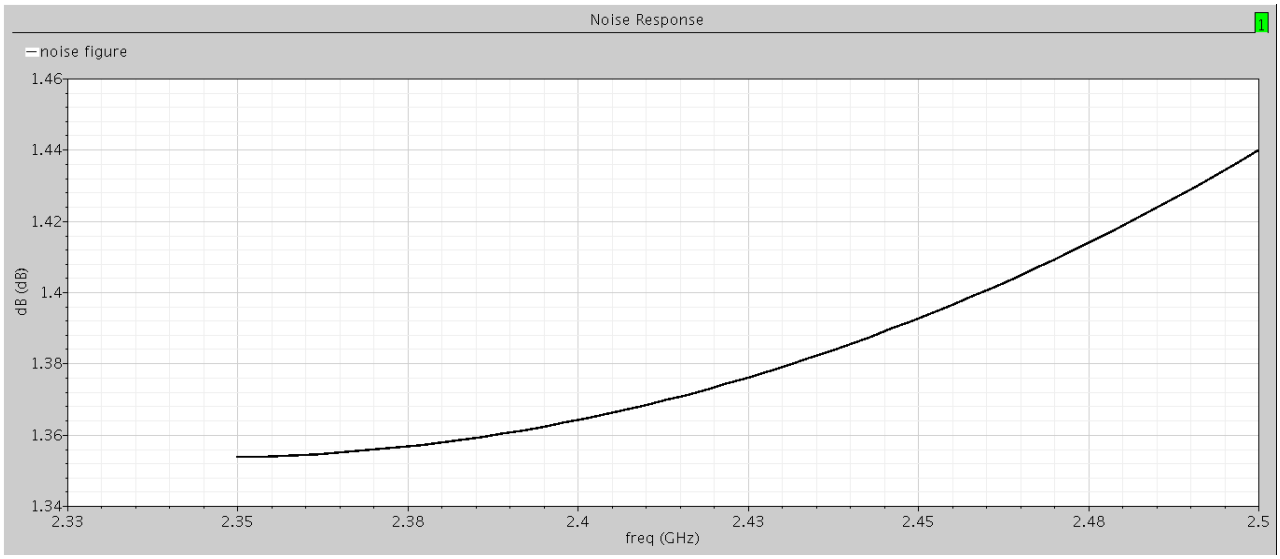


Figure 2.9 Noise Figure

As shown in (Figure 2.9) , the Noise Figure Varies between (1.36dB till 1.44dB) which is acceptable. This value is a good point in this design . this low value is due to the High Gain and the large value of gm in M1.

3) S11 Curve (less than -15 dB)

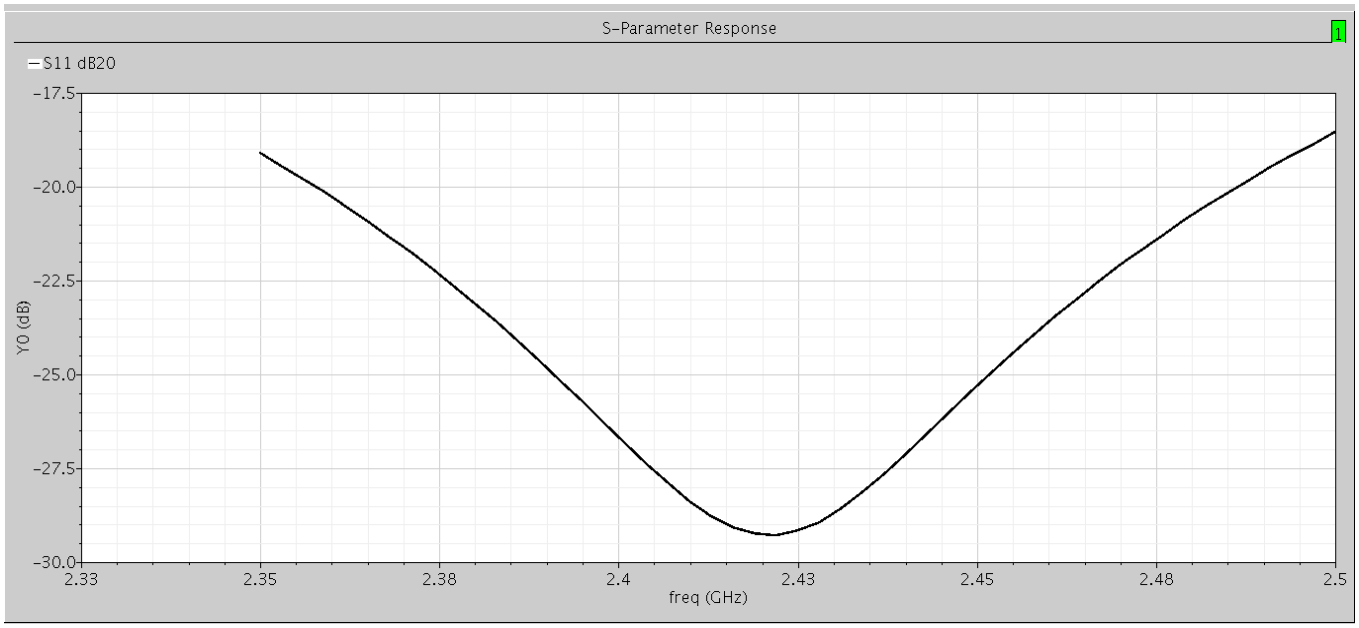


Figure 2.10 S11 Curve in dB

The S11 represents that input matching. S stands for “S parameters “ , and for better matching , the value of S11 has to be as lower as possible. As shown in (Figure 2.10), the Value of S11 is accpetable (Below -15 dB) , which means that we have good input matching conditions which maximizes the Power Transferred from the input Port. There is always a Tradeoff between Matching for maximimzing Power Transferred or Minimizing the Noise Figure. In This Design, we are maximizing the Transferred Power because we need a higher gain requierements.

4) **Z11 (Impedance matched to 50 Ω)**

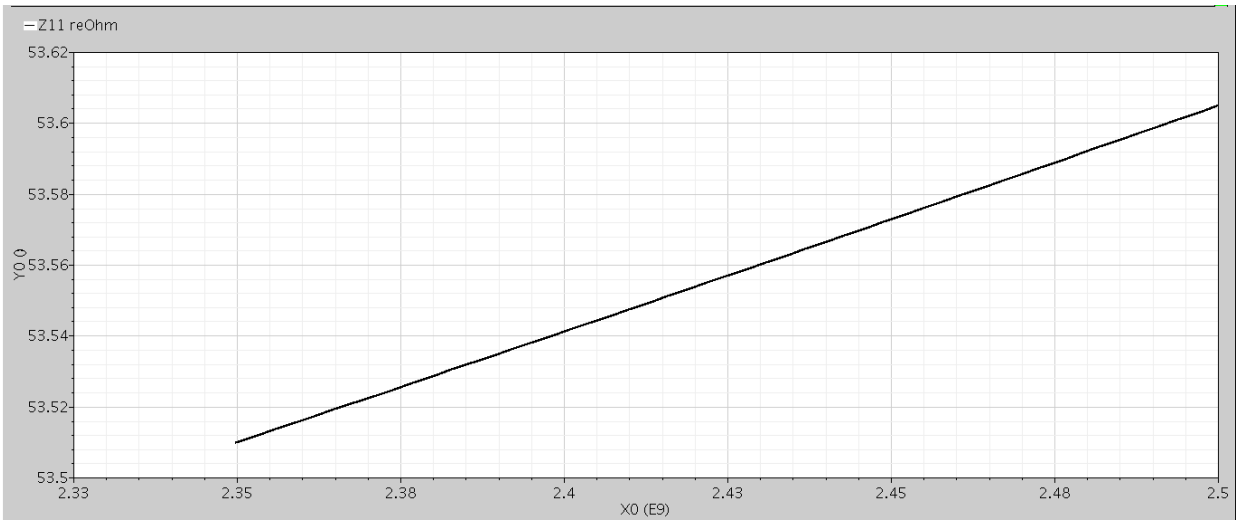


Figure 2.11 Z11 Curve

Z11 is another representation for Input matching, it represents the Impedance seen from the source. As we can see in (Figure 2.11) , the Input impedance of the LNA is matched to 50 Ω on the all Desired Band which is equal to the Source Impedance. Therefore, Power is Maximized.

5) IIp3 (> 0dBm = 2.13 dBm)

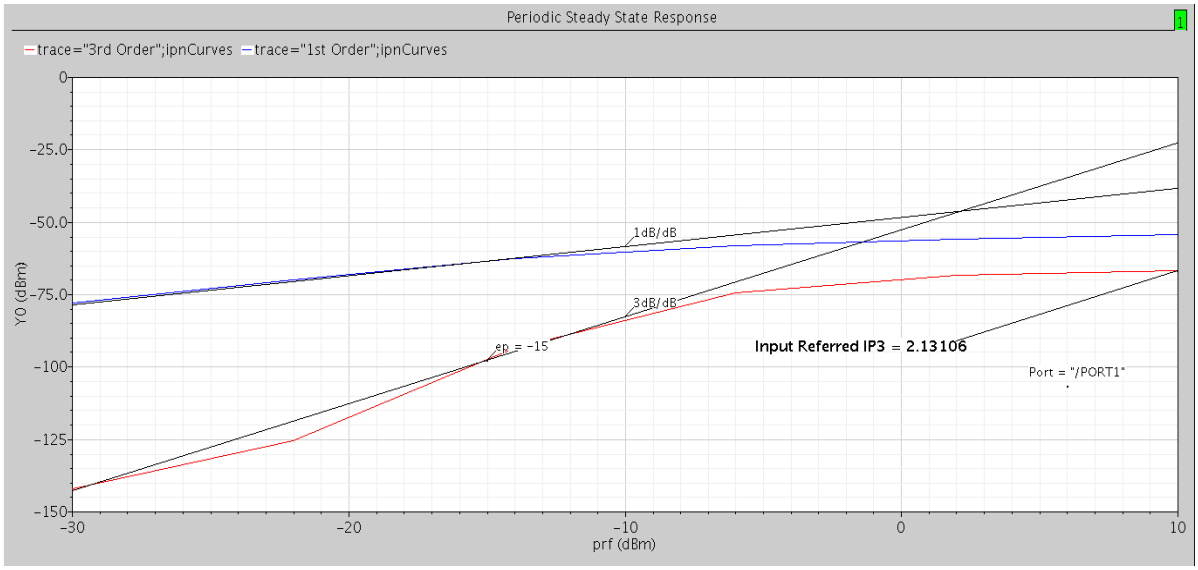


Figure 2.12 IIp3 Curves

The IIP3 is a measure of our circuit linearity, how it deals with higher order harmonics and their representation in the output, higher value of IIP3 means a better Performance. Our Circuit's IIP3 has a value of 2 dBm as it is shown in(Figure 2.12) which is a good design value.

It's now clear that this LNA is a narrow band LNA, where all the specifications are realized in a narrow Band. To make the LNA works properly in the TV Band (wide Band), we are going to discuss in the following section wide band techniques for LNA design.

2.4 Wide band LNA Techniques:

- Wide band LNAs require 2 kinds of wide band operations , wide band gain and wide band matching , and we will discuss both of them in this section.

2.4.1 Wide Band Gain :

2.4.1.1 *Active shunt peaking technique at transistor drain:*

The main idea is adding an active shunt parallel with the output to increase the Gain Bandwidth .

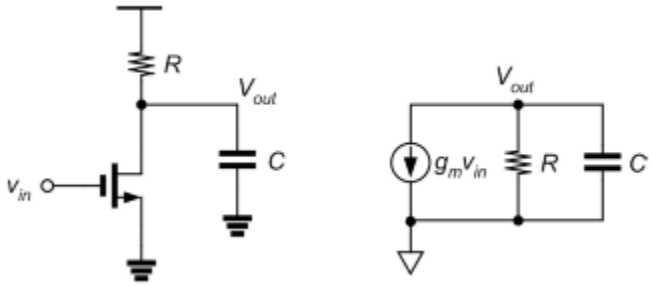


Figure 2.13[9] The common source amplifier and its equivalent circuit

Consider the simplified circuit in (Figure 2.13). Also for simplicity we add a normal shunt and we assume that the small signal frequency response of the amplifier is determined only by the dominant pole at the output node as described in Equation 2.9

$$A_v(\omega) = \frac{v_{out}}{v_{in}} = -g_m * \frac{R}{1 + j\omega RC} \qquad \text{Equation 2.9}$$

R and C are the output load resistance and the load capacitance, respectively.

Now we introduce an inductance L in series with a resistance R_L and add it parallel with the original RC load. The impedance of the inductive branch, increasing with the frequency, offsets partially the decreasing impedance of the RC network. It results a roughly constant gain over a broader frequency range and hence improves the bandwidth. We can also see from the transfer

function of the compensated amplifier shown below. It has two poles and one zero. The additional zero contributed by the inductive branch helps the enhancement of the bandwidth (see Figure 2.14)

L

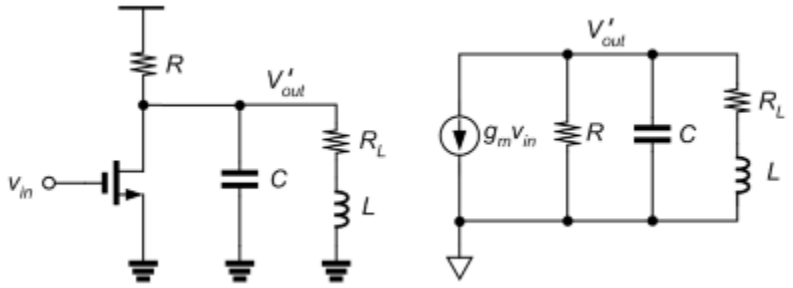


Figure 2.14 [9] : The common source amplifier with shunt peaking and its equivalent circuit

The new Wide Band gain is described in Equation 2.10

$$A_v(\omega) = \frac{v_{out}}{v_{in}} = -g_m * \frac{R_L + j\omega L}{1 + \frac{R_L}{R} + j\omega \frac{L}{R + R_L C} - \omega^2 LC} \qquad \text{Equation 2.10}$$

It should be noted that R_L should be in an appropriate range for getting an enhanced low-pass characteristic.

DC Gain was reduced from

$$\boldsymbol{A_v(0) = -g_m * R} \qquad \text{Equation 2.11}$$

To :

$$\boldsymbol{A_v(0) = -g_m * (R // R_L)} \qquad \text{Equation 2.12}$$

Now, let's consider an active shunt added to a Differential amplifier circuit as shown in (Figure 2.15)

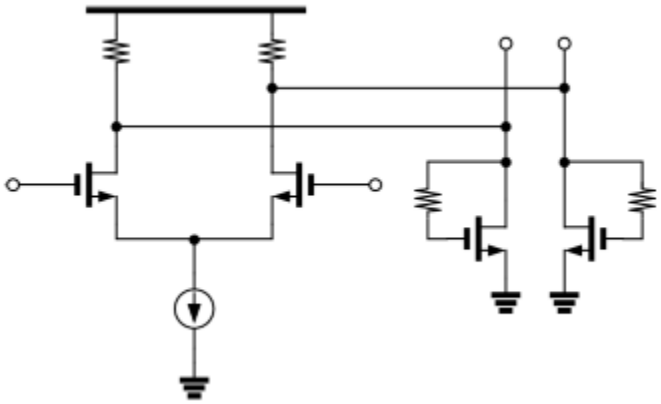


Figure 2.15 [9] : Active shunt peaking wideband differential amplifier

The equivalent impedance is a parallel connection of (see Figure 2.16)

1. Total parasitic capacitance C_P
2. Output resistance of transistors r_{ds}
3. The RC network composed of $R_f, C_{gd}\ and\ C_{gs}$

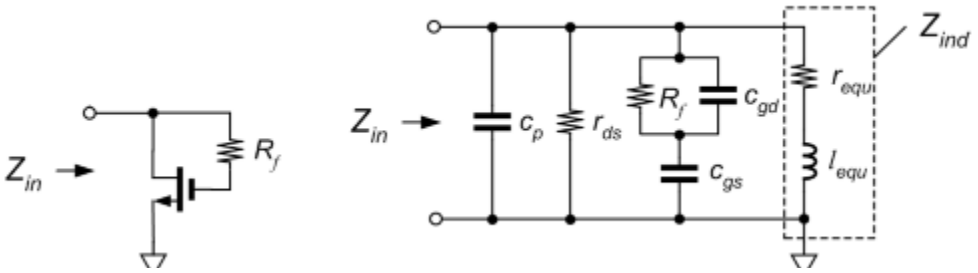


Figure 2.16 [9] : The active inductive branch and its equivalent model

The required input impedance is shown in Equation 2.13

$$\boldsymbol{Z_{in}} = \frac{1}{g_m} * \left(1 + \frac{j\omega R_f C_{gs}}{1 + j\omega R_f C_{gd}}\right) \qquad \text{Equation 2.13}$$

If we look insight into the operating mechanism, we can find that the voltage-controlled current source and a RC network realize the function of an ideal inductor: when the voltage at the input node changes, the current of the source which is controlled by gate-source voltage will not follow the change immediately but is delayed due to the RC low-pass network between the input node and the gate node.

Now let's separate the 2 equations of $\boldsymbol{r_{equ}}$ and $\boldsymbol{l_{equ}}$

$$\boldsymbol{Z_{in}} = r_{equ}(\omega) + j\omega l_{equ}(\omega)$$

$$r_{equ}(\omega) = real(\boldsymbol{Z_{in}})$$

$$r_{equ}(\omega) = \frac{1}{g_m} * \left(1 + \frac{(\omega R_f)^2 C_{gs} C_{gd}}{1 + \left(\omega R_f C_{gd}\right)^2} \right) \; at \; R_f \; \ll \; \frac{1}{\omega C_{gd}} \qquad \text{Equation 2.14}$$

$$r_{equ}(\omega) \approx \frac{1}{g_m}$$

$$l_{equ}(\omega) = {imag(\boldsymbol{Z_{in}})}/{\omega}$$

$$l_{equ}(\omega) = \left(\frac{C_{gs} R_f}{g_m * (1 + \left(\omega R_f C_{gd}\right)^2)} \right) \; at \; R_f \; \ll \; \frac{1}{\omega C_{gd}} \qquad \text{Equation 2.15}$$

$$l_{equ}(\omega) \approx \frac{C_{gs} R_f}{g_m}$$

When the condition of $R_f \; \ll \; \frac{1}{\omega C_{gd}}$ is fulfilled in the required frequency range, the effect of C_{gd} is almost ignored, and $\boldsymbol{r_{equ}}$ and $\boldsymbol{l_{equ}}$ are almost frequency independent.

2.4.1.2 Simulation results:

The simulated bandwidth of the maximum-bandwidth-optimized buffer is about 9.58 GHz. And that of the maximally-flat-optimized buffer is about 8.67 GHz. Compared the bandwidth of the normal buffer 5.20 GHz; both have evident bandwidth enhancements about 80% and 65% respectively(Figure 2.17).

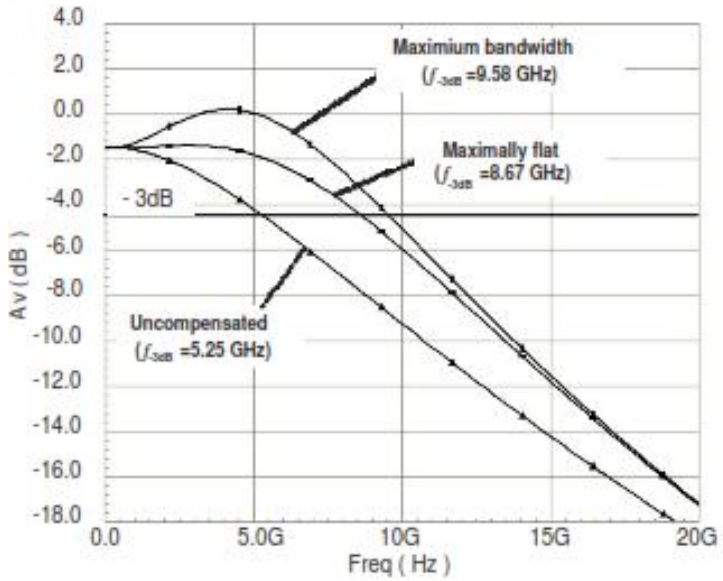


Figure 2.17 [9] : Gains of normal circuit and after adding the active shunt

2.4.2 Gate inductive peaking technique :

The size of the shunt inductor added parallel to the drain of the transistor which is very large and consumes a great deal of area. So an alternative way is a gate-inductive-peaking technique with an inductor placed at the gate of the input transistor is presented. Using this topology, a much smaller inductor is needed to achieve a similar bandwidth extension while the gain flatness is improved simultaneously.

Small note: while analyzing this technique we will consider the topology that ensures a wide band matching that will be discussed in section 2.5.1 (see Figure 2.18)

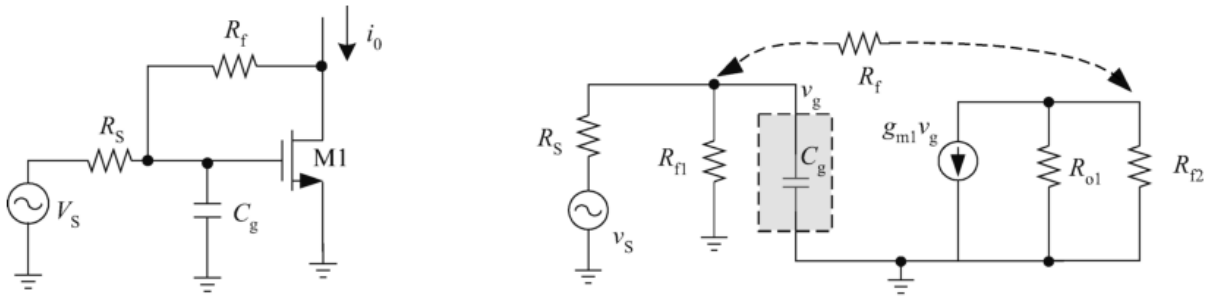


Figure 2.18[10] : Common source amplifier with resistive feedback to ensure wide band matching, and its equivalent circuit

In this topology, $Z_{in} = {}^{1}/_{g_{m1}}$

The small signal equivalent circuit of the matching stage amplifier where R_{f1} and R_{f2} are miller equivalent resistors of R_f and C_g is the sum ofC_{gs1}, Miller equivalent capacitor of C_{gd1} and other possible capacitors at the input port.

The signal voltage at the gate of M1 is derived as :

$$v_g = v_s * \frac{R_{f1} // \frac{1}{sC_g}}{R_s + R_{f1} // \frac{1}{sC_g}} = v_s * \frac{R_{f1}}{R_s R_{f1} s C_g + R_{f1} + R_s} \qquad \text{Equation 2.16}$$

And Voltage gain is derived as

$$\mathrm{A_v} = -\mathrm{g_{m1} v_g} * \frac{\mathrm{R_{f2} // r_{o1}}}{\mathrm{v_s}} = \mathrm{v_s} * \frac{-\mathrm{g_{m1} R_{f2} (R_{f2} // r_{o1})}}{\mathrm{R_s R_{f1} s C_g + R_{f1} + R_s}} \qquad \text{Equation 2.17}$$

Where the transfer function has only 1 pole at

$$s = \frac{-(R_s + R_{f1})}{R_s R_{f1} C_g}$$

Now let's apply the gate inductive peaking technique (see Figure 2.19)

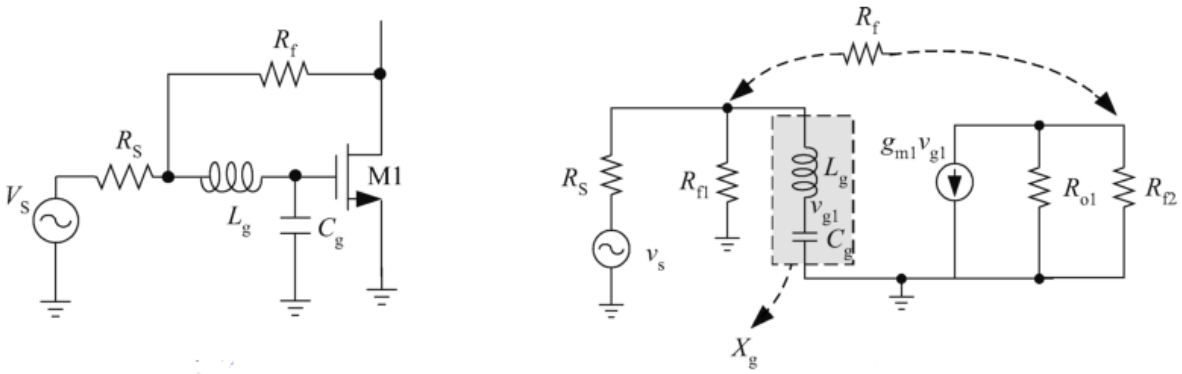


Figure 2.19 [10] : common source amplifier with inductive gate technique and its equivalent circuit

First we assume that

$$X_g = sL_g + \frac{1}{sC_g}$$

The signal at the gate of M1 is derived as

$$v_{g1} = v_s * \frac{R_{f1} // X_g}{R_s + R_{f1} // X_g} * \frac{\frac{1}{sC_g}}{X_g}$$

Then the Gain is derived as

$$A_v = v_s * \frac{-g_{m1} R_{f2} (R_{f2} // r_{o1})}{(R_{f1} + R_s) L_g C_g s^2 + \frac{\omega_o}{Q_o} s + {\omega_o}^2} \qquad \text{Equation 2.18}$$

Where $\omega_o = 1 \Big/ (\sqrt{L_g C_g})$ and $Q_o = \frac{(\sqrt{L_g C_g}(R_{f1} + R_s))}{R_s R_{f1} C_g}$

The real parts of the complementary poles at the transfer function are both $-\frac{\omega_o}{2Q_0}$ and they can be placed at higher frequency by adjusting the value of L_g. Therefore, the gain rolls off at higher frequency although the roll-off is twice as fast. This is the mechanism of the pole splitting (see Figure 2.19) So the value of L_g defines Q_0 which is related to the frequency response of the common source amplifier. High Q_0 result in gain peaking.

2.4.2.1 *Simulation results:*

After simulation, and comparing different values of L_g and its impact on gain and bandwidth, this was the result (see Figure 2.20), which clearly shows the gain flatness due to L_g .

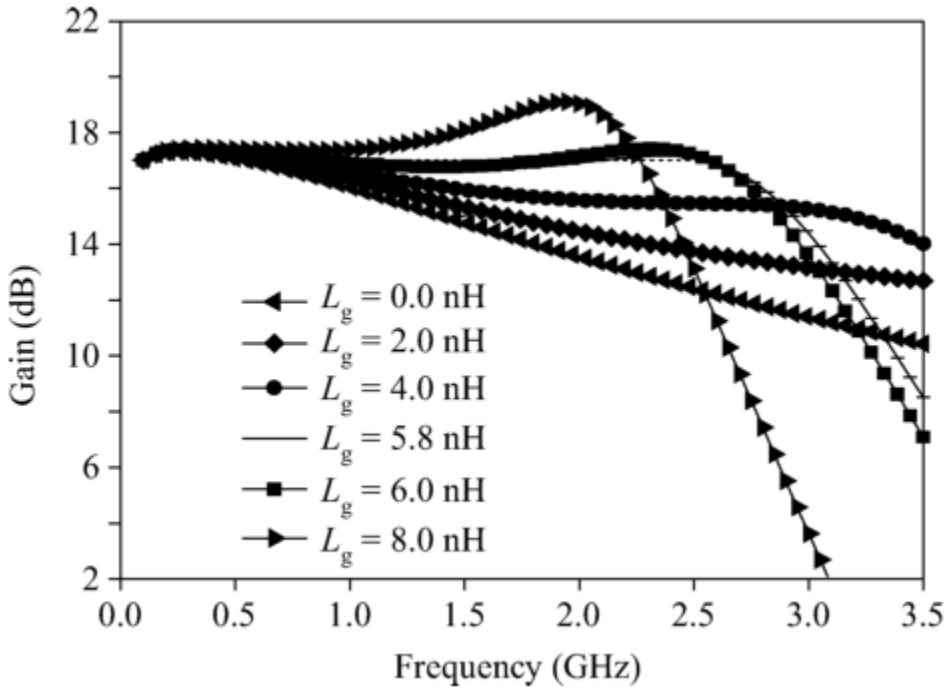


Figure 2.20 [10] : Different value of Lg and their impact on gain and bandwidth

2.5 Final LNA Design for TV-Tuner

After discussing the main wide band techniques, in this chapter we are going to discuss how we are going to design our LNA so it can meet the specifications required. As we discussed in section 2.4, the main challenges in designing an LNA are :

1) Wide band input matching

2) Moderate gain so it can reduce the noise Contribution from the other stages. This can be proved from (Equation 2.19):

$$NF_{total} = F1 + \frac{F2 - 1}{G1} + \frac{F3 - 1}{G1 * G2} + \cdots .. \qquad \text{Equation 2.19}$$

Where NF = the Noise Figure of the Total System in dB , (F) is the Noise Factor of each individual block and (G) is the gain of each individual block. It is clear that the LNA noise is added (1: 1) in the output, but the next stages are divided by the Gain of the preceding blocks.

3) Low Noise performance to improve the system sensitivity

4) Low power Consumption to extend the battery life

5) Small chip size to reduce the cost of the designed chip

First of All, we were choosing between a Common Gate LNA due to its wide band matching (1 /gm) Versus a Common Source LNA , but because of the Gain requirement was (14 dB to 17 dB), we choose the Common Source LNA because most of the papers we have read the CG-LNA can't achieve this gain easily . Now our main challenges are the Power and Noise Figure Requirements.

2.5.1 Wide Band Common Source LNA with Resistive Feedback

Resistive Feedback is one of the most famous techniques used to achieve a wide band matching and Minimum Noise Figure degradation. This was Proved and Simulated By [11] Kim, etc. They Published an UWB LNA using a resistive feedback. Design and Simulation results and shown in (Figure 2.22 , Figure 2.23 and Figure 2.24). the main advantages are that they reduce the Noise Figure , flatness the Gain and reduce the chip size because we use less inductors . So we are going to discuss a simple LNA with Resistive feedback.

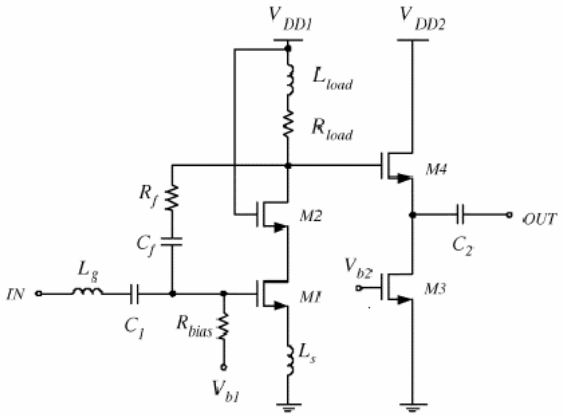


Figure 2.22 [11] Kim, etc Design

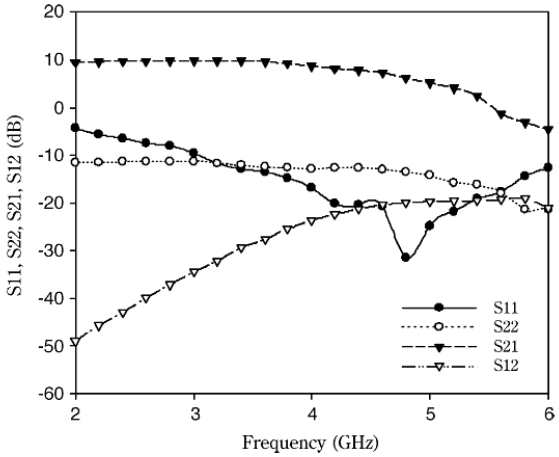


Figure 2.21 [11] Kim, etc Results

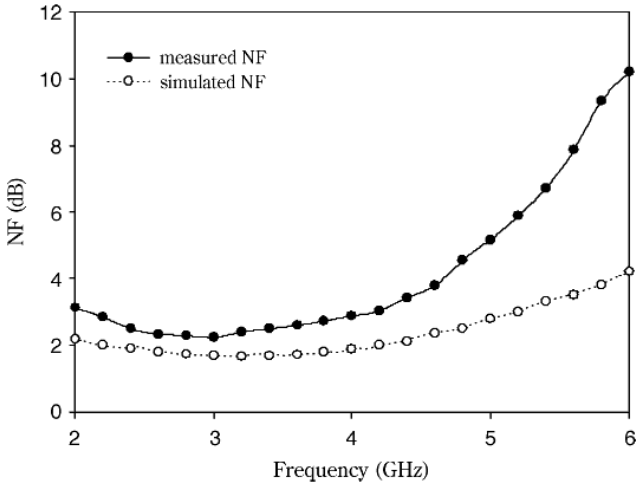


Figure 2.23 [11] Kim, etc NF Results

2.5.1.1 *Basic Structure of Resistive Feedback Amplifier*

The Basic Structure is shown in (Figure 2.24), where :

RL : Load Resistance

Rf : Feedback Resistance

Rs : Source Resistance

Vin : Input to the Amplifier

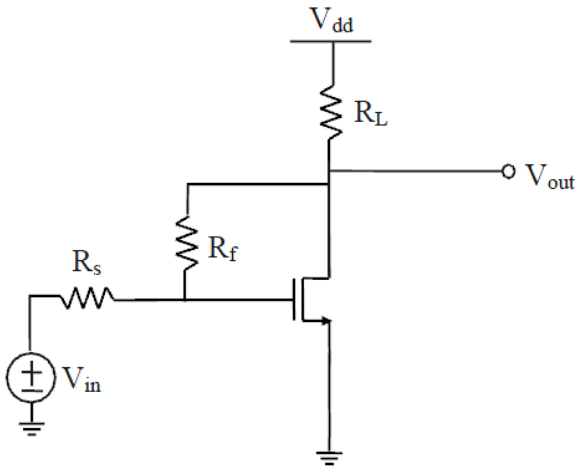


Figure 2.24 [8] [Basic Resistive feedback structure

Calculating **Rin** :

$$Rin = \frac{Vin}{I_{in}} = \frac{Vin}{gmVin + \frac{Vout}{Rl}}$$

$$Iin = \frac{V_{in} - V_{out}}{Rf} = \frac{Vout}{RL} + gmVin \rightarrow \quad Vout = \left[\frac{1 - gmRf}{Rf}\right] Vin\left[\frac{RfRL}{Rf + Rl}\right]$$

$$Rin = \frac{Vin}{In} = \frac{Rf + Rl}{gmRl + 1} \rightarrow gmRl \gg 1 \rightarrow Rin \qquad \text{Equation 2.20}$$

$$= \frac{1}{gm}\left(1 + \frac{Rf}{Rl}\right)$$

Calculating **Gain** :

$$Av = \frac{-V_{out}}{0.5\,Vin} = \frac{-Rl(gmRf - 1)}{Rf + Rl} \approx \frac{-gm\,Rf\,Rl}{RF + RL} \qquad \text{Equation 2.21}$$

$$\approx \frac{-Rf}{Rin}$$

Approximation is valid as gmRf >>1 , if we want to increase the gain , RF has to be increased w.r.t the Input , as by the way , gmRL has to be increased also .

Now if we want to achieve higher Gain, (17 dB in our Design) , Following(Equation 2.21) Rf will be around 350Ω and in order of input matching Rl will be around 240 Ω(Following Equation 2.20), which will make a very large headroom , so we have to find a way such we can Decrease the Value of RL for the same gain .

2.5.2 Feedback for a source Follower

The Following figure (see Figure 2.25) shows how a feedback for a source follower can be achieved, first we will ignore the effect of capacitors at nodes and we will calculate low frequency gain and Input Impedance

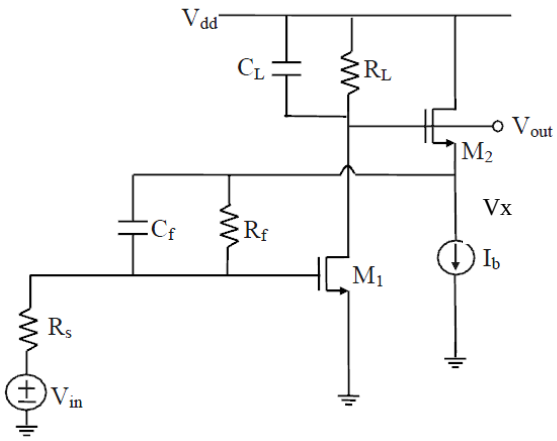


Figure 2.25 [8] R-C resistive feedback through a source follower

Now Calculating **Rin**

$$Rin = \frac{Vin}{I_{in}} = \frac{Vin}{-gm_2(vout - vx)}$$ Equation 2.22

$$vout = -gm_1 vinRL$$ Equation 2.23

Now Calculating **Vx**

$$\frac{Vin - Vx}{Rf} = -gm_2(Vout - Vx)$$

$$Vx = \frac{Vin + gm_2 Vout\, Rf}{1 + gm_2 Rf}$$ Equation 2.24

Now by Substituting(Equation 2.23 and Equation 2.24 in Equation 2.22) we can Calculate **Rin**

$$Rin = \frac{1 + gm_2 Rf}{gm_2(1 + gm_1 RL)} \approx \frac{1}{gm1}\frac{Rf}{RL} \qquad \text{Equation 2.25}$$

Approximation can be made when (gm1RF >>1 and gm2Rf >>1)

Calculating Gain

$$Av = -gm_1 Rl = \rightarrow -\frac{Rf}{Ri} \ \ from\ the \text{ Equation 2.25} \qquad \text{Equation 2.26}$$

Having the same gain which is equal to 17 dB , based on Equation 2.26 , Rf has to be 350 ohms , RL will be 140 ohms which is less than 235 ohms from the previous design . We can conclude that the headroom is decreased which is a good Point.

But the Previous analysis neglected the effect of the capacitance, now taking into Consideration the effect of CL. ,the Following equation will show the effect of CL on the input Impednace

$$Rin = \frac{1 + gm_2 Rf}{gm_2(1 + gm_1 RL)} * \frac{1 + s\ C_l RL}{1 + s\ \frac{C_l Rl}{gm1Rl}}$$

It is clear that the system now has one pole at ($1 + s\ \frac{C_l Rl}{gm1Rl}$=0) and one zero (at $1 + s\ C_l RL$=0)

At high frequencies, gain is dropped due to poles. This could be solved either increasing high frequency gain or reducing the feedback impedance at higher frequencies. This could be Done using the Cf Capacitor in parallel with the Feedback Resistor (Rf).

Now the System Frequency Response will be showed in the following equation:

$$Rin = \frac{1 + gm_2 Rf}{gm_2(1 + gm_1 RL)} * \frac{1 + s\, C_l RL}{1 + s\, \frac{C_l Rl}{gm1 Rl}} * \frac{1 + s\, \frac{CfRf}{gm2\ Rf\ Cf}}{1 + s\ CfRF}$$ Equation 2.27

It is clear Now that our system now have two poles and two zeros , by choosing suitable Values for CF , our system could have an excellent Frequency Response . But Due do that our system targets only the TV Band , (Maximum BW is 2 Ghz) , the effect of Cf will not be considered in our Design for simplicity and also so that we can decrease the Chip size .Improvements on the design will be made using **Input Gate Feedback Inductor**

2.5.3 Input Gate Inductor

The main Concept of Gate Feedback Inductor is Described in Section (2.4.2) , but as a brief idea , it makes a new Pole at high Frequency, but at the same time, it makes the 2 existing poles go to higher Frequency. There is an optimum value for this inductor, will be chosen properly by simulation.

Finally to conclude our first design, we will use Resistive feedback with gate inductor to achieve the wideband Range. Other improvement may be made during simulation and will be shown there.

2.5.4 Transforming from Single Ended to Differential Amplifier

To transform from single ended to differential Amplifier, we must add a Component that enables the signal to be divided into two, said in other words, transform the signal received from the antenna to two components such that they could be treated in a differential way. The device that can do that is the Balun . The balun is [balanced to Unbalanced] a device that takes single ended signal and transforms it to differential signal and vice versa. In next pages, the Response of the Balun will be shown.

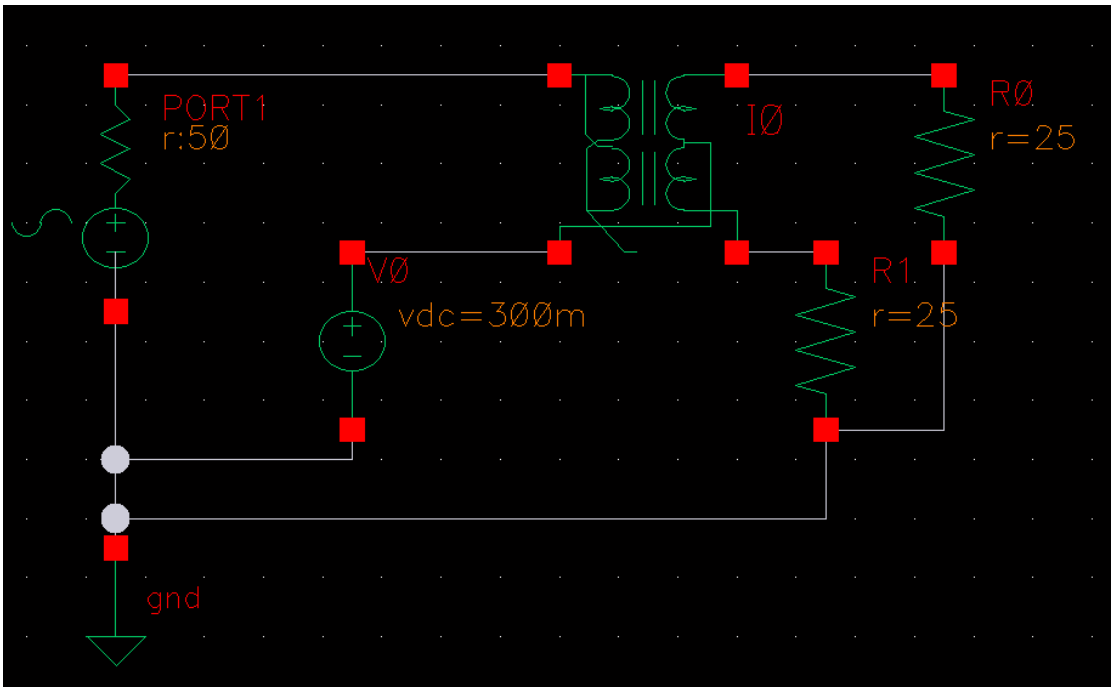


Figure 2.26 Balun Test bench

As Shown in (Figure 2.26), a test bench for the Balun is made first such we know how it deals with Differential signal. By adding a 25 Ω Resistance one Both Sides and an AC input Port, we are going to see the gain and the input impedance seen by the Balun in the following images.

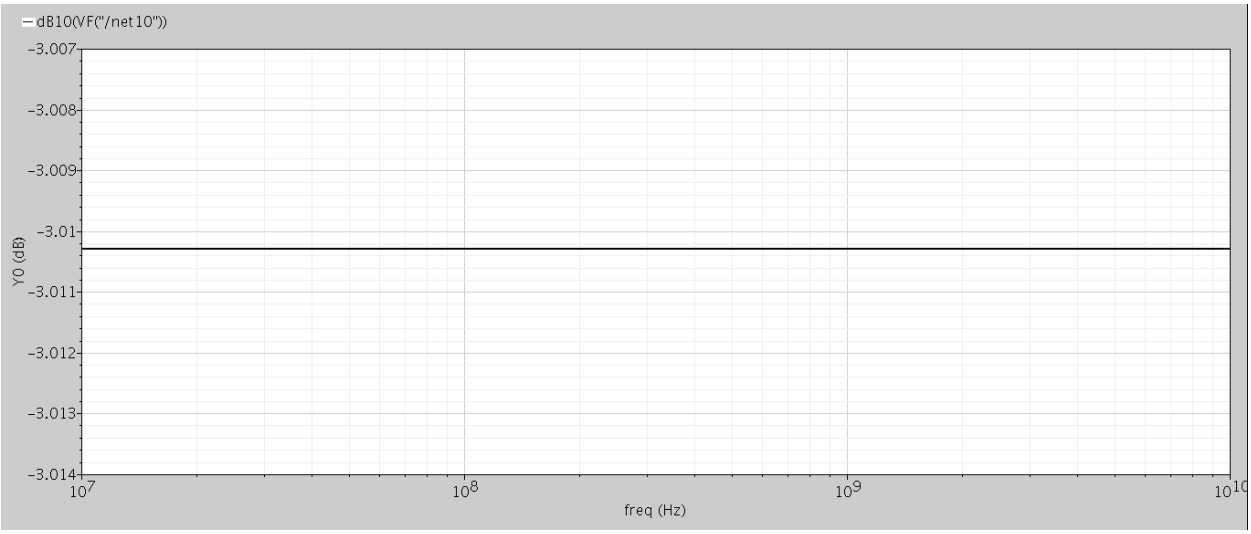


Figure 2.27 AC response of Balun

As described in Figure 2.27 , it is clear the the Balun inserts a gain of 3dB on the overall system. It must be taken into consideration while designing our system because it will affect the system response. Accurate simulation must be Done.

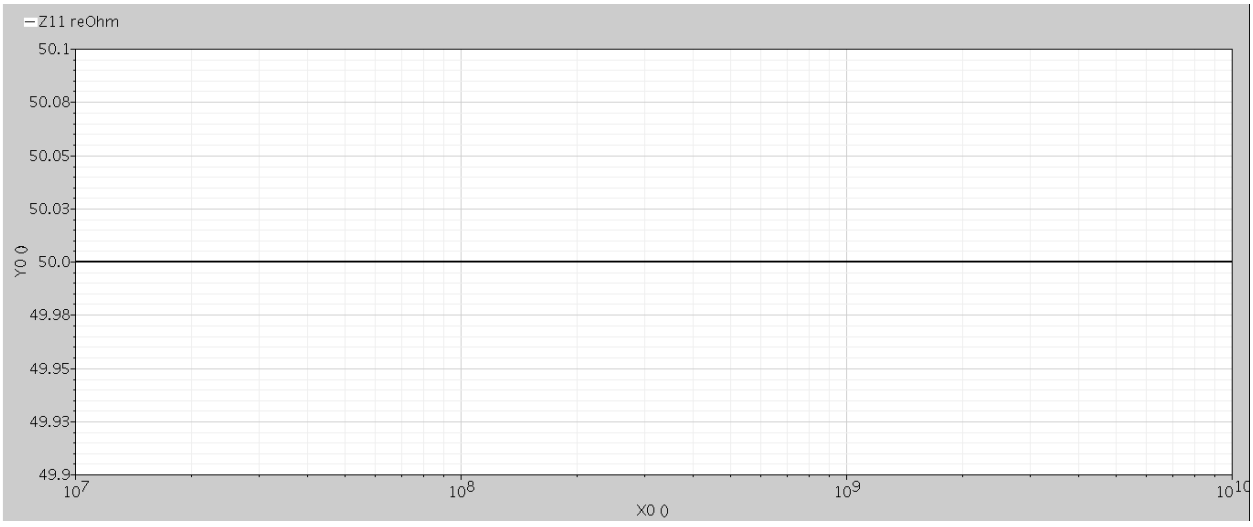


Figure 2.28 Input Impedance of Balun

it is clear that the balun is matched to 50 Ω when each differential pin has a 25 Ω Resistance. Therefore , we must take this into conisderation while matching our LNA.

To Summarize what Problems we Face with ideal Balun :

- Input Matching to 25 ohms at each terminal
- There doesn't exist an actual balun with a wide range
- Extra Gain of 3 dB.

2.5.5 Current Bleeding

The Current Bleeding as shown in (Figure 2.29) is an additional Current Mirror added in parallel with a Resistor to decrease the current flowing inside a resistor, so the headroom [voltage drop] across the resistor will decrease. This will allow an allowable swing for the Input MOSFET and also due to the Limited Voltage source (1.2 V), we need a voltage Drop to ensure that the differential current mirror enters the SAT region (V compliance).

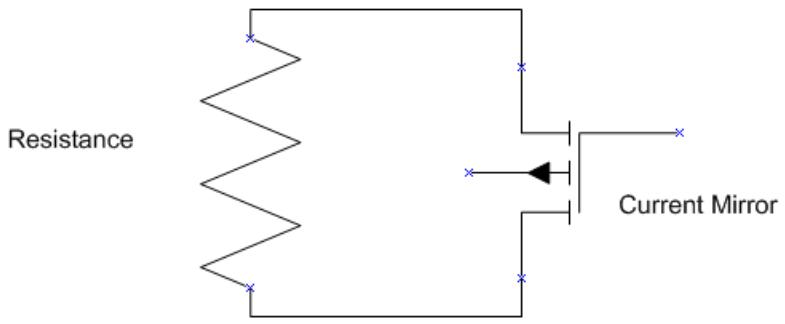


Figure 2.29 Current Bleeding Concept

2.5.6 LNA Design Procedure

2.5.6.1 *Single Ended LNA*

As a first wideband LNA, we began first by designing a moderate gain and noise, wideband LNA. Our main target was to apply wideband techniques that will help us to achieve our Final Design. We began by single ended LNA with Resistive feedback and Gate Inductive peaking technique for a wideband Range. As we can see in (Figure 2.30 and) we achieved a 3dB Bandwidth of approximately 9Ghz Band , but the gain was not as high as we want and consequently the noise figure was high than the Average.

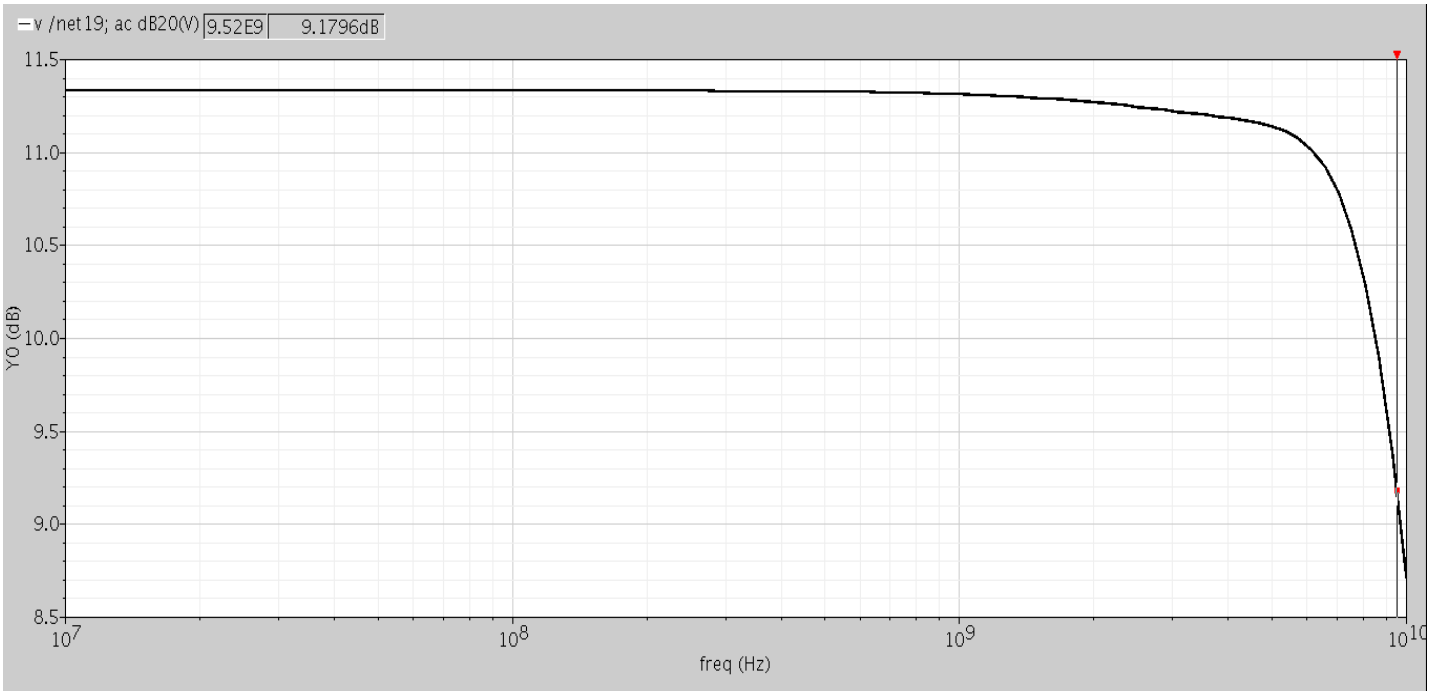


Figure 2.30 Wide Band Gain for a single ended LNA

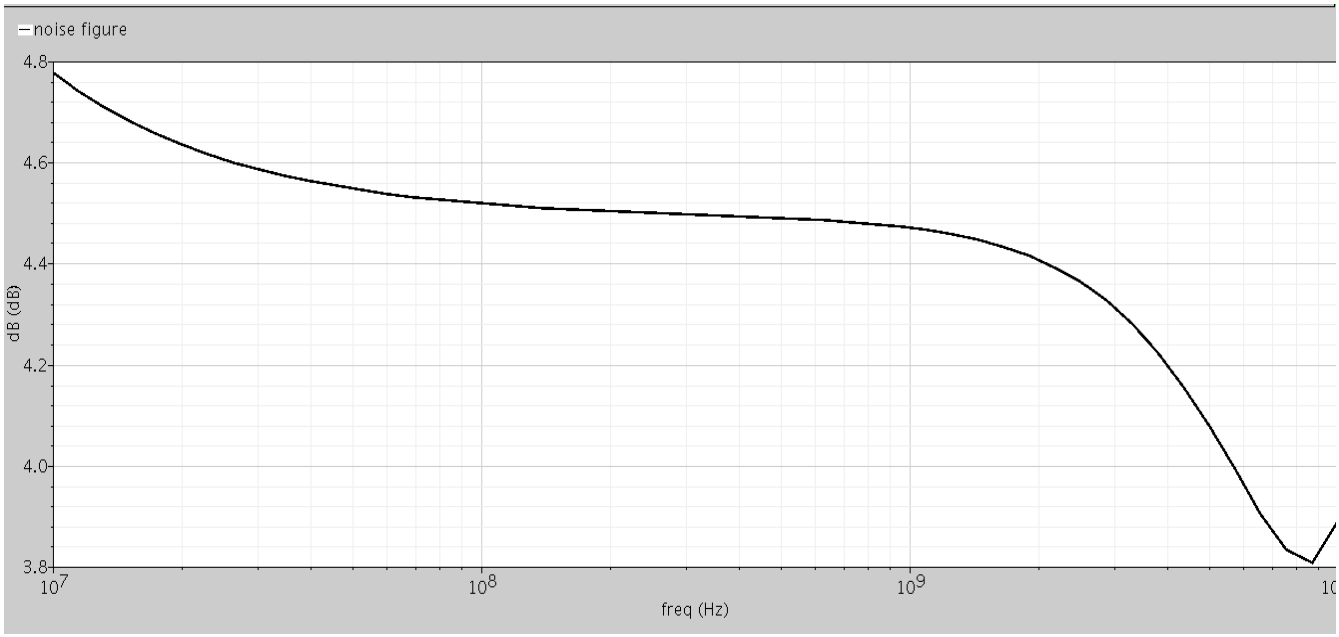


Figure 2.31 Noise Figure of Single Ended LNA

as we can see in(Figure 2.31) , the noise Figure Range is between 3.8dB and 4.8 dB over all the 10Ghz Range . But this design was made using all ideal Components, so these Results will be much worse than the real one. So, our Next Step in the design will be how to make a suitable design for our TV-Tuner. So we have put some challenging Specification so that we can make a great effort to achieve all the requirements for a minimum power consumption TV Tuner LNA.

2.5.6.2 *Differential LNA*

First of all , Consider(Table 2.3 Comparaison between Differential VS Single Ended LNA)that shows a clear comparison between a single ended LNA and a Differential one.

Differential LNA	Single Ended LNA
Common Mode Rejection	No Common Mode Rejection
Double area and Power	Less Power for Same NF and Linearity
Need a balun at input	No need for a balun
Drive Double balanced Mixer	Drive single Balanced Mixer

Table 2.3 Comparaison between Differential VS Single Ended LNA

The Requirements Set on the LNA are shown in (Table 2.4 Requirements Table**)**

Parameter	Restriction
Power Consumption	**15 mW**
Bandwidth	**40Mhz – 2Ghz**
Gain	**Between (14dB and 17dB)**
S11	**Less than -12dB**
Noise Figure	**Less than 2.5dB**
IIP3	**Greater than Zero**
Load Capacitance	**Mixer Input Capacitance**

Table 2.4 Requirements Table

2.5.6.3 *Proposed Schematic*

Our Final Design Propose a Differential LNA with Resistive Feedback and Inductive Peaking Techniques for Wideband Design. The Schematic shown in (Figure 2.32) Clarify the Wide Band techniques used.

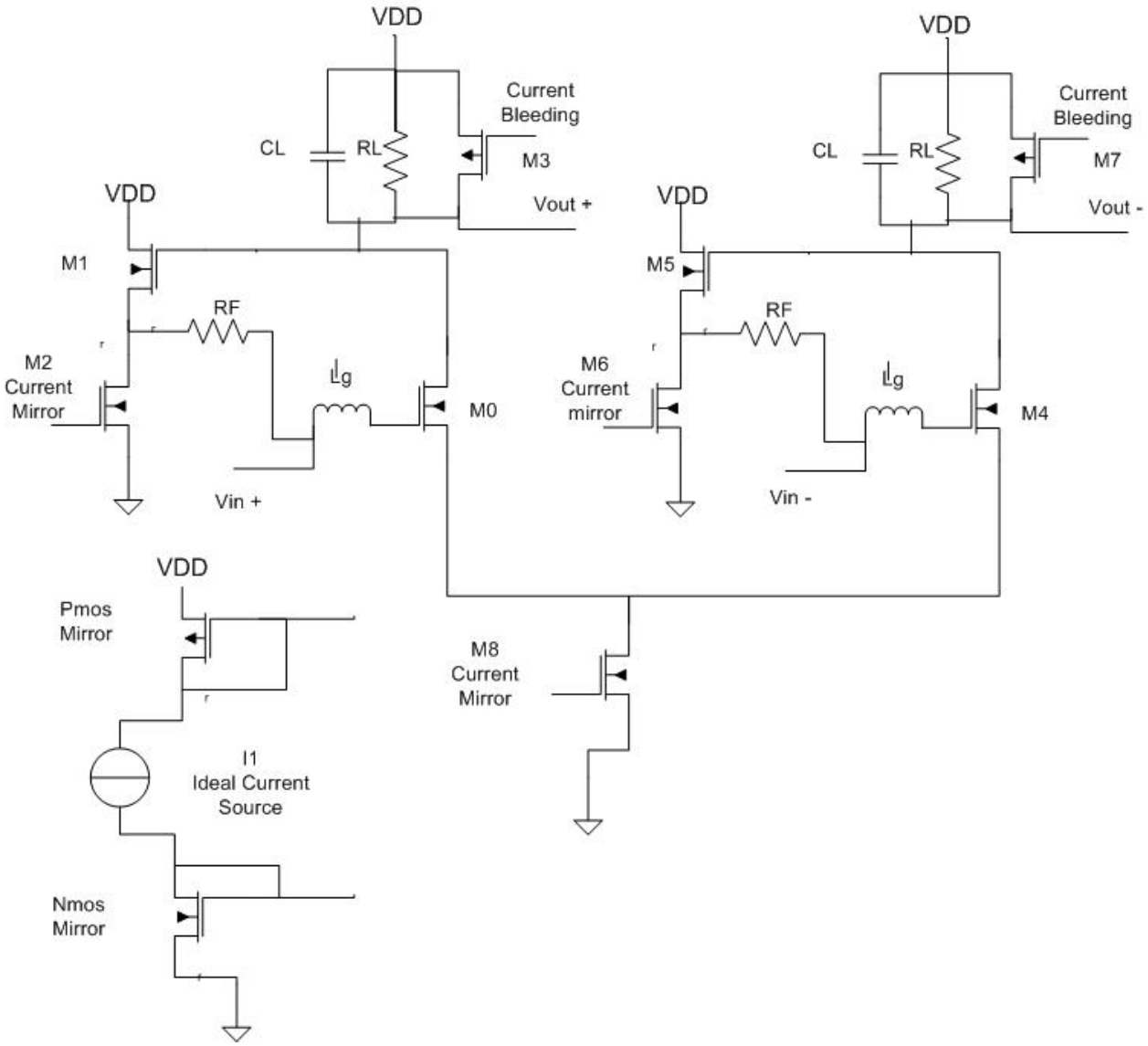


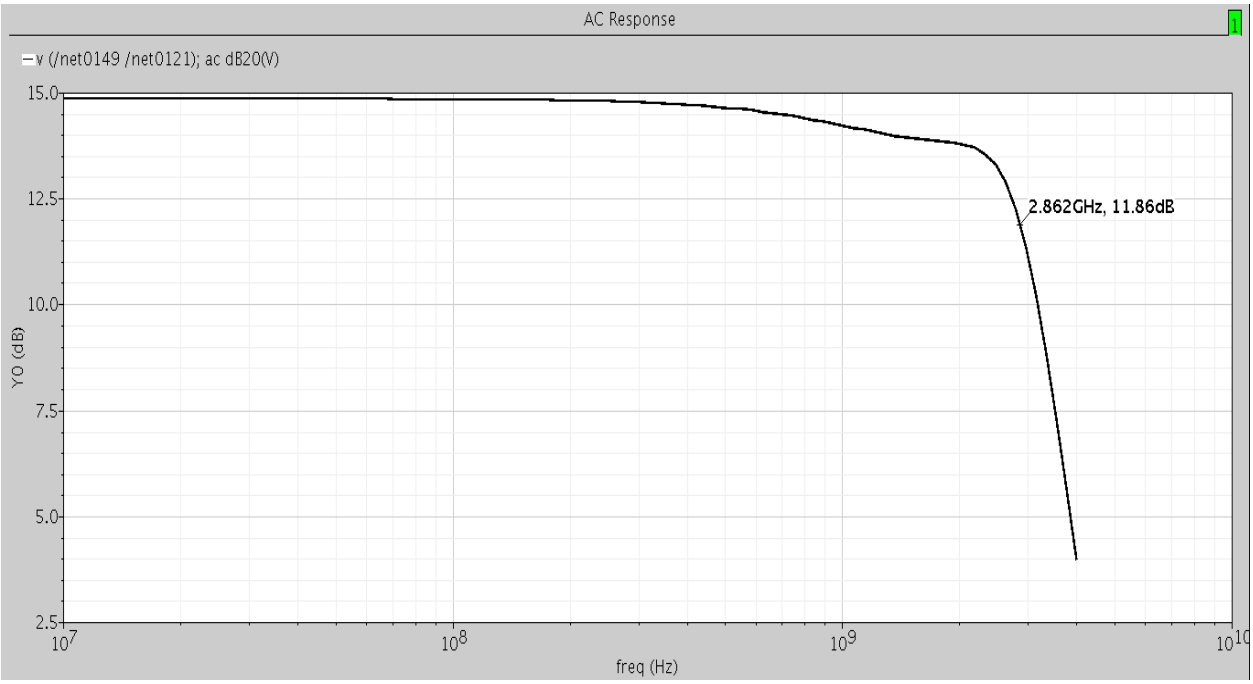
Figure 2.32 Differential LNA Final Design

2.5.6.4 *Final Results*

Note: Simulation Range (40Mhz to 4 Ghz)

Required Bandwidth : (40 Mhz to 2 Ghz)

In the following Next Pages, an Analytical Analysis will be made on the Design Results. First, as we can see in (Figure 2.33) , the Gain is Around 15 dB over the Total Bandwidth (till 1.45 GHz), and the 3-dB Point is at 2.862 GHz. We are ensuring that the Gain is between (14 dB and 17 dB over the 2GHz Band). The Gain can be increased by increasing the Ratio RF/RL but at the same time, we have to make sure that the Input Impedance is still matched. Changing a Parameter must take into Consideration the Change in other design results. Also Gain can be



increased by increasing (gm) of the input stage . To Conclude, a Higher Gain could be obtained

Figure 2.33 Gain (AC Response)

but the Power Consumption will increase to save the same matching condition at input

Now, as it is shown in (Figure 2.35), it is Clear that we are achieving a Noise Figure Below (3.7 dB) Across the Whole Range. As we know from Equation 2.8 that to have a higher value of Gain

will lead to a lower value for the Noise Figure. We also may think that designing a Differential LNA will increase the Noise due to the increase of the Number of Noisy Components, but this is wrong because the Gain will Also Increase leading to the same value of Noise Figure for single Ended LNA.

We were able to achieve a Noise Figure Value Lower than 2.5dB as its shown in (Figure 2.34) but due to Power Requirements(15 mW as a Maximum Power) , we weren't able to achieve this requirement in our design as shown in (Figure 2.35 Noise Figure in dB

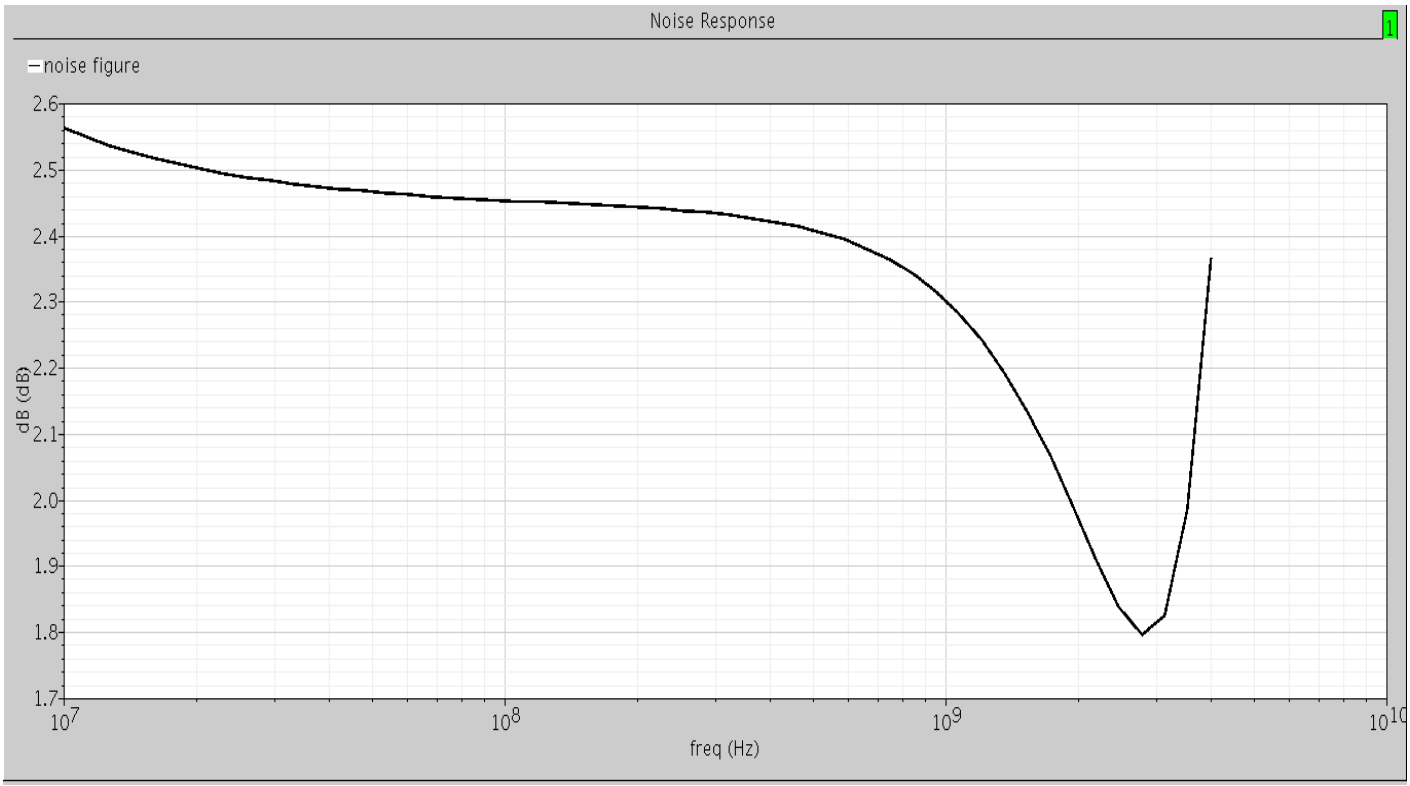


Figure 2.34 Noise Figure less than 2.5dB

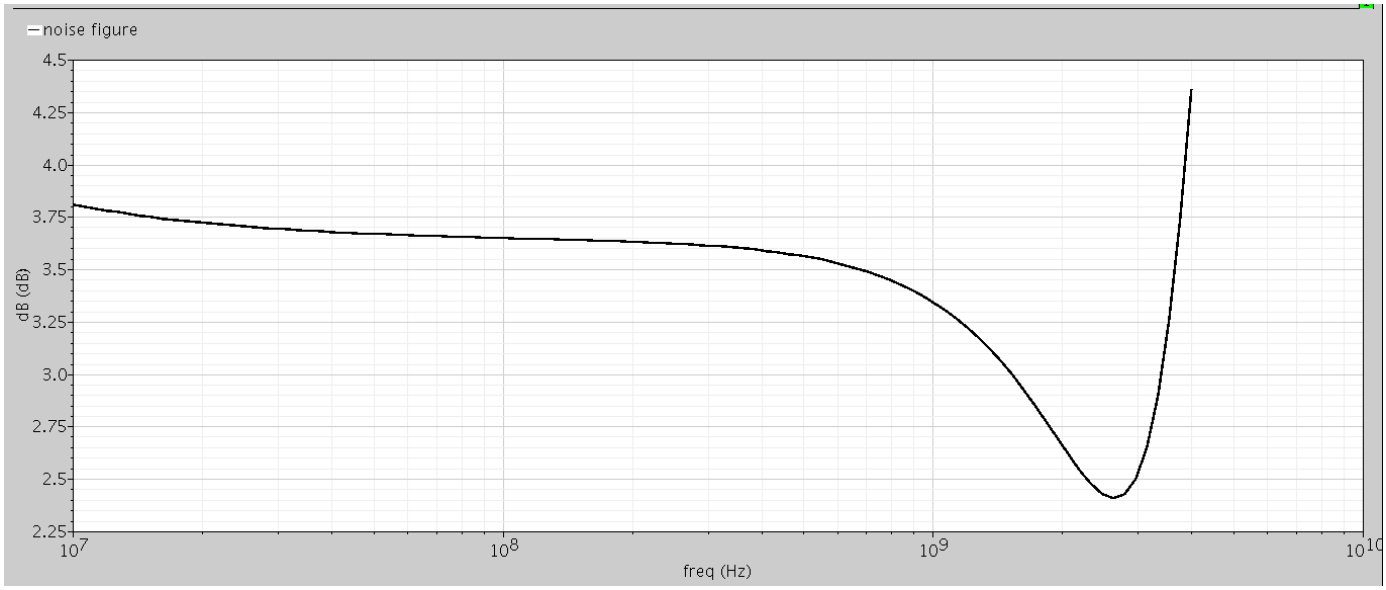


Figure 2.35 Noise Figure in dB

To Decrease the Noise Figure, we Make a Noise Summary and see the Contribution of each component in the Total Noise. The Noise of the Mosfet can be decreased by increasing (gm).

To Conclude : if we want to achieve a Lower noise figure based on this design, the Power Requirements have to be changed , such than the other requirements could be achieved too.

Now, let's consider the input matching. Input matching is always expressed In terms of the S parameters S11. If the Circuit Input is matched to the source, the value of the S11 should be as lowest as Possible, which means that there will be a little reflection and the Power Transfer is maximized. As it is shown in (Figure 2.36), we have achieved S11 to be Less than -12dB till 2.634 GHz.

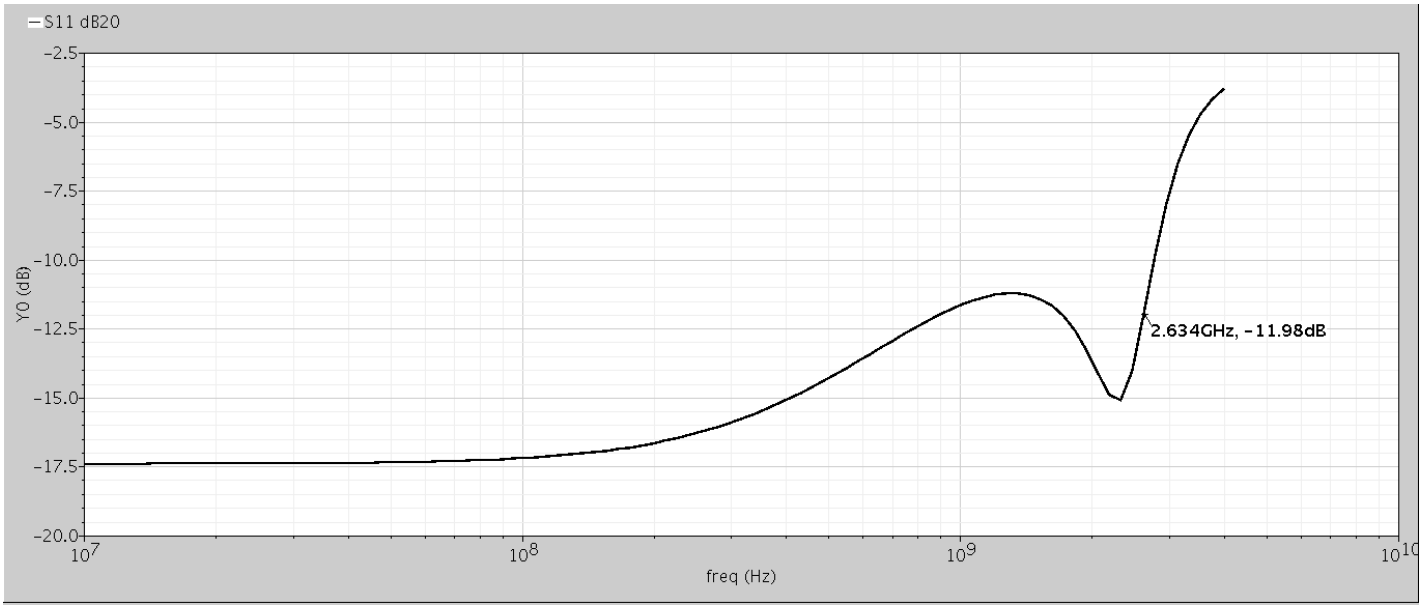


Figure 2.36 S11 in dB

Finally, talking about the Linearity Check , as its Shown in (Figure 2.37) the IIP3 is (701.671m dBm) with a worst case Value of (-1.28 dBm). All these Specifications were get with a Power Consumption almost 15mw as shown in (Figure 2.38)

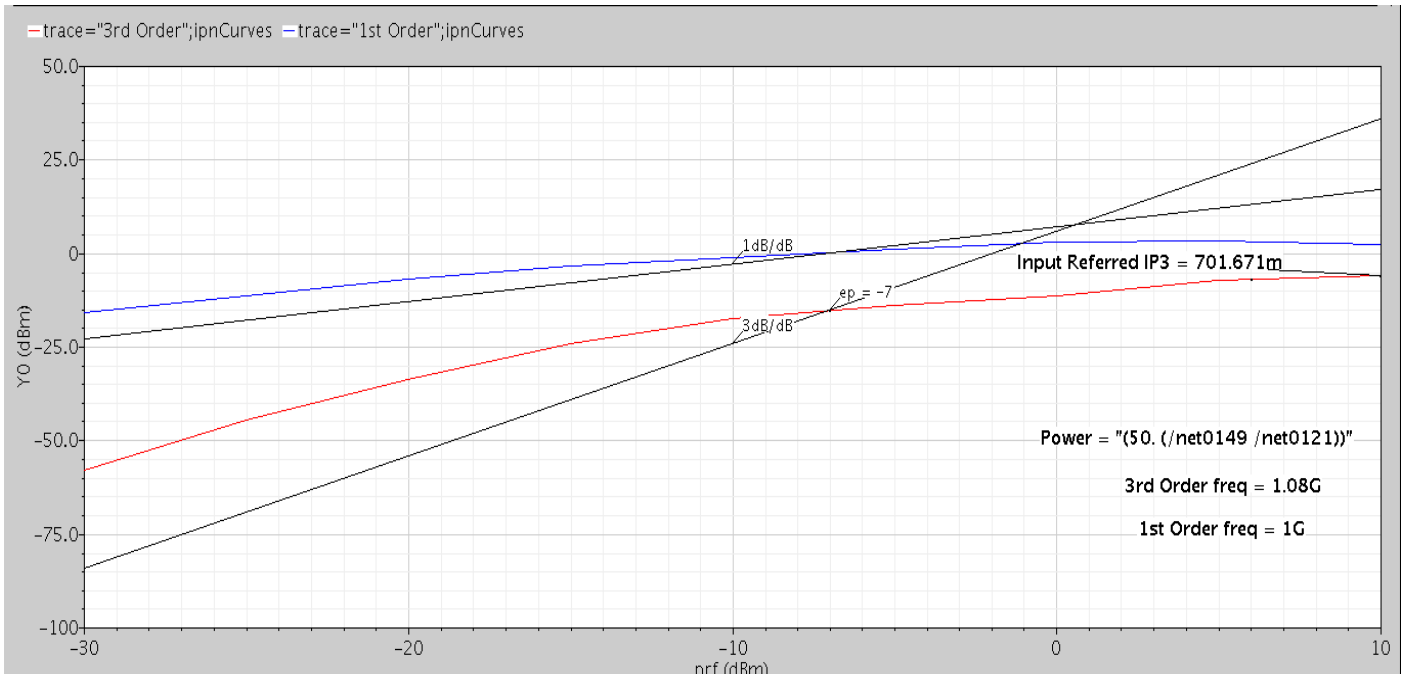


Figure 2.37 IIP3 Curve

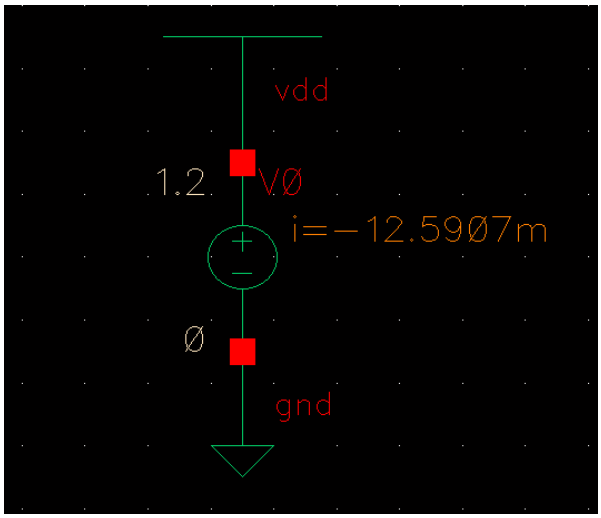


Figure 2.38 Power Consumption

To Summarize The Design, in the Following Tables we will find all the Values of The Resistances, Mosfets , Inductors ,….. etc. Also, The Specifications which we got .

Component	Values
M0,M4	Total Width =120u , L=180n, Mult=5
M3,M7	Total Width =268.8u , L=130n , Mult=4
M1,M5	Total Width=220u , L=180n
M8	Total Width =105u , L=130n , Mult =3
M6,M2	Total Width =60u , L=130n
Vdc	1.2 V
Ideal Current Source	100 u
RL	100 Ω
CL	50f
Lg	3.15 n
Rf	140Ω

Table 2.5 Design Values

The Specifications we achieved

Parameter	Restriction
Power Consumption	**15 mW**
Bandwidth	**40Mhz – 2.64Ghz**
Gain	**15dB**
S11	**Less than -12dB**
Noise Figure	**Less than 3.6 dB**
IIP3	**701m Dbm**

Table 2.6 Specs Achieved

As shown in (Table 2.6) , it's clear that all the Specs were achieved except the Noise Figure . Noise Figure can be achieved under a condition of Higher Power Consumption. Our LNA Is a Wide Band LNA (40M – 2.64 Ghz) which Supports the TV Band .

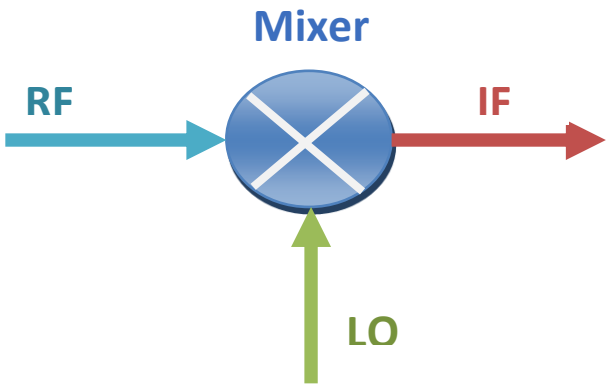
3 Mixers:

3.1 Mixers Theory:

Mixers are essential to most communications systems as they perform the necessary frequency translation of signals. Most information signals travel at frequencies much larger than that of human speech or digital data in order to maximize bandwidth and minimize propagation power and antenna size. Frequency translation is also done to make effective use of bandwidth and organization of frequency allocations for different types of propagating signals. This high frequency or radio frequency (RF) must be down-converted back into a lower intermediate frequency (IF) so that the data can then be interpreted. This down-conversion is realized by the multiplication of the incoming RF signal by a local oscillating (LO) frequency.

As such Mixers have 3 distinctly different ports, in the receive path, the down-conversion mixers senses the RF signal at its “RF port” and the local oscillator at its “LO port”. The output is called the “IF port” in a heterodyne receiver or the “Baseband port” in a direct conversion receiver.

The basic functionality of the mixer operation relies on the multiplication of two signals in the time domain.



The mixing result produces two located at the LO+RF signal and LO-RF frequency. One signal is the wanted IF signal and the other is the unwanted signal

$$V_{RF} = A\cos(\omega_{RF})t \qquad \textit{Equation 3.1}$$

$$V_{LO} = B\cos(\omega_{LO})t \qquad \textit{Equation 3.2}$$

$$V_{IF} = [A\cos(\omega_{RF})t] * [B\cos(\omega_{LO})t] \qquad \textit{Equation 3.3}$$

$$V_{IF} = \frac{AB}{2}[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t] \qquad \textit{Equation 3.4}$$

3.2 Active and Passive topologies:

Mixers can be either passive or active, so we had to know the difference between them and the properties of each to choose a suitable one for our design.

The **main difference** between mixer types is that the active mixer consumes power, whereas the passive one does not.

From the **RF metrics point of view**, the main difference is in the **linearity performance** and the **required LO drive level.**

As Shown in (Table 3.1 Active Vs Passive Mixers a comparison between Active and Passive mixers from point of view of RF parameters:

Active Mixers	Passive Mixers
Provides Gain	Provides no Gain
Good LO to RF Isolation	Good LO to RF Isolation
Requires low LO drive	Requires Strong LO Drive
higher NF	Reasonably Low Noise
lower input linearity	higher Input Linearity

Table 3.1 Active Vs Passive Mixers

Also we refer to ([5] , Comparison of active and passive mixers) which made a comparison between active and passive mixers with real values and simulation to make sense of the difference between the 2 topologies.

As shown in (Figure 3.1 [5] Passive Vs Active Mixers Simulation results of Active and Passive Mixers:

	Passive Mixer	Active Mixer
Supply voltage (V)	1.2	1.2
DC Power consumption (mW)	0	4.8
RF-to-IF conversion gain (dB)	-4.6	8
SSB Noise Figure (dB)	9	9
$P_{-1}(dBV)$	-10	-21
IIP3 (dBV)	-5.4	-11.5
LO power level (dBV)	-9	-9
LO frequency (GHz)	2.1375	2.1375
RF power level (dBV)	-9	-9
RF frequency (GHz)	2.1325	2.1325

Figure 3.1 [5] Passive Vs Active Mixers

It is clear that main differences between active and passive mixers are in the **Conversion Gain** and **linearity**. Active mixers give high conversion gain and low linearity while passive mixers give high linearity and no conversion gain.

3.3 Performance Parameters:

3.3.1 Conversion Gain:

The voltage conversion gain of a mixer is defined as the rms voltage of the signal at the IF frequency divided by the rms voltage of the signal at the RF frequency.

$$V_0 = V_{RF} * V_{LO} \qquad \textit{Equation 3.5}$$

$$V_{RF} = V_{RF}\cos(\bar{\omega}_{RF} * t) \qquad \textit{Equation 3.6}$$

The LO signal is a square wave from -1 to 1, after doing fourrier series the signal will be have a fundamental amplitude of 4/π.

$$V_0 = gmR_L\left(\frac{4}{\pi}\right)[\frac{1}{2}\cos(\omega_{RF} - \omega_{LO})t + \frac{1}{2}\cos(\omega_{RF} + \omega_{LO})\,t \ldots] \qquad \textit{Equation 3.7}$$

Then the **Conversion gain** will be:

$$\frac{\boldsymbol{V_0(t)}}{\boldsymbol{V_{rf}(t)}} \approx \boldsymbol{gmR_L\left(\frac{2}{\pi}\right)} \qquad \textit{Equation 3.8}$$

3.3.2 Linearity:

The non-linear properties of circuitry can be described in the following power series equation:

$$v_0 = k_0 + k_1 v_{in} + k_2 {v_{in}}^2 + k_3 {v_{in}}^3 + k_4 {v_{in}}^4 \ldots \qquad \textit{Equation 3.9}$$

Where Vin equals:

$$v_{in} = x_1 + x_2 = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \qquad \textit{Equation 3.10}$$

Noting that the first three terms will yield a sufficiently accurate characterization, the output of the power series equates to:

$$v_0 = k_0 + k_1(x_1 + x_2) + k_2(x_1 + x_2)^2 + k_3(x_1 + x_2)^3 \qquad \textit{Equation 3.11}$$

$$v_0 = k_0 + k_1(x_1 + x_2) + k_2({x_1}^2 + 2x_1x_2 + {x_2}^2) + k_3({x_1}^3 + 3{x_1}^2x_2 + 3x_1{x_2}^2 + {x_2}^3) \qquad \textit{Equation 3.12}$$

The expanded second order and third order terms are:

$$(x_1 + x_2)^2 = (x_1 2 + 2x_1x_2 + x_2 2) \qquad \textit{Equation 3.13}$$

HD2 MIX HD2

$$(x_1 + x_2)^3 = ({x_1}^3 + 3{x_1}^2x_2 + 3x_1{x_2}^2 + {x_2}^3) \qquad \textit{Equation 3.14}$$

HD3 IM3 IM3 HD3

The second order term MIX, also known as IM2 (second order intermodulation) produce the nonlinearity needed for frequency translation. The undesired terms HD3 and IM3 produce undesired nonlinear effects such as gain compression and intermodulation distortion.

3.3.2.1 *Third Order Intercept Point IP3:*

Although mixers are based on a fundamental non-linear principle, it is important that the mixer must also be able to amplify a range of incoming signals in a linear fashion. A commonly used measure of linearity is the third order intercept (IP3) point. This measure describes the real-world scenario of having two input signals spaced relatively close together on the frequency spectrum fed into the mixer, one being the desired signal in the channel of interest and the other being the undesired signal (an interfering signal of the adjacent channel). The collaborated effects of these signals are known as intermodulation. Most critical are third-order intermodulation (IM3) components that appear at the output of the mixer, their frequencies of 2ωRF1 - ωRF2 and 2ωRF2 - ωRF1 may lie within the passband of the desired IF, subsequent to mixing operation. Ideally this is to say that as the RF input power increases, the output power of the undesired IM3 signals will intersect the output power of the desired signal. It is this intersection that is referred to as the IP3 point. In reality, since either of the signals will saturate and this intercept point will never occur, however an extrapolation of their linear slopes will serve as a good estimate. If the IP3 is referenced to the input power of the mixer, it is known as the input third-order intercept point (IIP3).

In other words, the Third Order Intercept Point (IP3) is a theoretical point at which the fundamental and third order response intercepts. This point is found when two signals that are very close in frequency are applied to the mixer. Third-order intemodulation (IM3) appears at the output. The IM3 components will be at 2f1 – f2 and 2f2 – f1 which is in the vicinity of the desired frequency causing intermodulation distortion.

Figure 3.2 shows the fundamentals and Images signals:

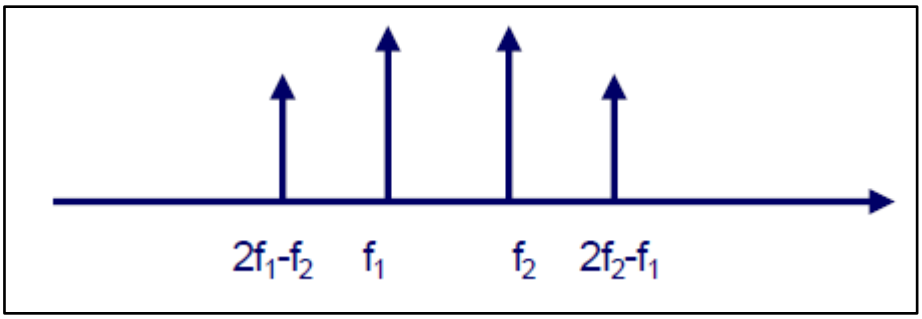


Figure 3.2 [2]

Figure 3.3 [2]: IIP3 shows the IIP3 curve:

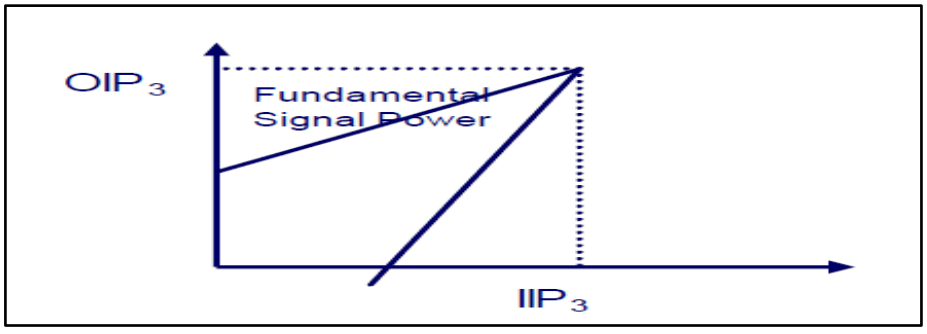


Figure 3.3 [2]: IIP3

3.3.2.2 *1dB Compression Point:*

Characterization of linear behavior in RF circuits requires quantification of the maximum input range for a given design stage. Ideally one would like the output power to be linearly proportional to a given input power. However, due to the effects of noise and intermodulation distortion, mixer behavior will deviate from desired linearity, entering a region of saturation or compression. The 1dB compression point as shown in (Figure 3.4 [2] : 1dB Compression Point is simply described as the point where the output power is 1dB less than that of the ideal gain for a given input power.

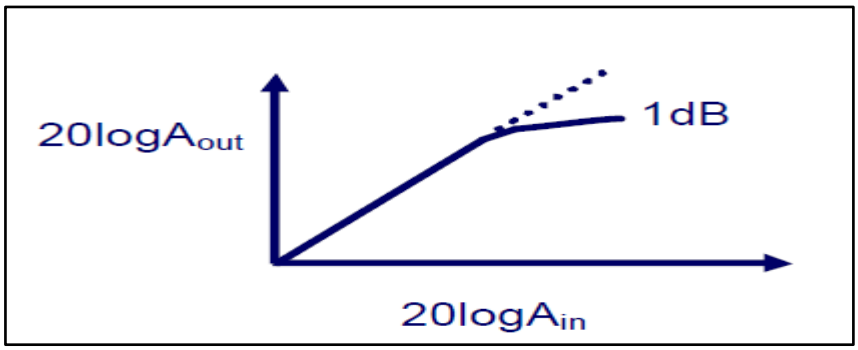


Figure 3.4 [2] : 1dB Compression Point

1-dB compression and the third order intercept point (IP3) are related to each other. By knowing one, the other can be approximated.

Then, Linearity describes the region of operation where the output signal varies proportionally to the input signal.

3.3.2.3 *Spurious Free Dynamic Range (SFDR):*

Since mixers can accommodate a wide range of signal strengths, (weak signals are governed by the noise floor while strong signals are governed by the 1dB compression point) a measure is introduced so as to quantify the overall usable range, known as the spurious-free dynamic range (SFDR). The SFDR of a system as shown in (Figure 3.5 [4]: SFDR is defined as a ratio where the input power level is distinguished by the intersection of the IM3 term and the minimally detected signal.

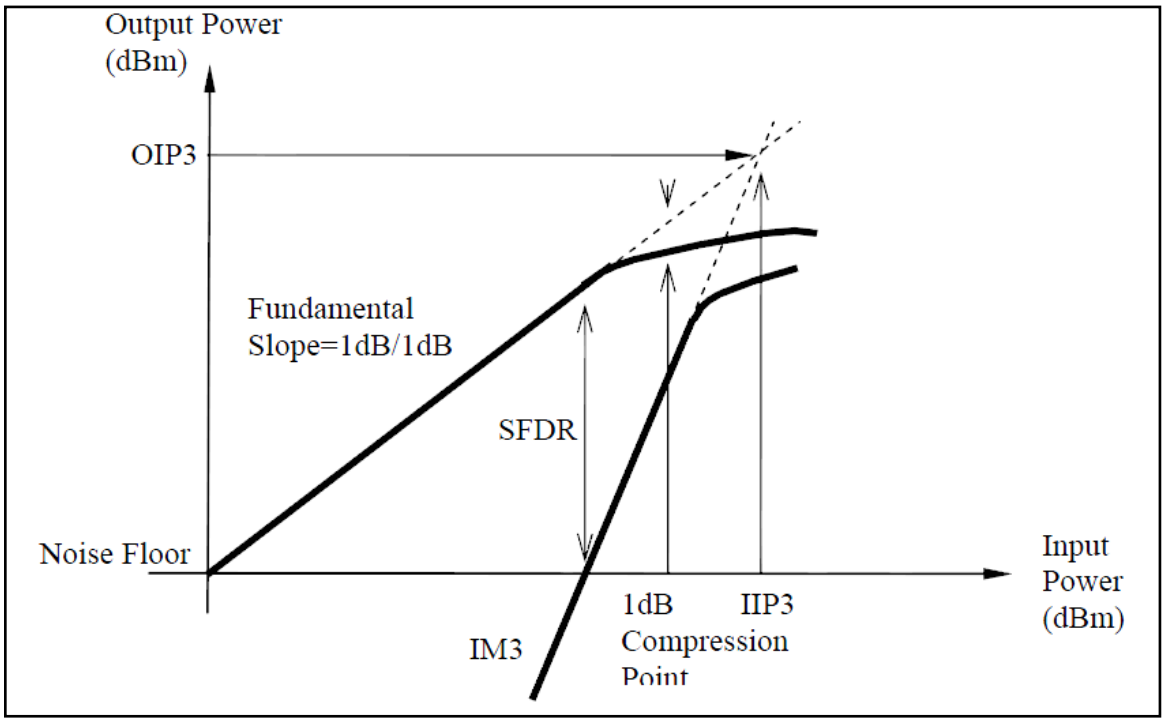


Figure 3.5 [4]: SFDR

3.3.3 Noise:

Noise is defined as any random interference that is unrelated to the signal of interest. The different types of noise in all circuits are **Thermal noise**, **Flicker noise**, **and Shot noise** as shown in (Figure 3.6 [13]: Noise Types.

Thermal noise: From resistors and channel resistance of MOSFETs.

Flicker noise: Arising from random trapping of charge at the oxide-silicon interface of MOSFETs.

Shot Noise: Associated with the transfer of charge across an energy barrier.

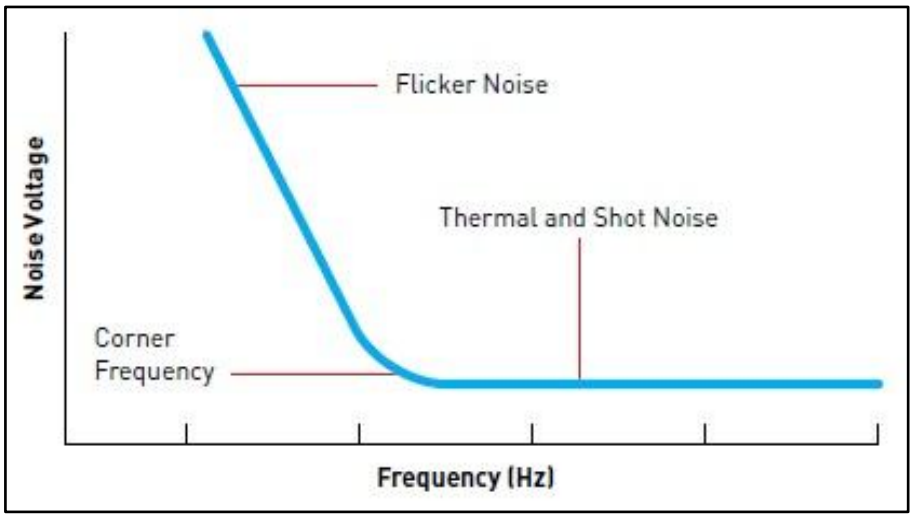


Figure 3.6 [13]: Noise Types

In addition, mixers also suffer noise from the thermal noise generated by the output resistance of the LO and noise contributed by the switching pairs.

3.3.3.1 *Noise Figure:*

Noise figure (NF) measures how much the signal to noise ratio (SNR) of a signal degrades because of the added noise as it passes through the mixer.

The NF of the mixer is defined as the total SNR at the RF frequency divided by the SNR at the IF frequency.

$$NOISE\ FIGURE = 10 \log\left(\frac{SNR_{in}}{SNR_{out}}\right) \qquad \textit{Equation 3.15}$$

Noise figure, for a mixer, considers only the noise associated with the IF (fLO-fRF) frequency, according to the IEEE's NF definition for mixers, it assumes that there are no noise contribution at the image frequency (2fLO-fRF) due to mixing.

The IEEE definition of noise figure states that the numerator of the noise figure expression should represent ALL output noise while the denominator should only represent noise translated from frequency bands that contain signal information.

SSB system (i.e. a system that processes information found in only one down converted frequency band) the denominator of the noise figure expression represents the input noise found in only one of the two sidebands as shown in (Figure 3.7 [3]: SSB.

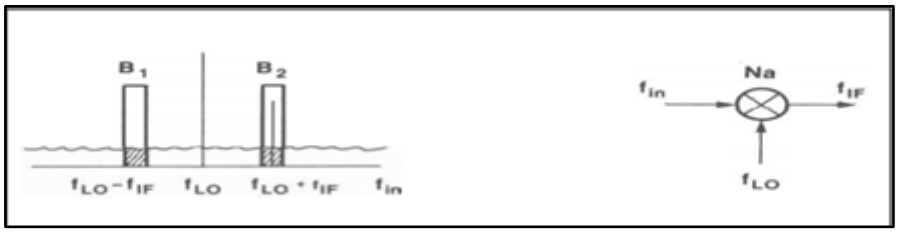


Figure 3.7 [3]: SSB

$$F_{SSB} = \frac{N_a + \frac{KT_0B_1}{L_1} + \frac{KT_0B_2}{L_2}}{\frac{KT_0B_2}{L_2}} \qquad \textit{Equation 3.16}$$

In DSB systems (i.e. systems that down-convert useful information from two frequency bands) the denominator of the noise figure expression represents input noise from two frequency bands as shown in (Figure 3.8 [3]: DSB

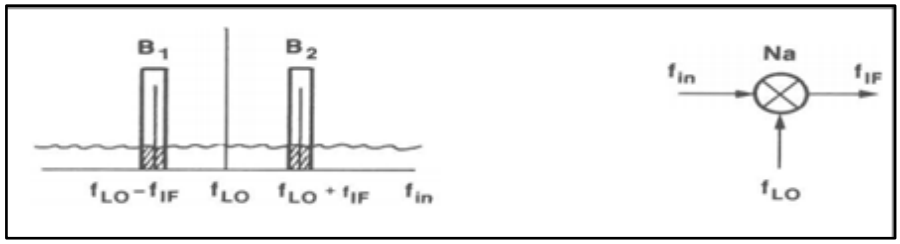


Figure 3.8 [3]: DSB

$$F_{DSB} = \frac{N_a + \frac{KT_0B_1}{L_1} + \frac{KT_0B_2}{L_2}}{\frac{KT_0B_1}{L_1} + \frac{KT_0B_2}{L_2}} \qquad \textit{Equation 3.17}$$

For a mixer, SSB noise figure will be 3dB higher than DSB noise figure.

$$F_{SSB} = \frac{N_a + 2\left(\frac{KT_0{}^2}{L}\right)}{\frac{KT_0B}{L}} \qquad \textit{Equation 3.18}$$

$$F_{DSB} = \frac{N_a + 2\left(\frac{KT_0{}^2}{L}\right)}{2\left(\frac{KT_0}{L}\right)} \qquad \textit{Equation 3.19}$$

$$\therefore F_{SSB} = 2F_{DSB} \qquad \text{Equation 3.20}$$
$$\therefore (F_{SSB})_{dB} = (F_{DSB})_{dB} + 3\ dB$$

3.4 Mixer Topologies:

3.4.1 Single-Balanced Mixer:

A mixer with a single-ended IF signal shown in (Figure 3.9 [2] : Single Balanced Architecture is called a single-balanced mixer. This configuration is rarely used because it is more susceptible to noise in the LO signal. Its main drawback is the LO-IF feed-through. The low pass filter following the mixer may not properly suppress the LO signal without affecting the RF signal.

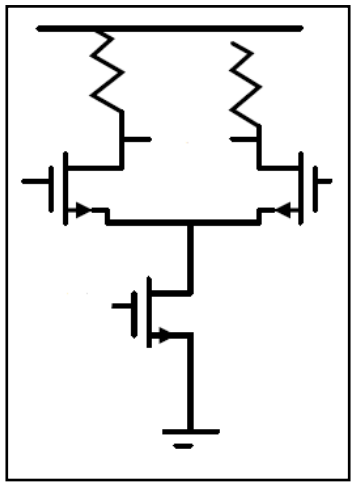


Figure 3.9 [2] : Single Balanced Architecture

3.4.2 Double Balanced Mixer:

Double Balanced Mixers are used to prevent the LO products from reaching the output. It is essentially two single-balanced circuits with the RF transistors connected in parallel and the switching pair in anti-parallel. Therefore, the LO terms sum to zero and the RF signal doubled in the output. This configuration provides a high degree of LO-RF isolation easing filtering requirements at the output. Double Balanced mixers shown in Figure 3.10 [4]: Double Balanced Architecture are less` susceptible to noise than the single-balanced mixers because of the differential RF signal, it is also known as the Gilbert Cell Mixer.

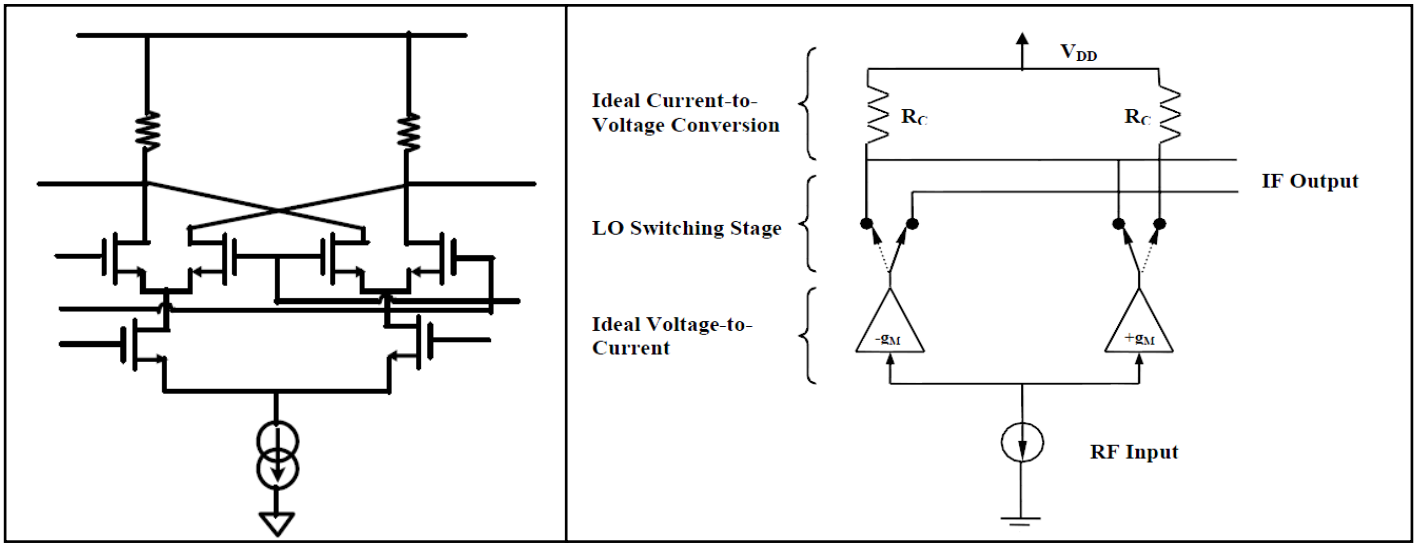


Figure 3.10 [4]: Double Balanced Architecture

3.4.2.1 *Gilbert Cell Mixer Mechanism:*

The Gilbert Cell has two pairs of transistors connected in parallel; this provides a double balanced mixer which attenuates the feed-through RF and LO components produced by the mixer. When two signals are mixed, the output will be the wanted frequency (the mixing) and the feed-through. Some of the feed-through is cancelled out due to a 180 degrees phase shift. The two transistors

with the IF terminals act as an amplifier increasing the gain of the signal before mixing. Two resistors, called emitter degeneration resistors, are connected between them. It can be adjusted to increase or decrease linearity or gain. The output is taken at the difference between IF- and IF+.

No input and output impedance matching are required for the mixer. A filter with high input impedance will be added at the output of the mixer to filter out the unwanted high frequency produced.

3.5 Design Procedures:

The design procedure of the mixer is based on the required specifications. So we choose the double balanced architecture (Gilbert Cell) to meet the high Gain and Noise Figure required. We started by trying several Mixers architectures with different topologies. Adjusting circuitry for the purpose of optimizing a particular performance parameter may serve to unintentionally degrade the performance of the other parameters. It is important to monitor all of the performance parameters throughout the design process.

The first stage in the design process was to approximate values for each circuit element in the mixer.

- **Transistor Operation Regions:** All transistors are to operate in the saturation region.

For this requirement to be met, two expressions must be satisfied:

$$V_{GS} \geq V_{TH} \qquad \textit{Equation 3.21}$$

$$V_{DS} \geq V_{GS} - V_{TH} \qquad \textit{Equation 3.22}$$

Once these conditions have been satisfied it is possible to approximate the transistor behavior in the saturation region through the following equation:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad \textit{Equation 3.23}$$

The parameters which remain fixed in the above equation are μn, Cox, L and VTH. The parameters which can be adjusted for optimization are ID, W and VGS.

- **Transistor Biasing:** A common practice in RF IC design is to ensure that the gate bias voltage relative to the source voltage VGS is between 200mV and 400mV above the threshold voltage VTH.
- **Gain:** There are several factors that affect the gain of the mixer:

✓ Transconductance of the input stage.

✓ Current in the input stage.

✓ Ideality of switching stage.

✓ Resistance of the output stage.

✓ Poles and Zeroes of the system.

- **Linearity:** A circuit will exhibit nonlinear characteristics when there is a variation in the small signal gain with respect to the input signal level. The resulting output signal will be distorted or compressed. There are three phenomena which affect linearity in the mixer circuit.

The first source of compression occurs at the driver stage. If the applied signal at the driver stage is greater than the maximum differential input compression will take place. Linearity can be improved in this situation by decreasing the driver stage transistor ratio and increasing the bias current. Trade-offs to these corrections will serve to increased overdrive voltage increased power dissipation and again decreased gain respectively

The second source of compression occurs at the output load. If the output load resistor size is too large, the voltage drop VDS across the switching transistors will decrease thus forcing the switching transistors out of saturation and into the triode region of operation (VDS < VGS – VT). Reducing the size of the load resistors will move the DC output voltage to a higher level, this serves to reduce the gain as previously discussed. Reducing the bias current at switching stage will help solve this problem without severely affecting the gain.

The third source of compression occurs at the driver stage drain voltage. As in the switching transistors, the driver transistors are required to operate in the saturation region of operation. The voltage across these transistors Vds1 & Vds2 are set by the DC voltage level but it causes a reduction in gain

- **Noise Figure:** Decreasing the size of the degeneration resistor will significantly improve the noise figure; however the linearity of the overall system will decrease.

3.5.1 Simulations Methods:

3.5.1.1 *Conversion Gain:*

We combine a PSS analysis with a periodic small-signal transfer function PXF analysis to determine the conversion gain of the down converter.

We had modify the schematic to set the RF source to a DC source to be sure the PSS analysis is the response of only the LO signal.

3.5.1.2 *Noise Figure:*

We combine a PSS analysis with a small-signal Pnoise analysis to determine the noise figure. Noise analysis calculates the total noise at the output of the circuit. The spectreRF Pnoise analysis computes the single sideband noise figure (-1 in this case). The total noise can vary with the number of harmonics you choose because each harmonic contributes a noise component.

We had modify the schematic to set the RF source to a DC source to be sure the PSS analysis is the response of only the LO signal.

3.5.1.3 *IP3:*

We insert 2 sinusoid tones with different frequencies and perform a PSS analysis to calculate the value of the IP3.

Here we inserted 2 tones spaced by 10 MHz, the power of the signals were swept for the same range during the PSS analysis, and then run the simulation to calculate the IP3 by selecting number of harmonics from a range of frequencies and choose the desired ones.

3.5.2 First Trial:

- 1.9GHz Gilbert Mixer in 0.18m CMOS
- Gilbert Mixer with resistors biasing the RF and LO ports to improve the gain and linearity.
- **Schematic**:

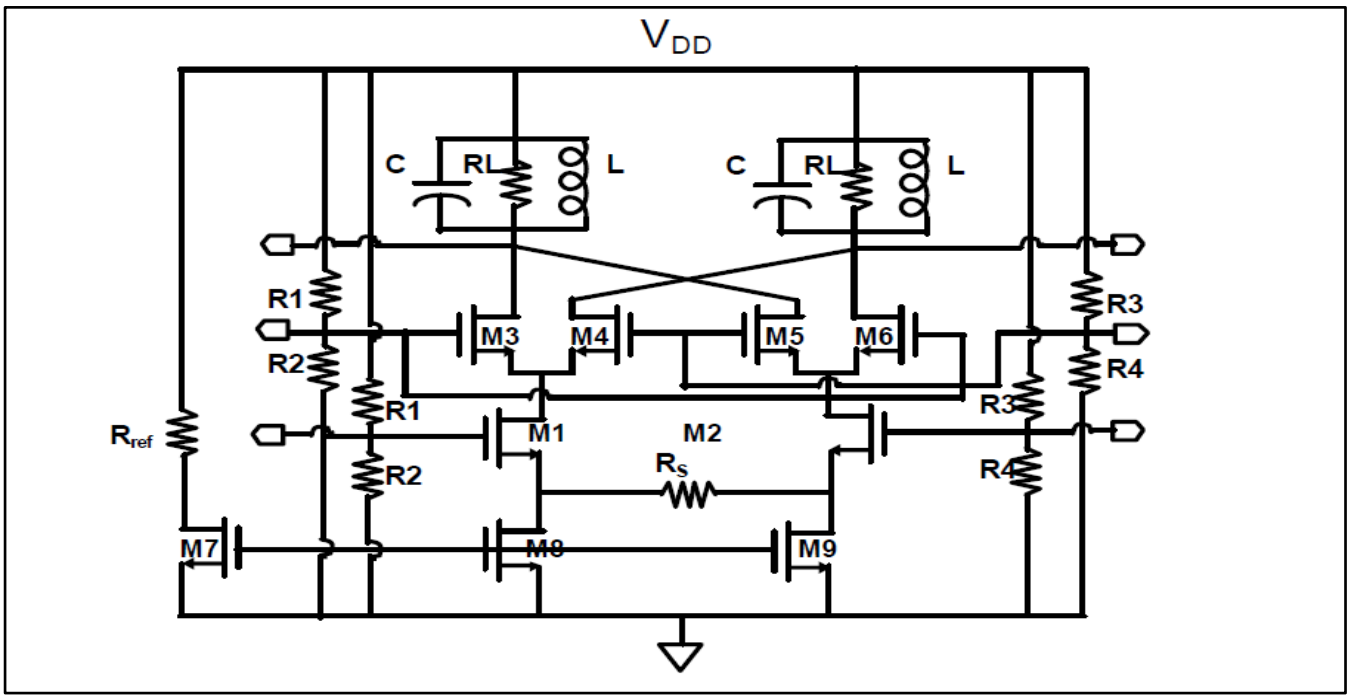


Figure 3.11 [2] : Schematic

- **Specifications**:

	Required Specifications	Achieved Specifications
Conversion Gain	0 to 4 dB	3.48 dB
IP3	>25 dBm	-9 dBm
Noise Figure	<18 dB	15.64 dB
Supply voltage	3.3v	3.3v

Table 3.2: Required Vs Achieved Specifications

- Simulation Results:

RF-LO-IF Signals:

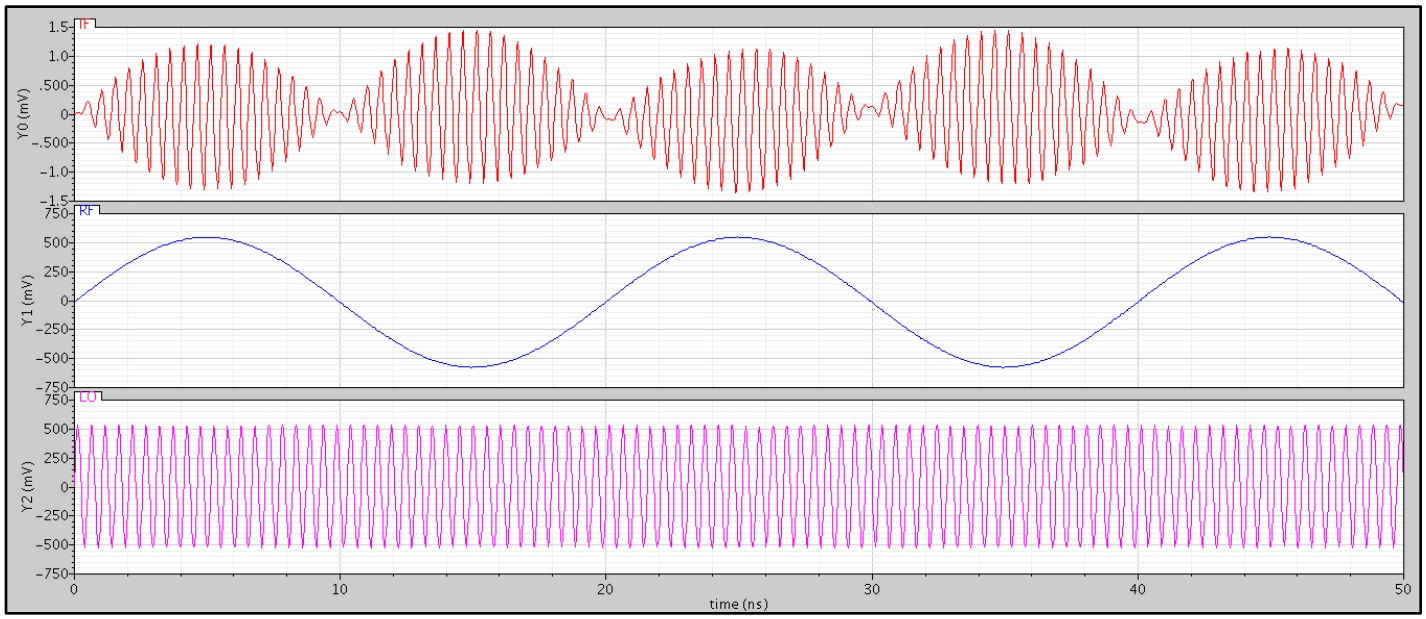


Figure 3.12: RF-LO-IF

Conversion Gain:

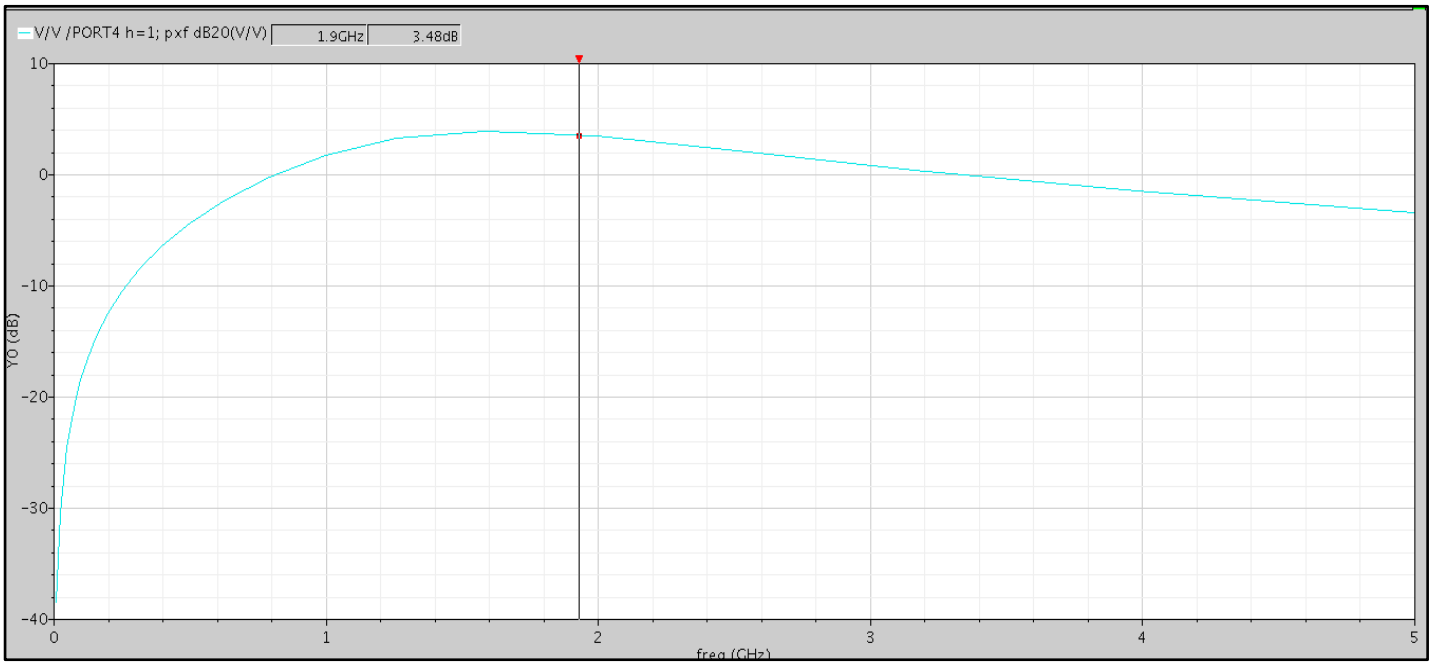


Figure 3.13: Conversion Gain

Noise Figure:

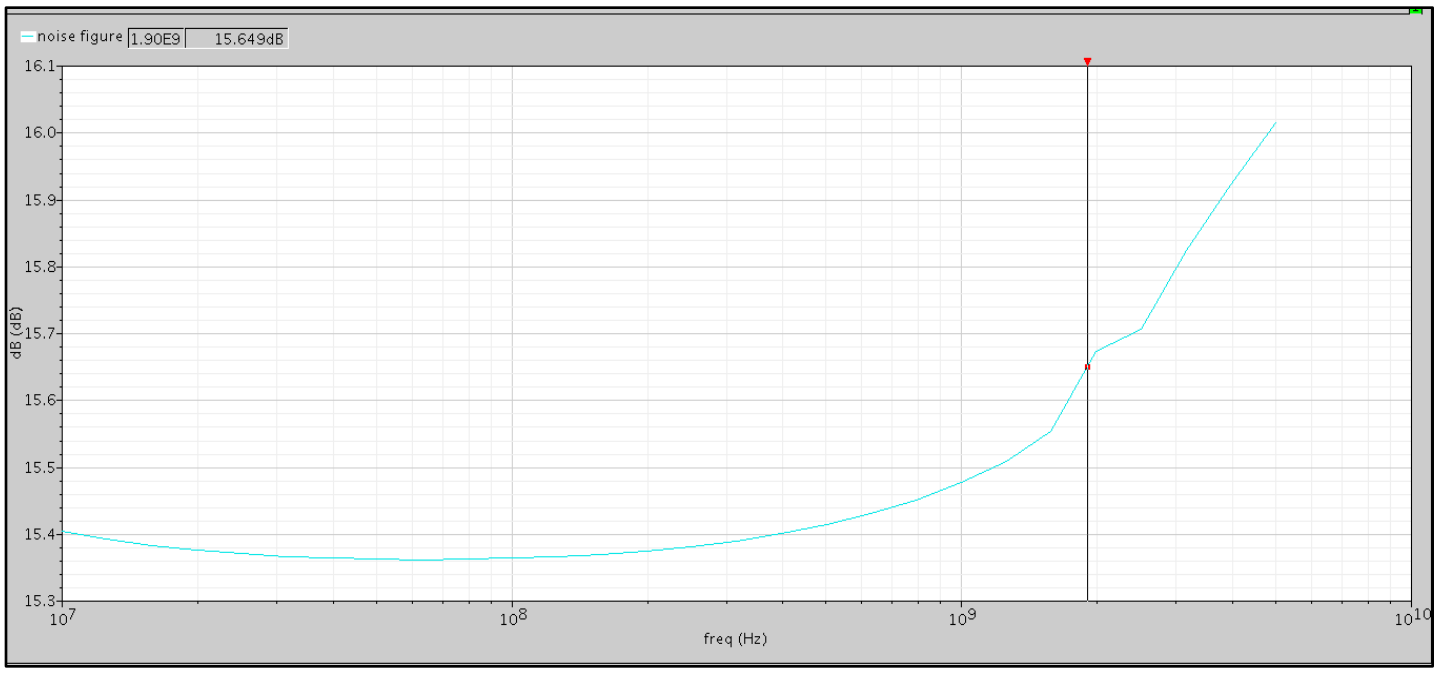


Figure 3.14: Noise Figure

IIP3:

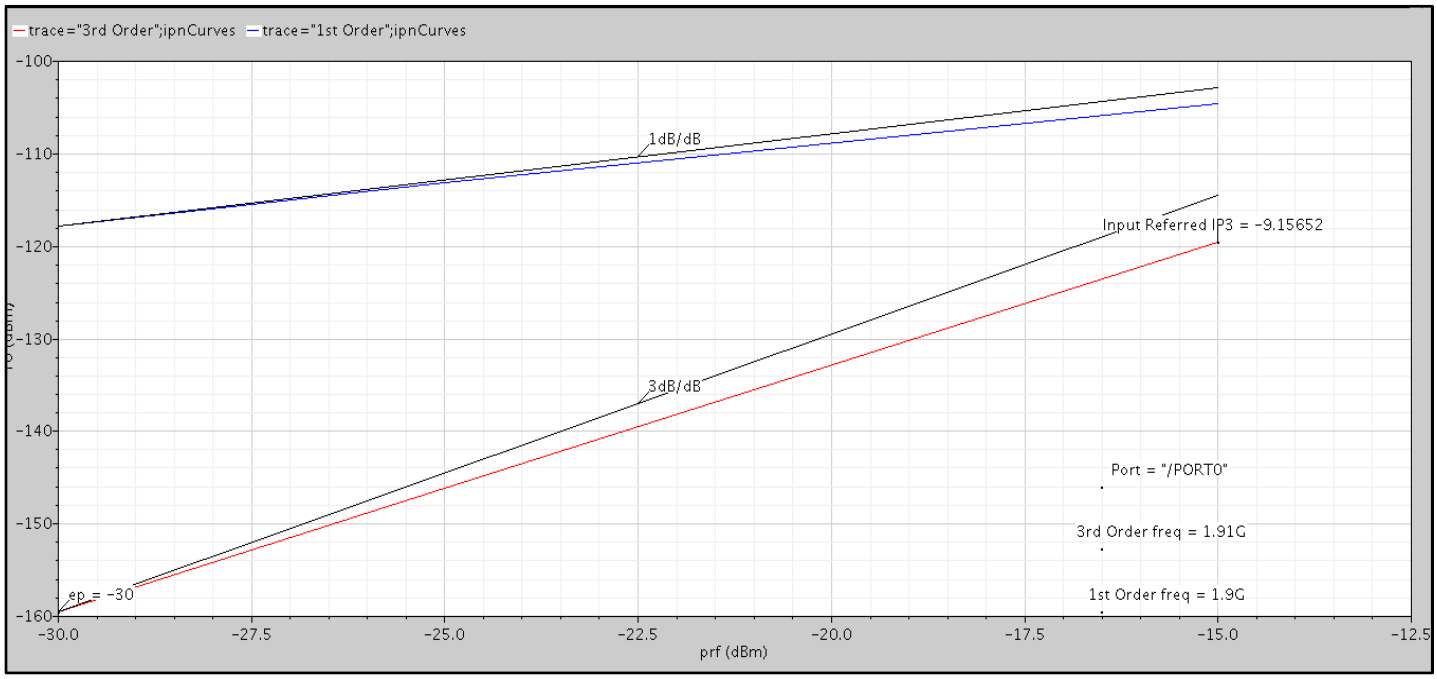


Figure 3.15: IIP3

3.5.3 Second Trial:

- 2.4 GHz Up-Conversion Mixers with current bleeding.
- Gilbert Mixer with Current-Mirror topology in the driver Stage and Current-Bleeding Technique in the switching stage.
- **Schematic**:

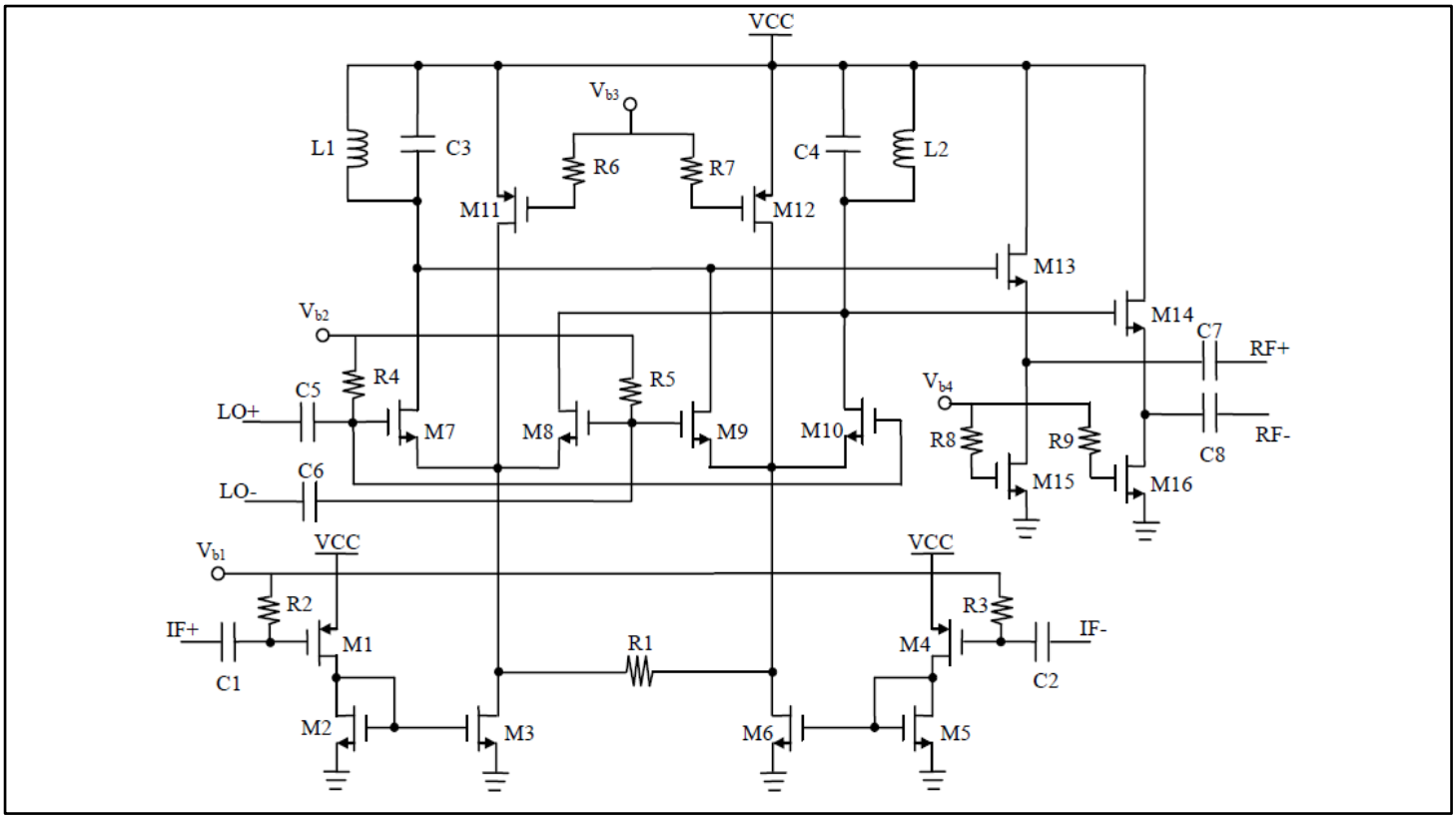


Figure 3.16 [3] : Schematic

- **Specifications**:

	Required Specifications	Achieved specifications
Technology	0.18um	0.18um
Conversion Gain	7 dB	8.95 dB
Noise Figure	11.9 dB	13.3 dB
Supply Voltage	1.2v	1.2v

Table 3.3: Required Vs Achieved Specifications

- Simulation Results:

IF-LO-RF:

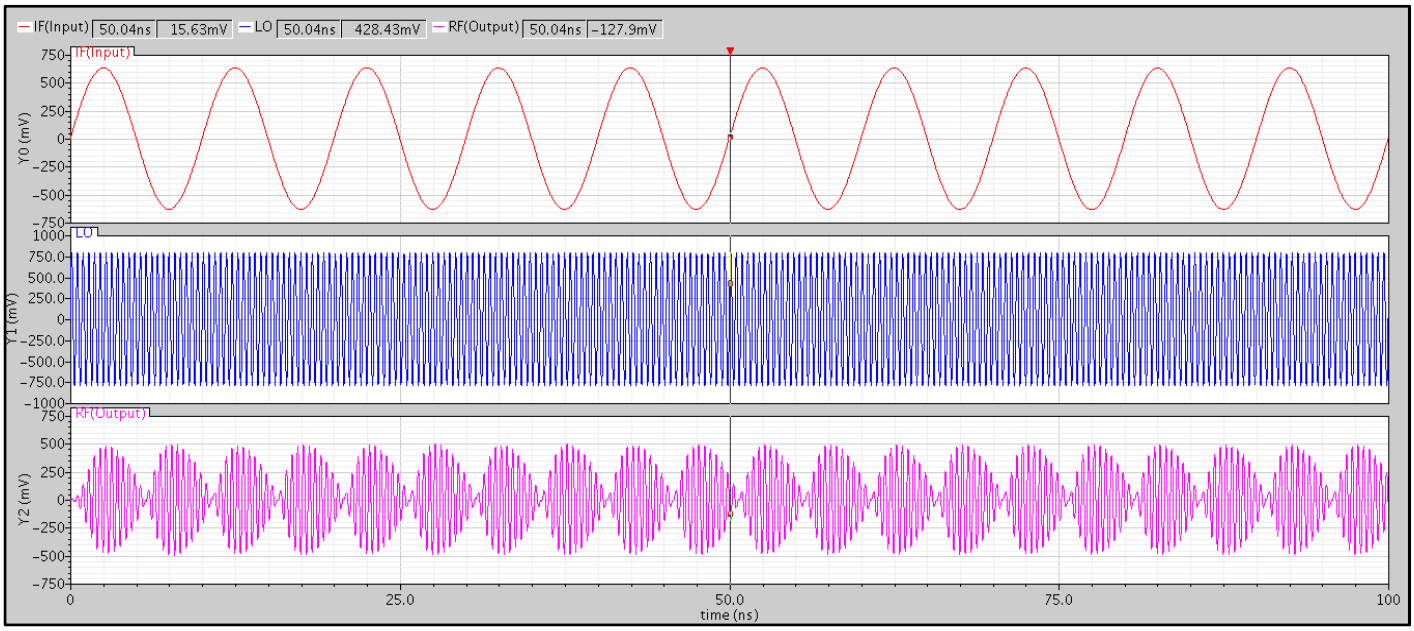


Figure 3.17: IF-LO-RF

Conversion Gain:

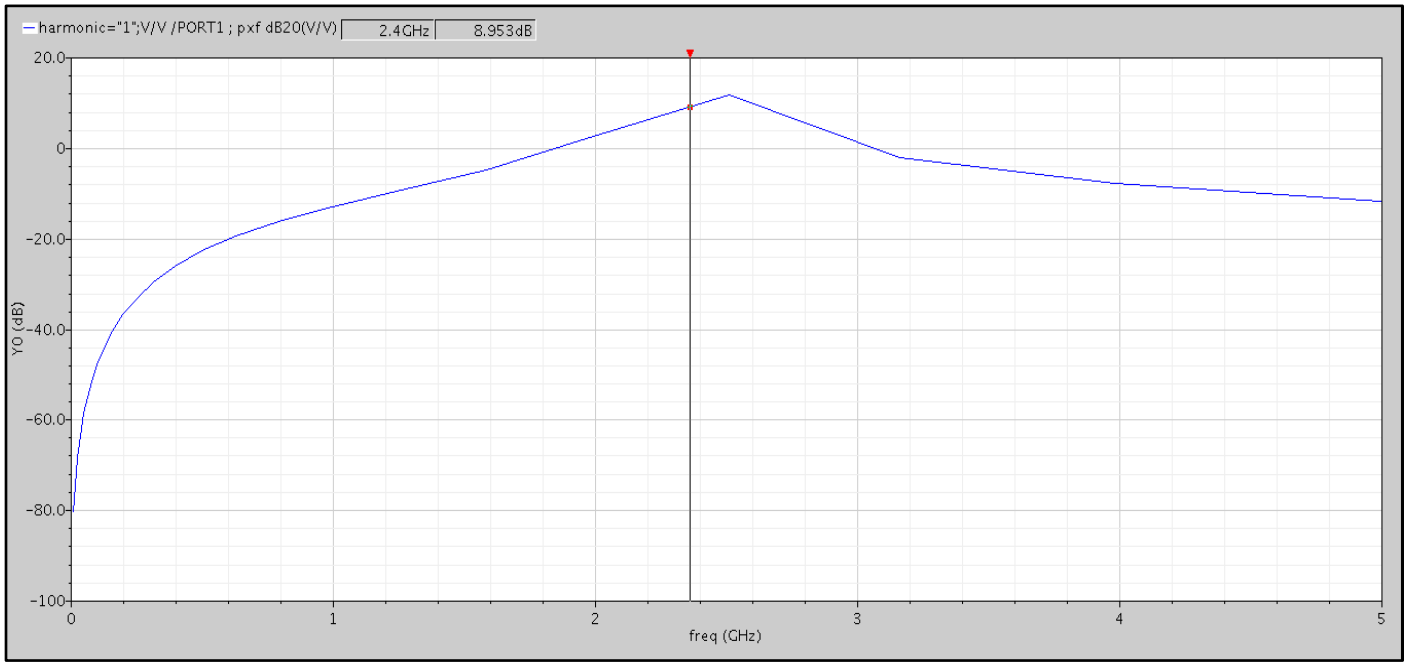


Figure 3.18: Conversion Gain

Noise Figure:

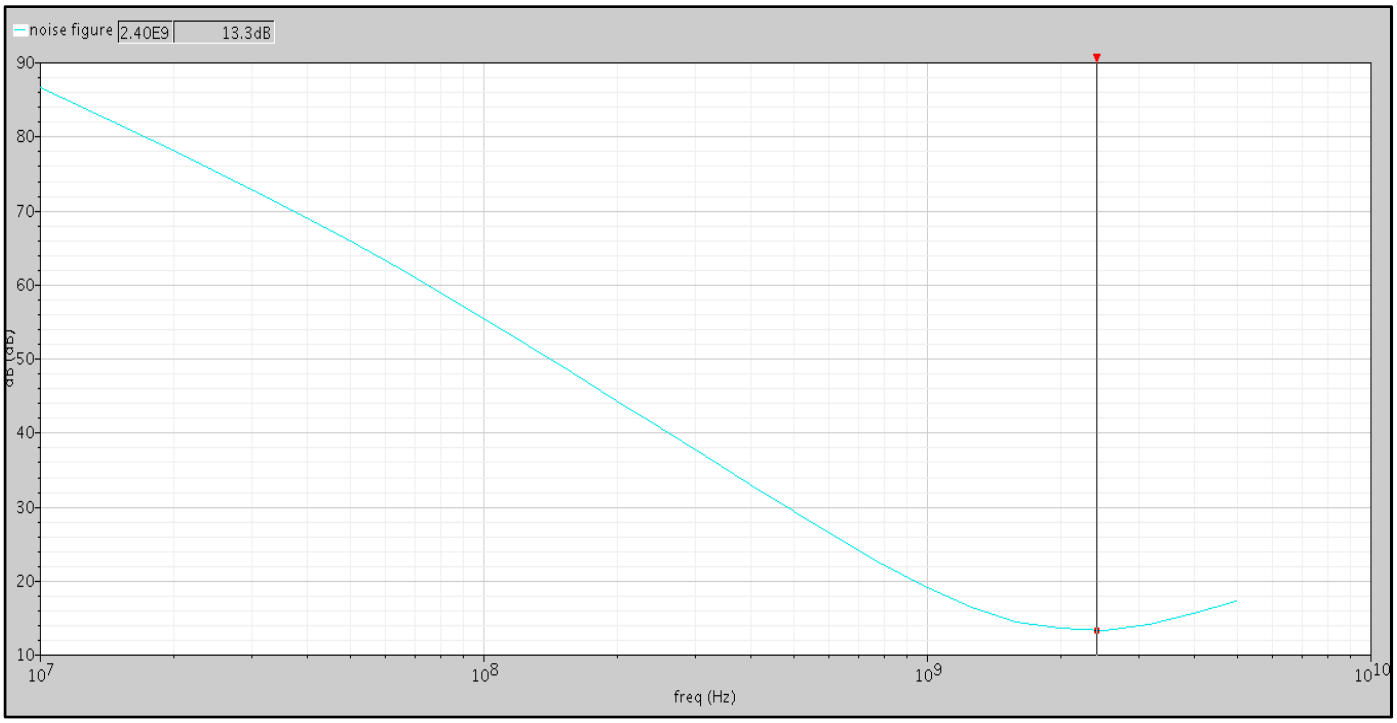


Figure 3.19: Noise Figure

3.5.4 Third Trial:

- 1.9Ghz Down Conversion Mixer in 0.18µ CMOS.
- Folded Mixer design whose main advantage is attributed to the strong improvement in mixer gain.
- Schematic:

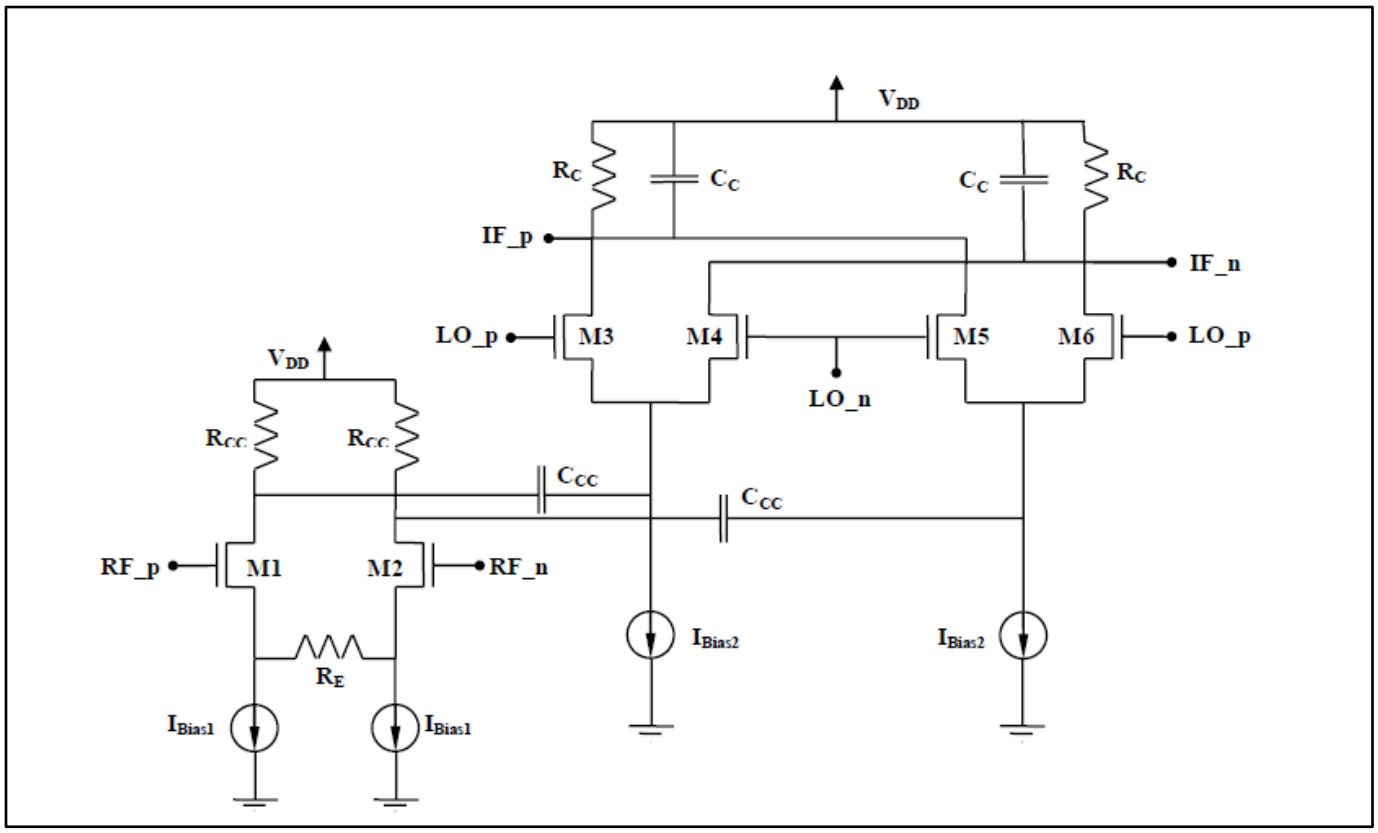


Figure 3.20 [4]: Schematic

- Specifications:

	Required Specifications	Achieved Specifications
Conversion Gain	>10 dB	11.6 dB
IP3	>5 dBm	-905 mdBm
Noise Figure	<10 bB	9.1 dB
Supply Voltage	3.3 v	3.3 v

Table 3.4: Required Vs Achieved Specifications

• Simulation Results:

RF-LO-IF:

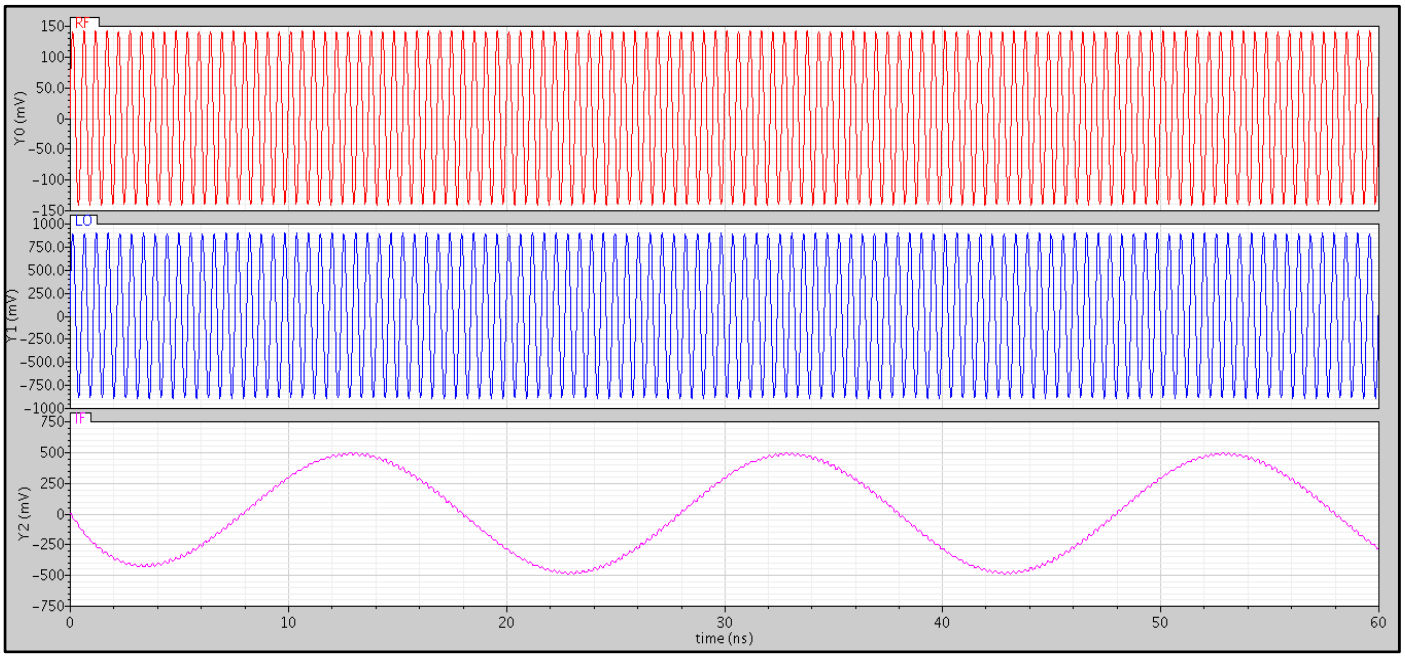


Figure 3.21: RF-LO-IF

Conversion Gain:

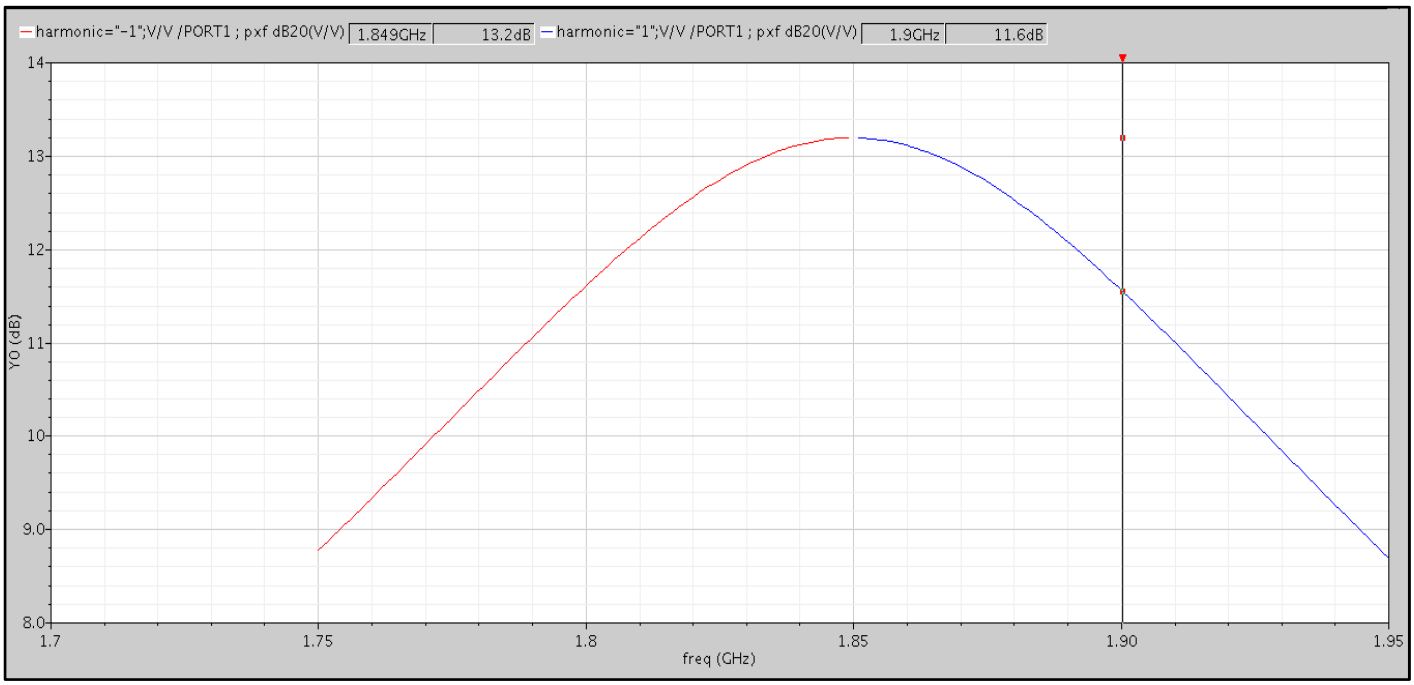


Figure 3.22: Conversion Gain

Noise Figure:

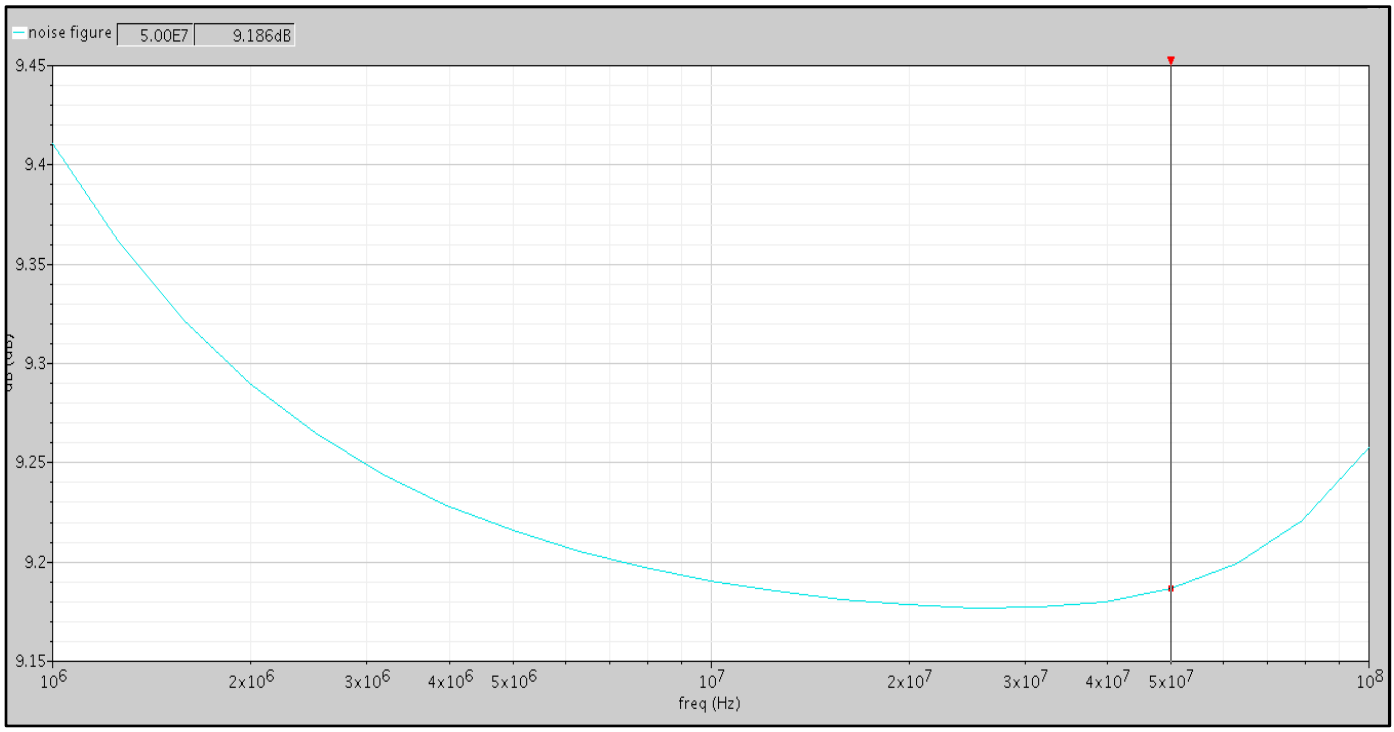


Figure 3.23: Noise Figure

IIP3:

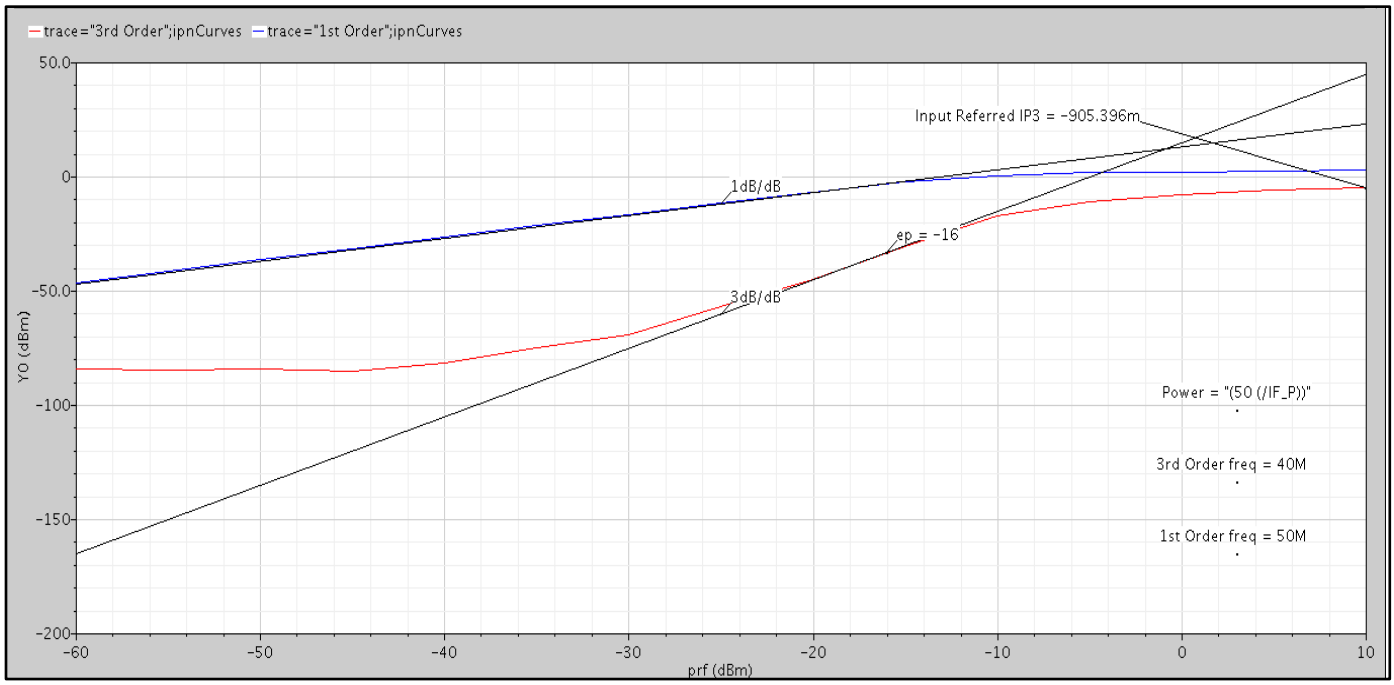


Figure 3.24: IIP3

3.6 Required Specifications:

The specifications were previously calculated for the design of the overall project and for each sub-system block. The following Table 3.5: Mixers Specifications lists the required specifications for the down converting mixer.

Parameter	Specification
Bandwidth	40 MHZ ~ 2 GHZ
Voltage Conversion Gain	18 dB ~ 22 dB
Input referred IP3	≥ 5 dBm
Noise Figure	≤ 10 dBm
Supply Voltage	1.2 V
Power Consumption	15mW
Load	200fF on each terminal
IF signal bandwidth	6MHz
LO max. amplitude	0.8vpp

Table 3.5: Mixers Specifications

3.7 Our Mixers Design:

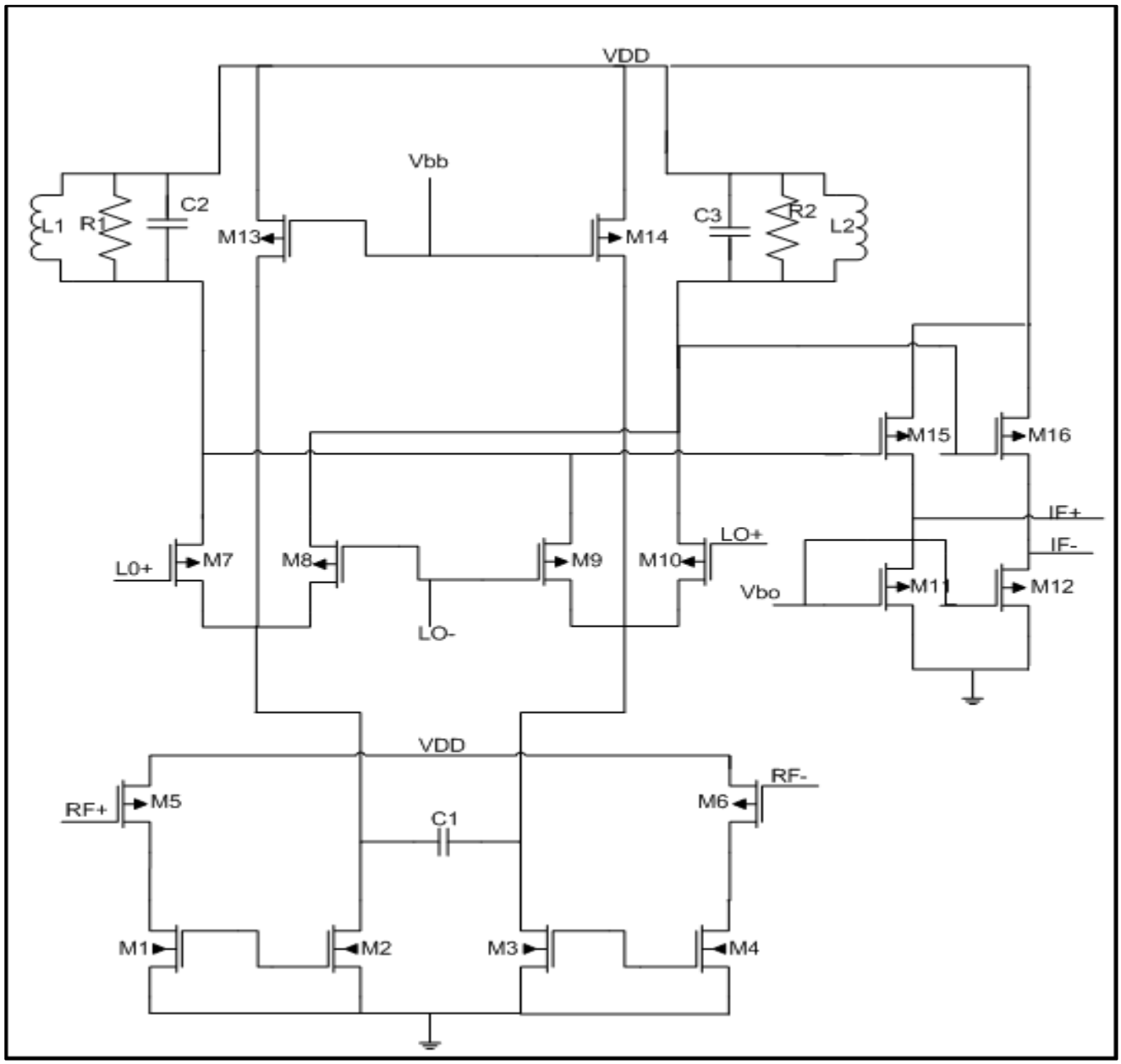


Figure 3.25: Schematic

The following (Table 3.6: Parameters Values shows the parameters and its values:

Parameter	Value	Parameter	Value
M5,M6	200u/180n	C1	2.5p F
M1, M4	50u/180n	C2, C3	200f F
M2,M3	88u/180n	L1, L2	2u H
M7,M8,M9,M10	80u/180n	R1, R2	600 ohms
M13,M14	40u/180n	Vb_LO	700m V
M15,M16	100u/180n	Vb_RF, Vb_buff	500m V
M11,M12	160u/180n	Vb_Leakage	50m V

Table 3.6: Parameters Values

3.7.1 Main Blocks:

3.7.1.1 *Input Stage:*

- The input stage shown in Figure 3.26: Input Stage is considered as the gain stage, In traditional Gilbert-cell the total conversion Gain can be approximated to gm(in)*Rout because the input stage is just formed of a single Nmos transistor but here the Conversion gain is calculated as follows:

$$\begin{aligned} Av &= gm2 * \left(\frac{gm0}{gm1}\right) * 0.5 * R \\ &= 30.4 * \frac{38.57}{29} * 0.5 * 600 \\ &= 21.676\ dB \end{aligned}$$

Equation 3.24

- In our design we tried to increase the gain by entering the signal to the gate of a pmos transistor followed by a current mirror so we can increase the gain by increasing the ratio between W0 & W1 while keeping L constant.

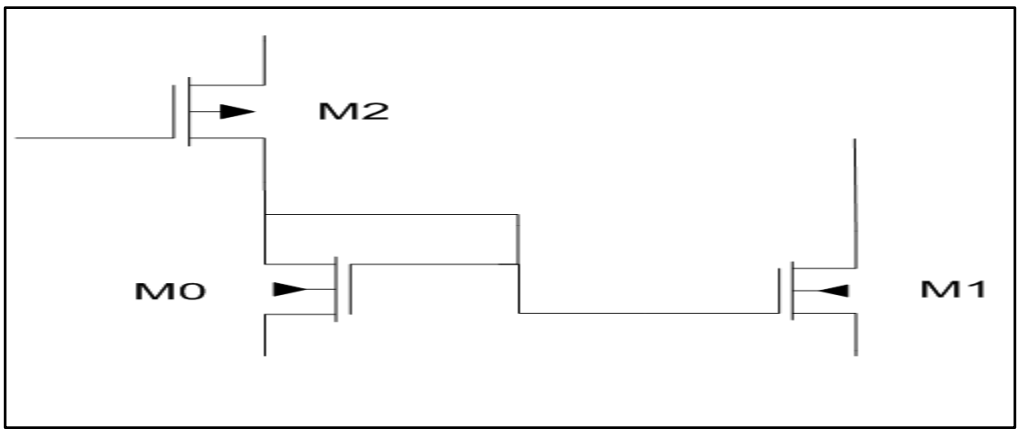


Figure 3.26: Input Stage

3.7.1.2 *Switch Stage:*

- When LO voltage level is too small the output voltage is dependent on the LO level, which means gain will be larger for larger LO because output voltage will become insensitive to the LO amplitude. Noise is also minimized for large LO. However, when the LO becomes too large, this leads to spikes in the signals, reducing switching speed and increase LO feed-through. The result of the spikes can also cause transistors to leave the saturation region.
- When one transistor pair is conducting, we want the other pair to be completely off. If two pairs are conducting current at the same time, it will generate noise. Therefore, the overdrive voltage (Vgs – Vt) should be as close to zero as possible. This is the midpoint between turning the transistor on and off.

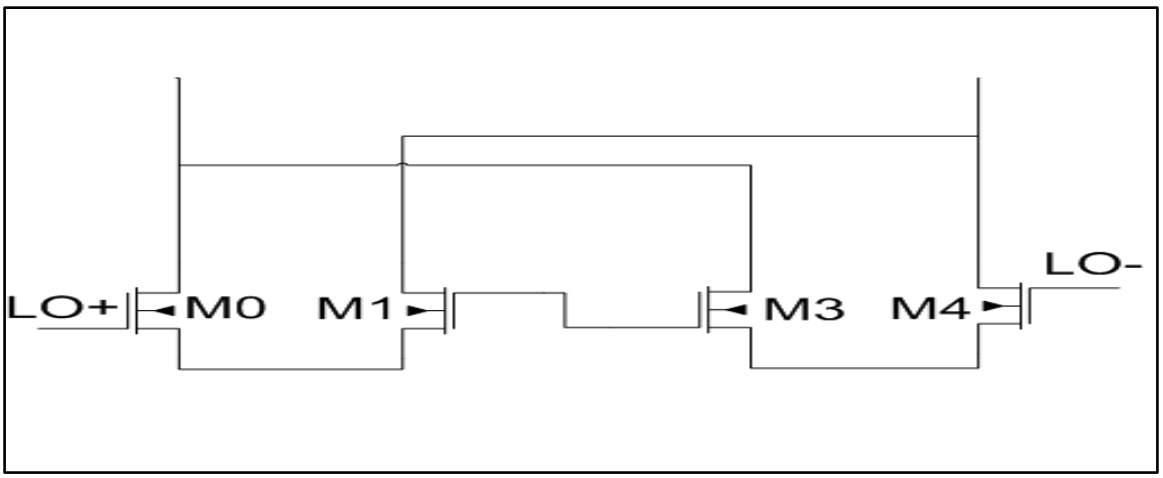


Figure 3.27: Switch Stage

3.7.1.3 *Current Bleeding:*

- Typical bleeding circuit with two PMOS transistors providing dc current into the driver stage as shown in (Figure 3.28: Current Bleeding

- The PMOS pair provides high output impedance that is in parallel with the low input impedance of the switching pair. Therefore, the weak IF signal is forced to go into the switching pairs. The gain of the mixer is maximized with fast switching similar to a square wave.

- At the same time, the bias current through the driver stage can be increased without increasing the current through the switching transistors.

- Also, with bleeding, either the switching transistors can be operated at a lower gate-source voltage or smaller size transistors can be used.

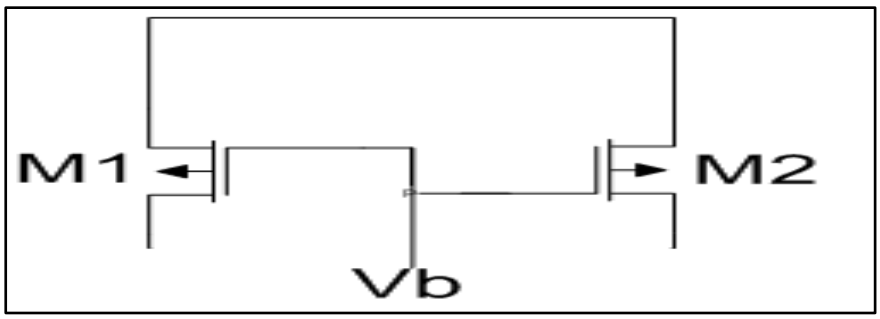


Figure 3.28: Current Bleeding

3.7.1.4 *Output Stage:*

- The down converting mixer has a broadband input and a fixed IF output. It only needs to provide gain over a narrow frequency range centered on the IF frequency. If headroom is a problem, a tuned load can be used to provide larger output swings. At DC, the inductor is shorted and hence there is no voltage drop across the tuned load so there is more room to work with. At the resonating frequency of the tank, the gain becomes Gm*R since the inductor and capacitor are an open circuit at this frequency.

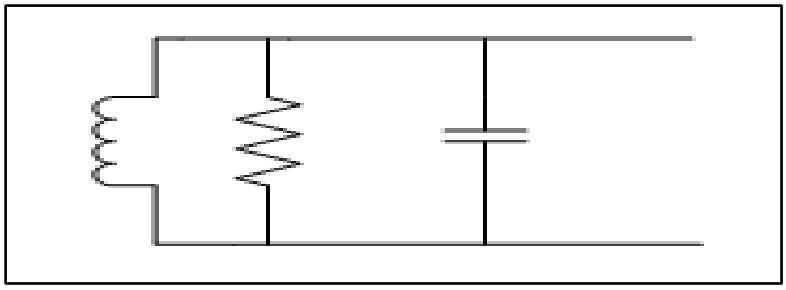


Figure 3.29: Output Stage

➔ It was found that the system has a main pole at

$$\frac{1}{2\pi * R_{out} * C_{eff}} \qquad \textit{Equation 3.25}$$

- Where $R_{out} \approx 600\, ohm(\, load)$ & $C_{eff} \approx$ 200f F(load) + 394f F (parasitic capacitance added by the transistors of the Switch stage).
- Parasitic capacitances of transistors ≈ 2*C_{M7}

  $C_{ss7} = 70.0752f\ F,\quad C_{gs7} = 81.4199f\ F,\quad C_{ds7} = 26.2452f\ F \quad \& \quad C_{bs7} = 20.2201f\ F$

- Following this equation the pole will be at frequency 446.562 MHz, so a capacitor of 2.5 pF was added in series with the sources of transistors of the switch stage to the ground to decrease their parasitic capacitance and make the pole out of the required band.

3.7.1.5 *Buffer stage:*

In order to drive different load resistances without degrading the performance of the mixer, an output buffer was implemented. The source follower as shown in (Figure 3.30: Buffer Stage is a common configuration and was implemented in the mixer design. The source follower will allow the gain to remain consistent with the expected mixer gain while changing the mixer's output resistance.

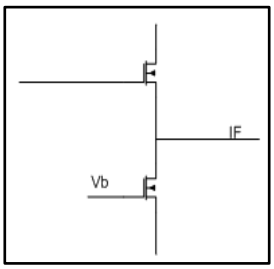


Figure 3.30: Buffer Stage

3.7.2 Simulation Results:

3.7.2.1 *RF-LO-IF:*

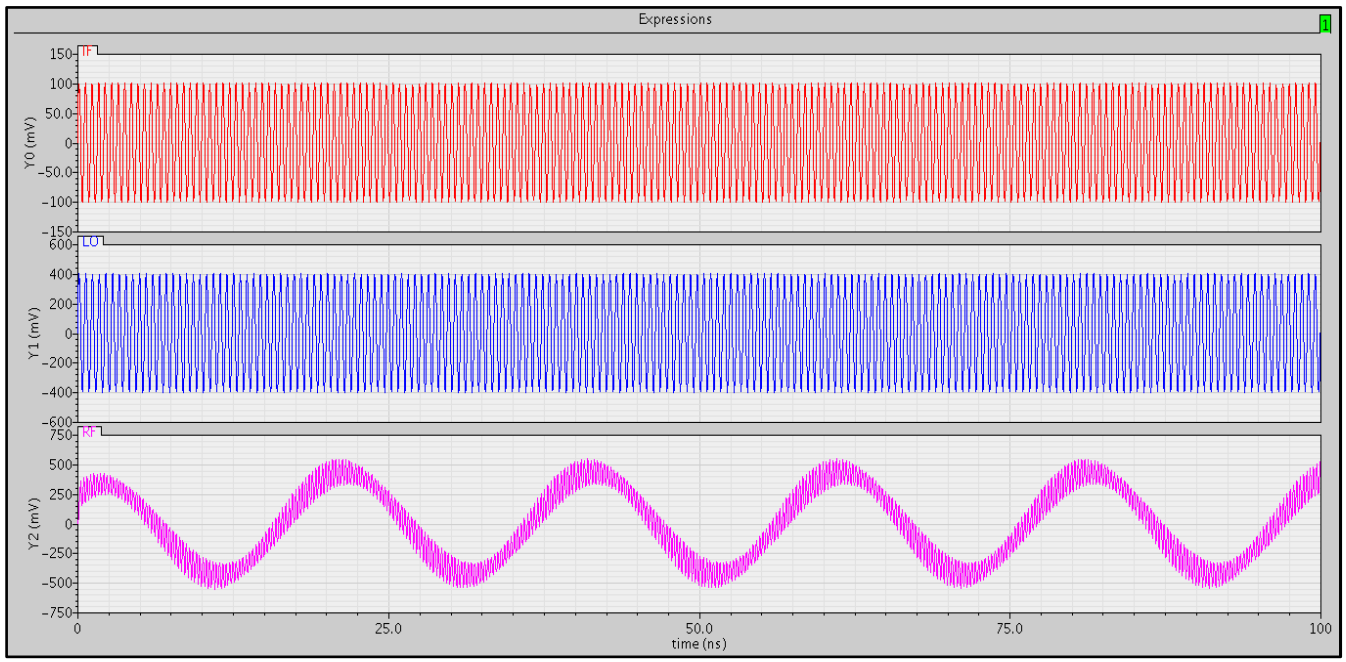


Figure 3.31: RF-LO-IF

3.7.2.2 *Conversion Gain:*

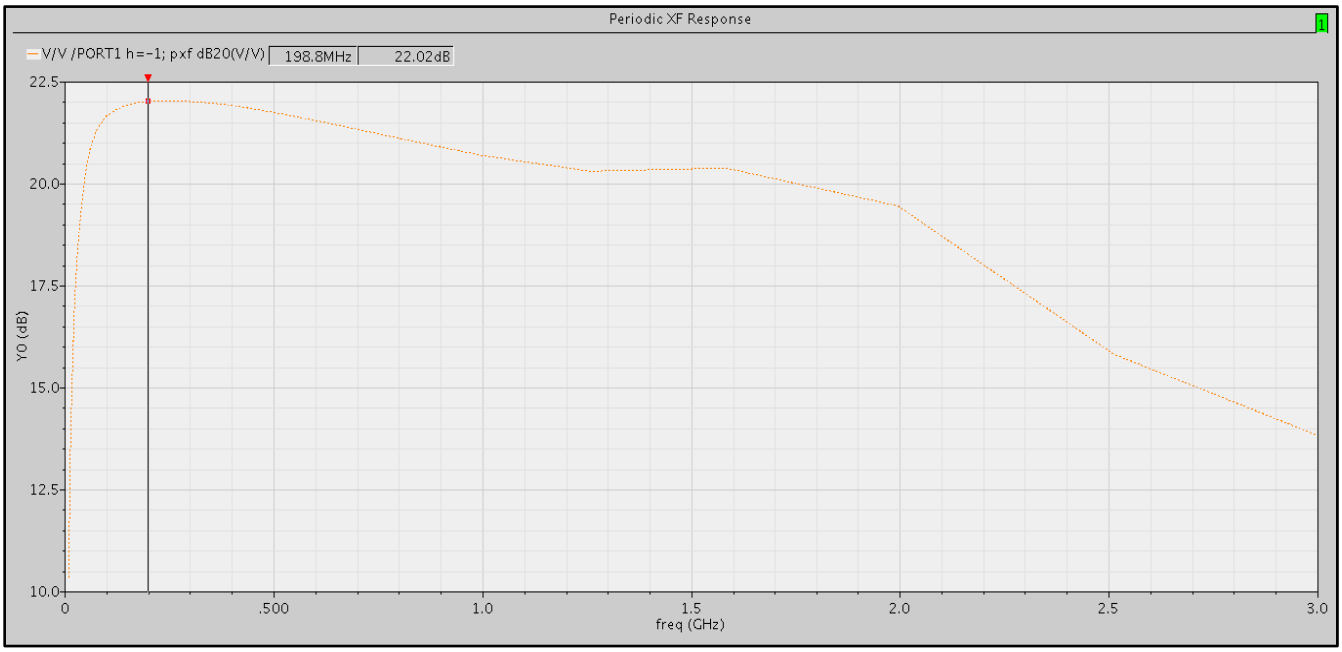


Figure 3.32: Conversion Gain

3.7.2.3 *Noise Figure:*

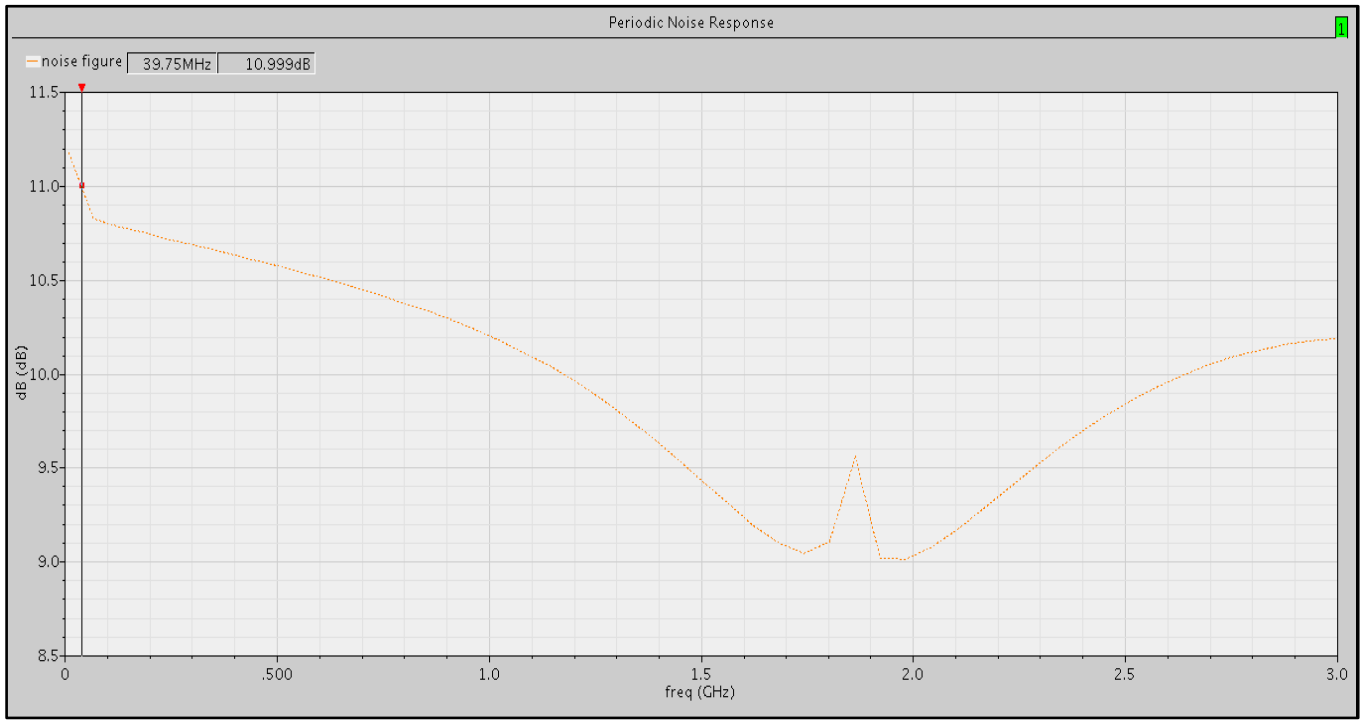


Figure 3.33: Noise Figure

3.7.2.4 *IIP3:*

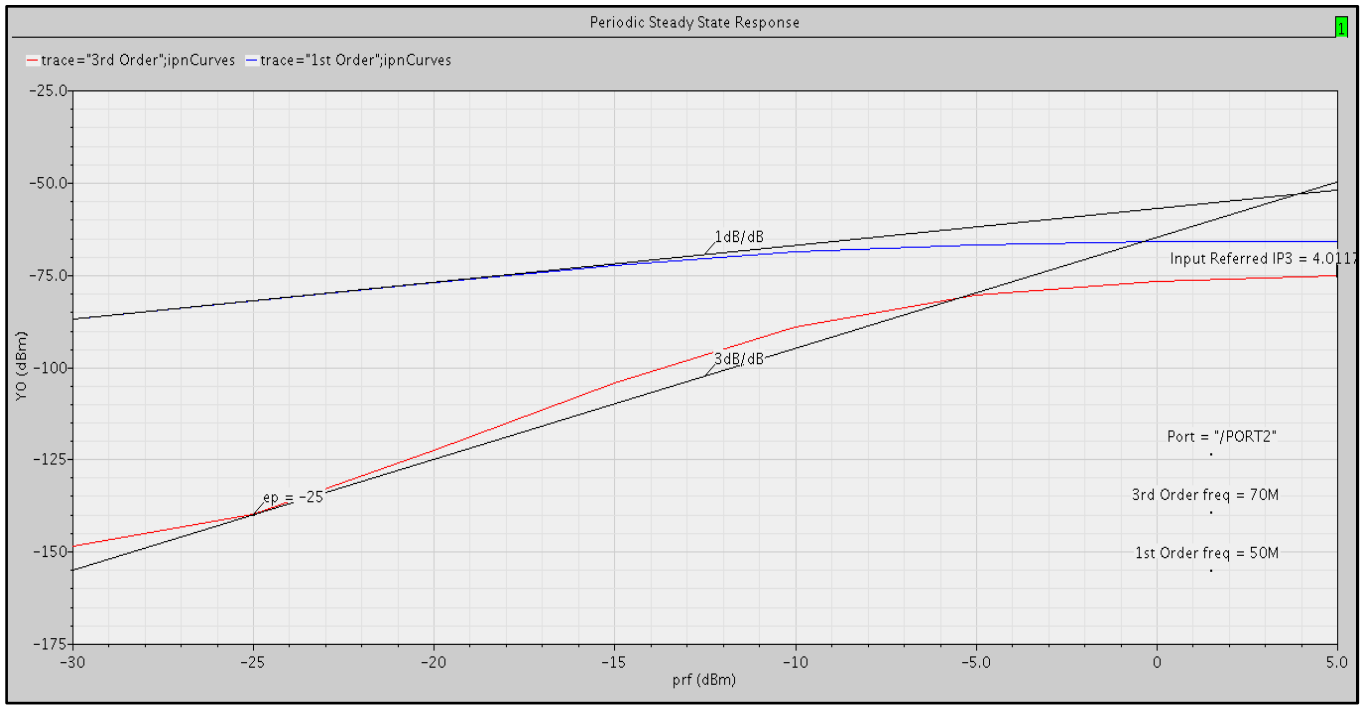


Figure 3.34: IIP3

3.7.2.5 *Achieved Specifications:*

Parameter	Required Specification	Achieved Specifications
Bandwidth	40 MHZ ~ 2 GHZ	40MHz-2Ghz
Voltage Conversion Gain	18 dB ~ 22 dB	18-22.02 dB
Input referred IP3	≥ 5 dBm	4 dBm
Noise Figure	≤ 10 dBm	9-10.9 dB
Supply Voltage	1.2 V	1.2V
Load	200fF on each terminal	200fF on each terminal

Table 3.7: Required Vs Achieved Specifications

3.7.3 After Inserting the Non-Ideal Components:

We have replaced Ideal Components in the circuit with non-Ideal Components to simulate the behavior of the circuit with real components used in industry and to be ready to make a layout for the circuit.

Ideal Components	Non-Ideal Components
Output Resistance	rnhpoly resistor
Output Capacitor	pmos1vcap
Pole Capacitor	MIMcap

Table 3.8: Ideal Vs Non Ideal Components

rnhpoly resistor:

The resistors are made from doped polysilicon (all poly) or different diffusions in the process. The three diffusions that are used for resistors are N+, P+, and N-Well. The N+ and P+ diffusions are used for the drain/source of NChannel/PChannel transistors respectively.

The N-well is the body of a PMOS transistor. The N+ and P+ are shallow lower sheet resistance resistors. They would be best for lower value of resistors. The N-Well is a deeper junction and would be better for middle values of resistors.

MI MCap:

MIM capacitors basically a parasitic capacitor between the metal layers (MIM -->Metal insulator Metal). CTM mask layer is used for insulation. It gives an accurate capacitance value but it takes lot of area.

Pmos1vcap:

Mos capacitors which is formed between POLY layer and Nwell layer(Poly Nwell Cap) gives more capacitance in less area but the Capacitance is not such accurate as MIMcap.

3.7.3.1 *Simulation Results:*

1.1.1.1.1 RF-LO-IF:

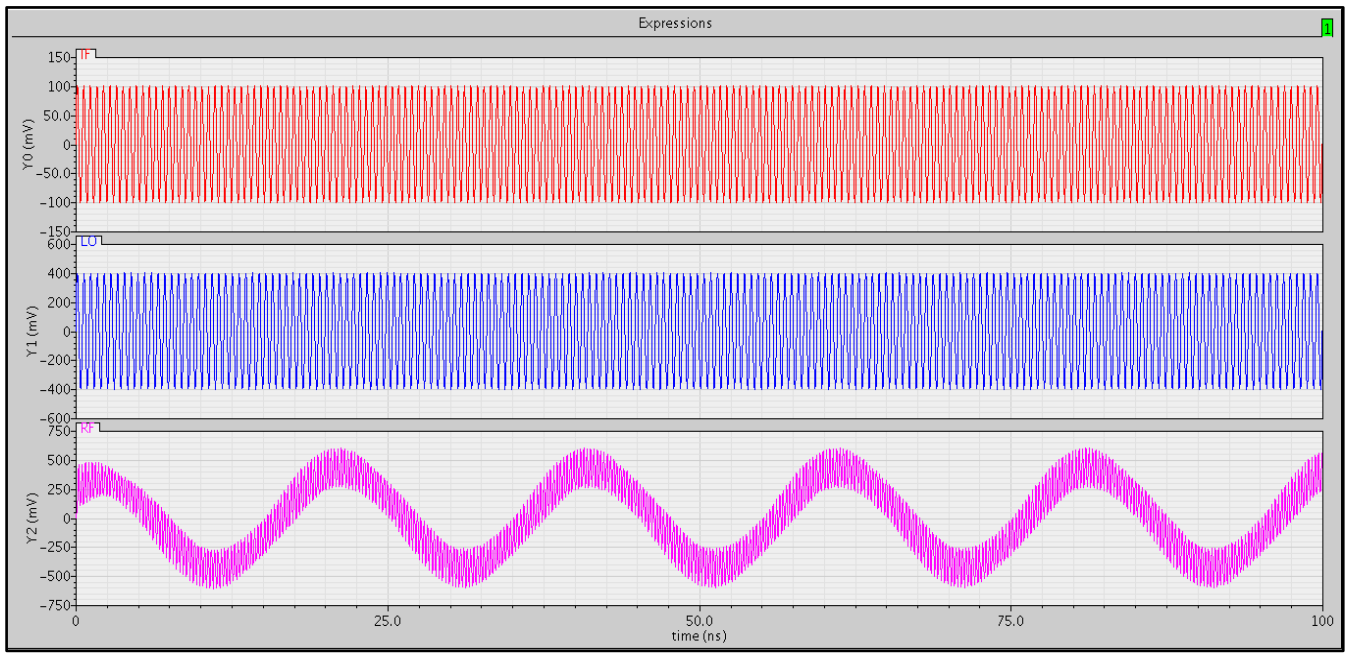


Figure 3.35: RF-LO-IF

3.7.3.1.1 Conversion Gain:

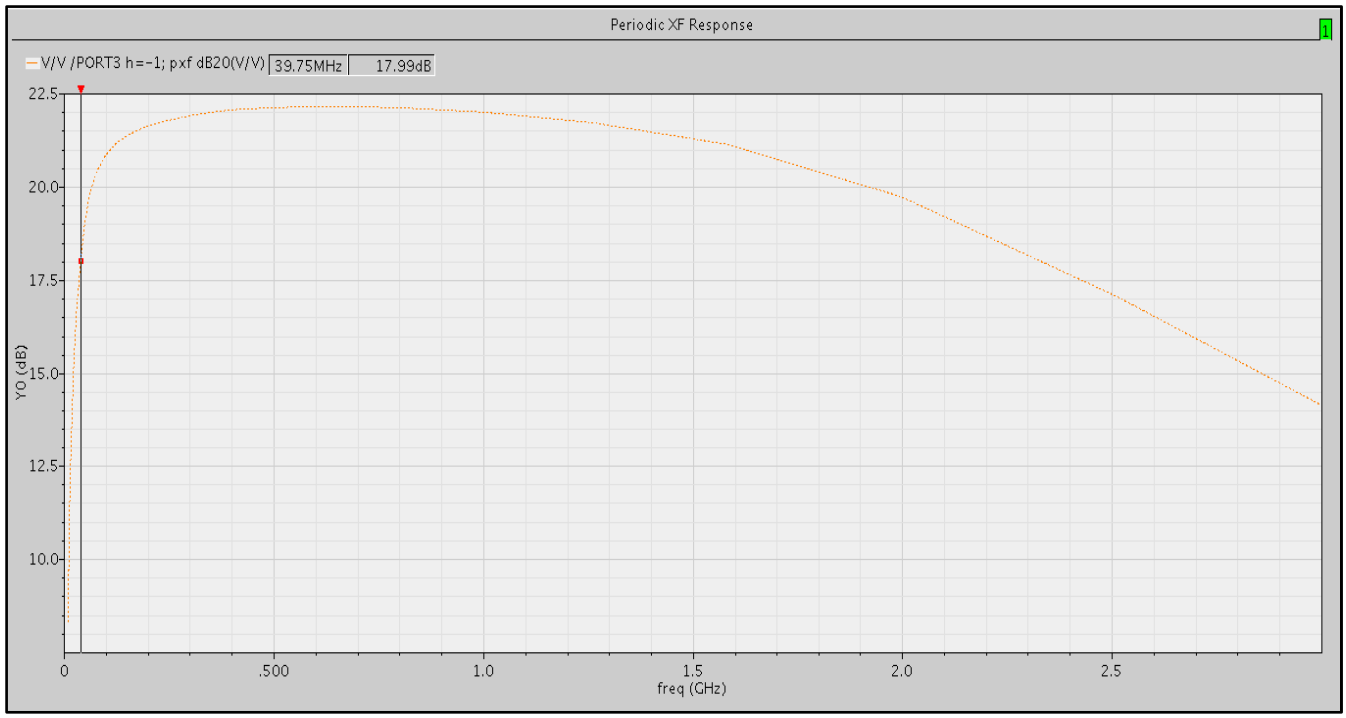


Figure 3.36: Conversion Gain

3.7.3.1.2 Noise Figure:

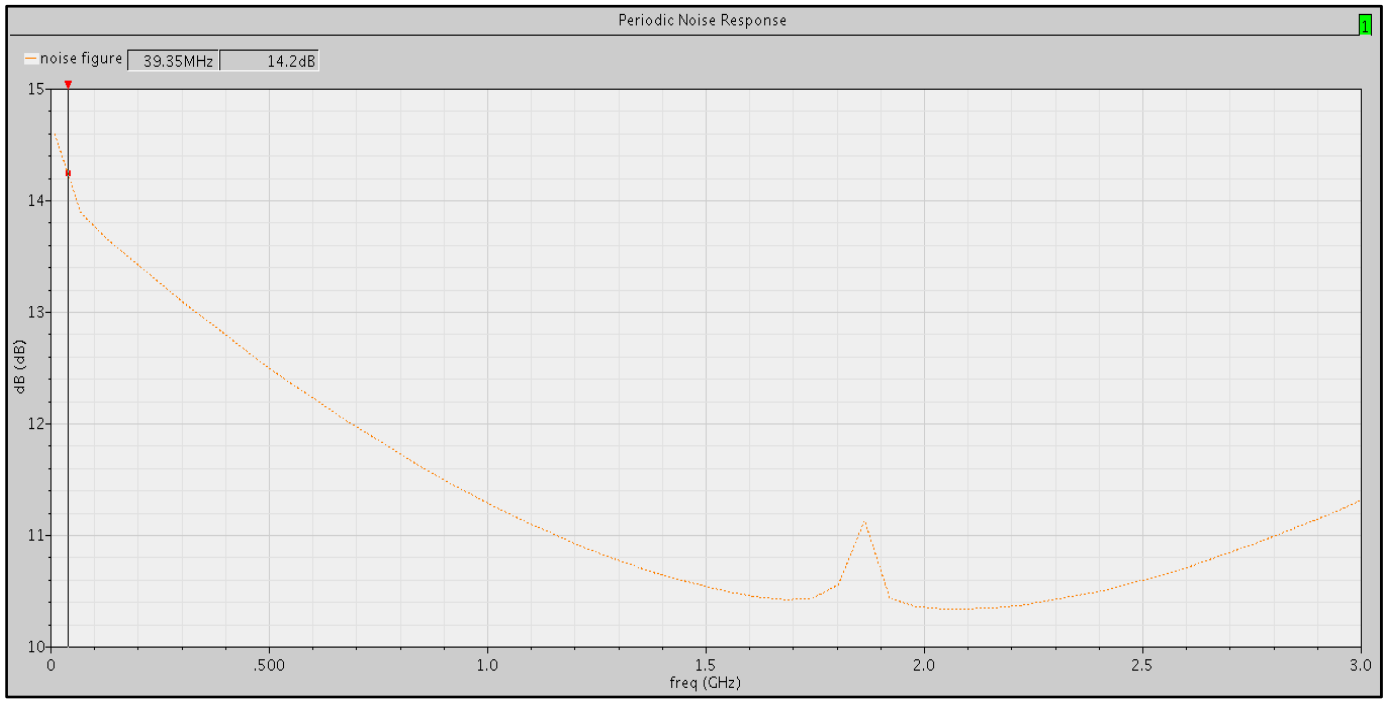


Figure 3.37: Noise Figure

3.7.3.1.3 IIP3:

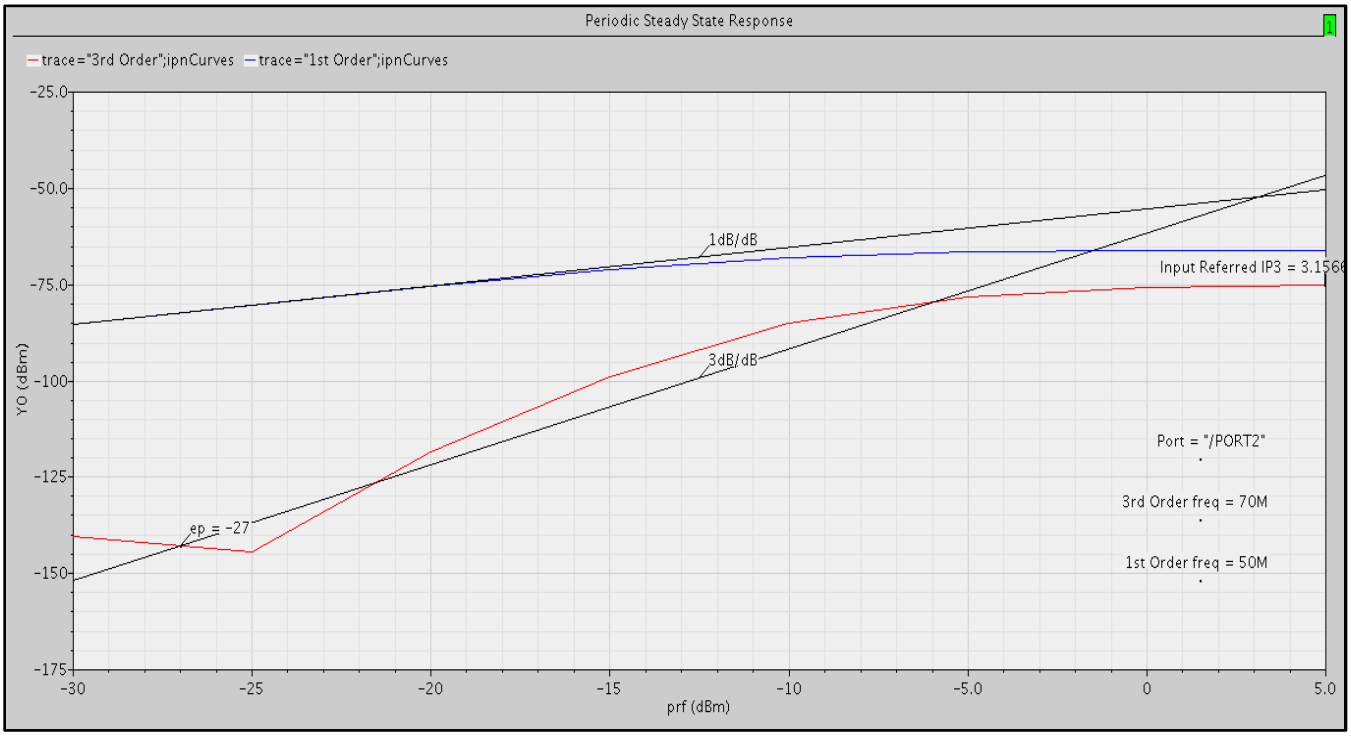


Figure 3.38: IIP3

3.7.3.1.4 Achieved Specifications:

Parameter	Required Specification	Achieved Specifications
Bandwidth	40 MHZ ~ 2 GHZ	40MHz-2Ghz
Voltage Conversion Gain	18 dB ~ 22 dB	18-22.05 dB
Input referred IP3	≥ 5 dBm	3.15 dBm
Noise Figure	≤ 10 dBm	10.2-14.2 dB
Supply Voltage	1.2 V	1.2V
Load	200fF on each terminal	200fF on each terminal

Table 3.9: Required Vs Achieved Specifications

3.8 Enhancements

As shown in previous simulation results, Noise Figure and IP3 results needs some enhancements to meet the requirements.

Some suggestions of enhancement topologies that can be tried:

3.8.1 Active Mixer with current source helper

- The principal difficulty in the design of active mixers presents from the conflicting requirements between the input transistor current which must be high enough to meet the noise and linearity specifications and the load resistor current which must be low enough to allow large resistance and hence a high gain, we therefore summarize that adding current sources in parallel with the load resistors can solve this conflict by affording larger resistors values as shown in Figure **3.39 [1]: Active Mixer with current source helper**

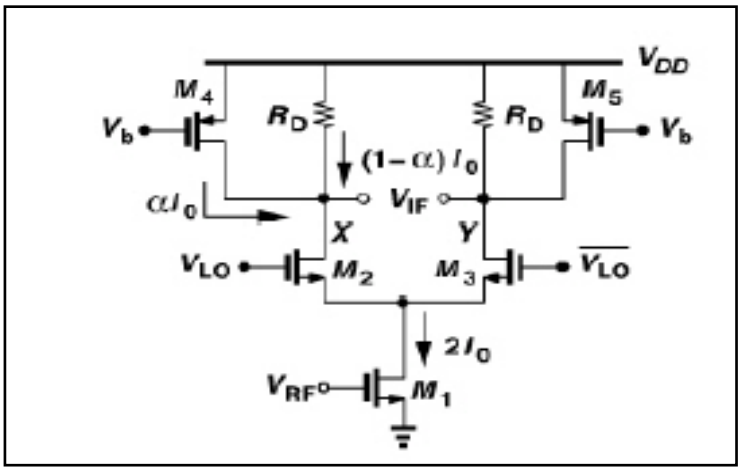


Figure 3.39 [1]: Active Mixer with current source helper

3.8.2 Active Mixer with enhanced transconductance

- Same concept of the previous topology but this time we will insert the current source helper in the RF path rather than the IF path as shown in (Figure 3.40 [1]: Active Mixer with enhanced transconductance, the idea is to provide most of the bias current of M1 and M4 which will reduce the current flowing the load resistors and the switch transistors.

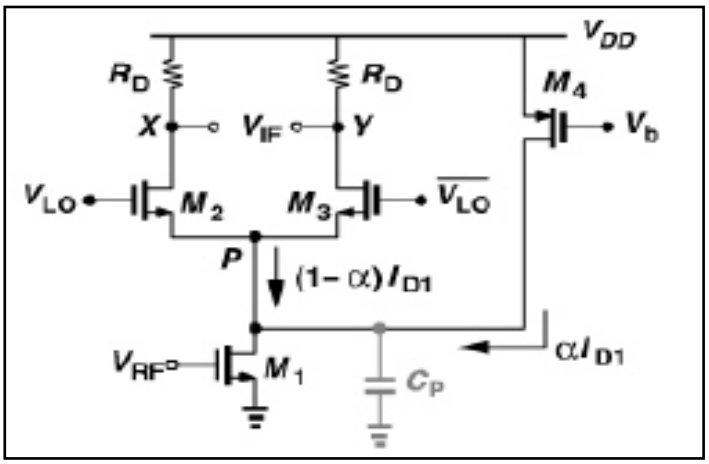


Figure 3.40 [1]: Active Mixer with enhanced transconductance

3.8.3 Active Mixer with low flicker noise

- The down-converted flicker noise of the switching devices is proportional to their bias current and the parasitic capacitance at their common source node.
- Reducing the current through the switching devices at the crossing points of LO and $\overline{LO}$ can alternatively be realized by turning off the transconductance momentarily, one way of making that is illustrated in the following (Figure 3.41 [1]: Active Mixer with low flicker noise

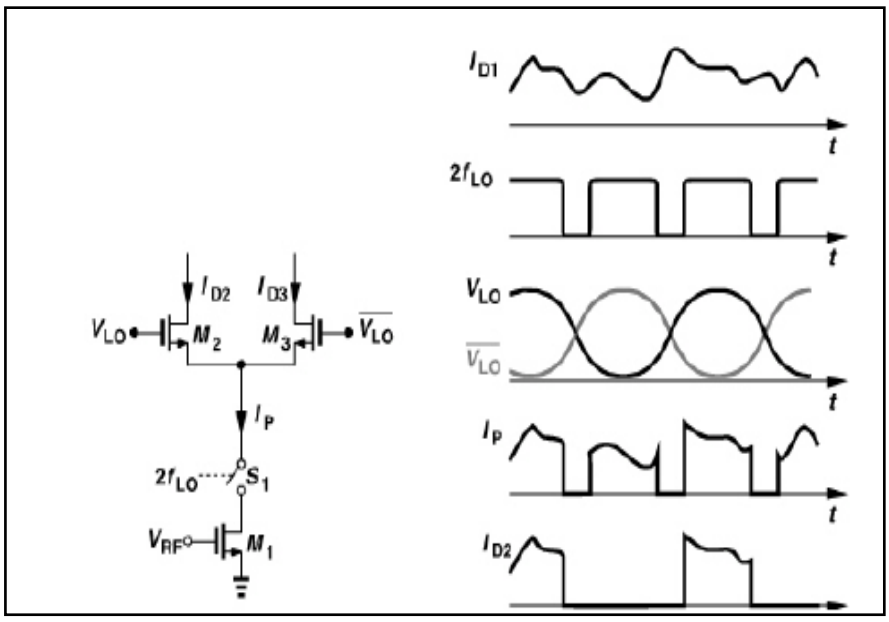


Figure 3.41 [1]: Active Mixer with low flicker noise

- Where S1 is driven by a waveform having a frequency 2flo but a duty cycle of 80%, S1 briefly turns the transconductance off twice per LO period, so if the crossing points of LO and $\overline{LO}$ are chosen to fall at the times when Ip is zero then the flicker noise of M2 and M3 is heavily attenuated and also will make M2 and M3 inject no thermal noise to the output near the equilibrium
- The main problem in this topology is that the conversion gain will suffer because the transconductane remains off for a greater portion of the period.

4 Layout

After finishing the schematic, we started transforming our schematic design to a layout a design, using Calibre layout tool that we installed on Cadence.

4.1 Steps of layout design :

1. Remove all ideal components and replace them with non-ideal components.
2. Re-simulate the circuit to make sure that the non-ideality of the components didn't affect the required specifications .
3. If the non-ideality affected the circuit , then we must re-configure the values of the non-ideal components to compensate the errors .
4. After reaching the same old results , then we have to remove all input and output ports and replace them with input and output pins.
5. Also removing all supplies and replace them with input pins .
6. Removing the components who don't have a layout package (i.e Ideal current sources , balun,..etc).
7. Then initiating caliber and generate the instances from the schematic .
8. Placing the instances on the reference board .
9. Perform routing .
10. Check DRC (Design rule check , in which Calibre check if any design rule was broken by our placing or routing , to make sure of the correctness of the circuit)
11. Check LVS (Layout versus schematic , in which Calibre checks if the routing between the instances is the same as in the schematic , to make sure that all connections are valid connections) .
12. And finally Perform PEX (in which we simulate the layout and compare to the original simulation of the schematic , to see the effect of the routing parasitics and non-ideality of the components).

4.2 Some rules to take into considerations while placing and routing:

1. The layout should be compact, we must place the instances as near to each other as possible.
2. We have to adjust the thickness of the routing wire to ensure a 1 um/ 1 mA , to make sure that this route will be able to stand the high current(but this differs according to different technologies).
3. We have to try to avoid 90 degrees turns of the wires , because it causes reflections , which decreases the signal power
4. Try to minimize the use of poly , and even if it's used , we have to make the wire as short as possible
5. If the circuit is fully differential , the +ve and –ve differential lines should be somehow near each other so that they are affected with the same conditions (length of wire , temperature , noise , ….etc)
6. Also the differential pairs wires should have almost the same length , to have the same degradation of power(FIGURE XXX)
7. Wire should not be too long , it should be as short as possible , to decrease the effect of the power loss of the signal when it travels for long distances
8. Distance between 2 inductors must be at least 2R (where R is the radius of inductor)
9. The width of the wires will affect its capacitance , so we to take that into our considerations.

4.3 Non-ideal components used:

1. Spiral Std M6 Inductor

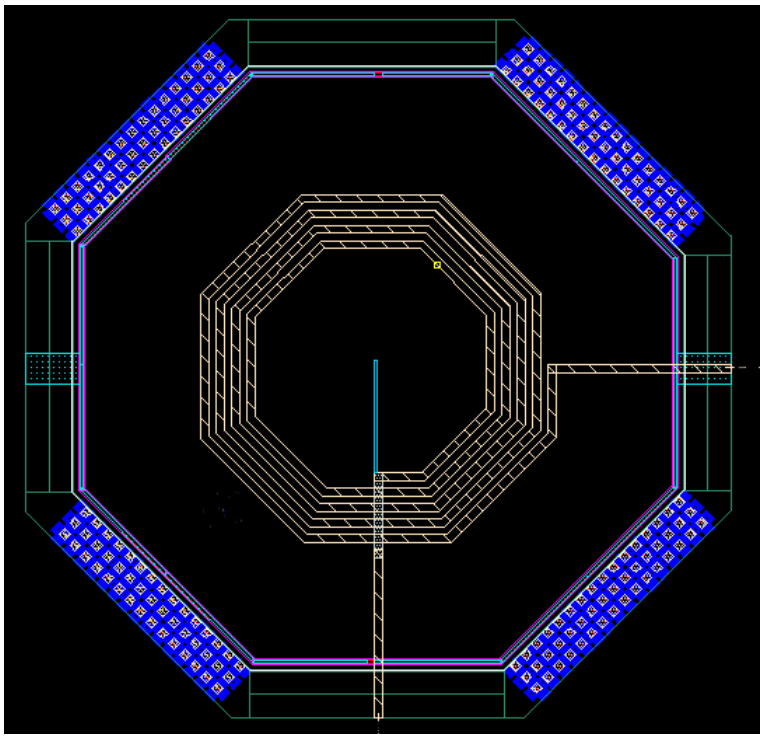


Figure 4.1 Inductor used in LNA

2. Pmos1v capacitor

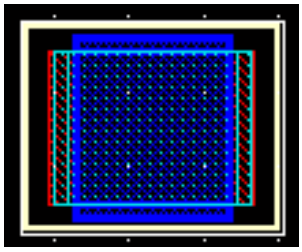


Figure 4.2 : Capacitor used in LNA

3. Rm1 resistor (Metal 1 because it has a small value)

Figure 4.3 : 140 ohm resistor used

4. Rnhpoly resistor (used this one because we needed a higher value of resistance)

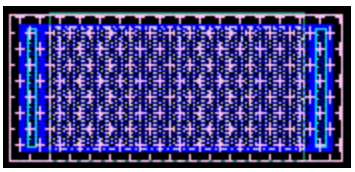


Figure 4.4 : resistor used in mixer

5. Mimcap (used this one because we needed a higher value of capacitance)

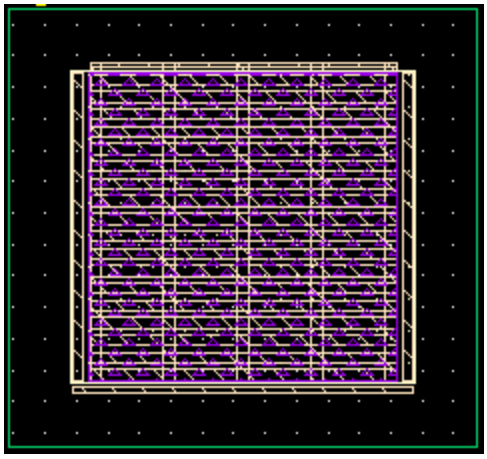


Figure 4.5 : capacitor used in Mixer

6. Rfnmos1v

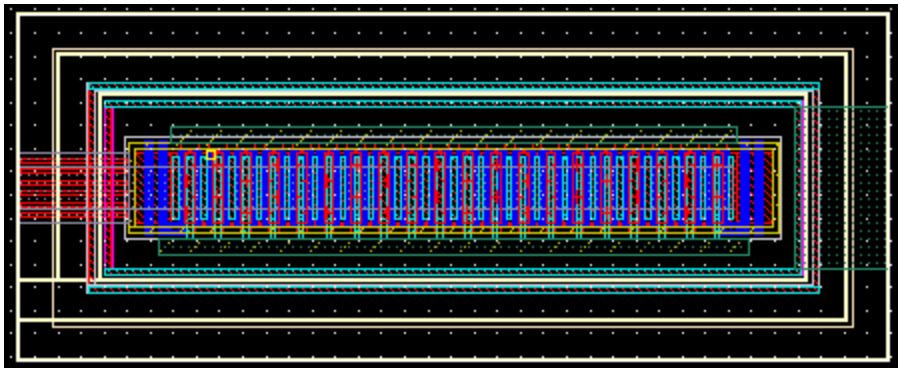


Figure 4.6 : Rfnmos1v used in LNA and Mixers

7. Rfpmos1v

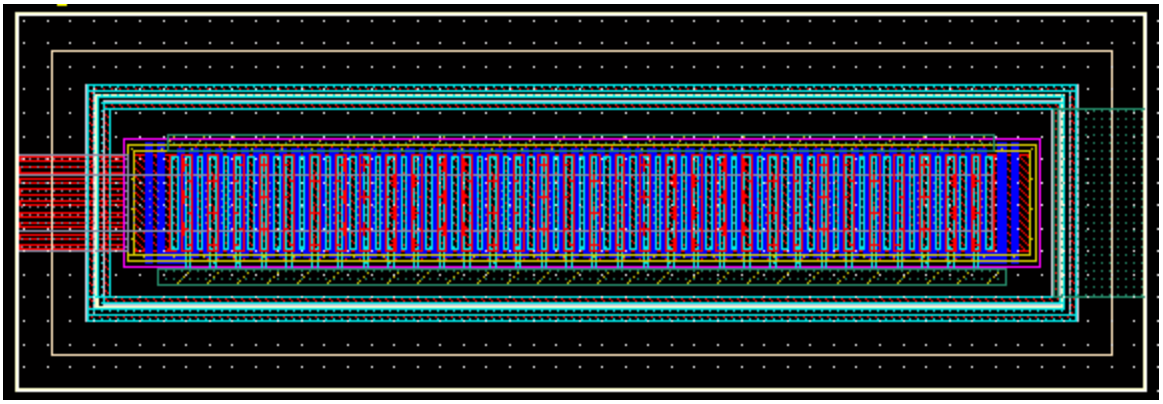


Figure 4.7 : rfpmos1v used in LNA and Mixers

4.4 Differences between normal NMOS1V and RFNMOS1V:

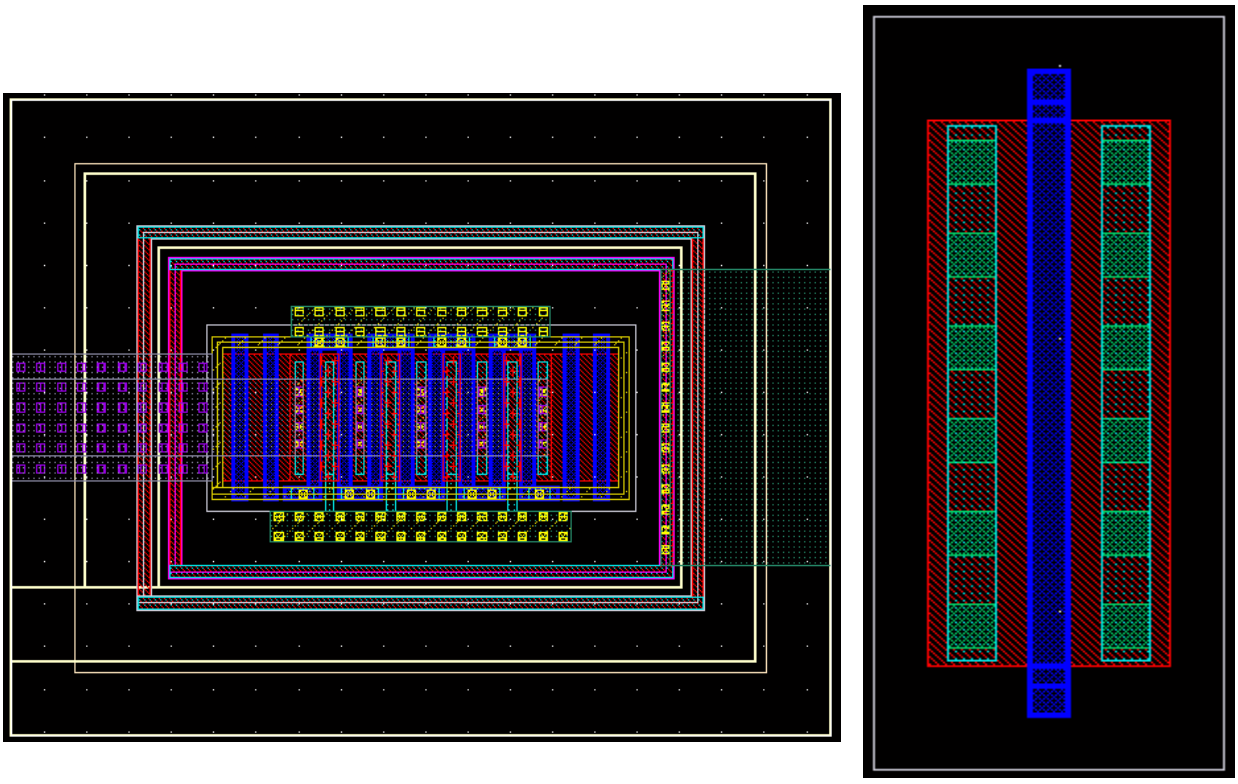


Figure 4.8 : rfnmos1v (on the left) and nmos1v (on the right)

Main differences between both of them are that the rfnmos1v has already all its peripherals connected and extra poly are added to simulate the effect of parasitics, which is the main issue of RF layout design.

4.5 Steps taken in layout:

So at the beginning, the copy Cadence (that we already have) didn't have Calibre installed on it , so we had to search for a long time for someone in the faculty who has Calibre.

Eventually, we found T.A Mahmoud , and he helped us installing Calibre and downloading its libraries.

All our design (including LNA and Mixer) is based on RFNMOS1V and RFPMOS1V , because it helps simulating the practical parasitics that a transistor will have in the high frequency range.

But when we started generating layouts out of schematics , we had a huge error in all RFNMOS and RFPMOS because of a missing library called GR (Guard Ring) which helps in decreasing the latch ups of the transistor .

So we ended up making an empty library and renaming it GR and the problem was solved, and we decided to go on with the layout design and get back to the actual GR design when we finish our design.

But unfortunately this trick only worked on only laptop , we tried the same concept on other laptops but we failed , so we ended up working on only on laptop , so basically we started working in series .

So first , we started designing the layout of the LNA , using the non-ideal components , and trying to achieve full symmetry between both half circuit to ensure that each difference signal endorse the same effect (noise , … etc) so as we see (Figure 4.9), this is the design of the LNA layout .

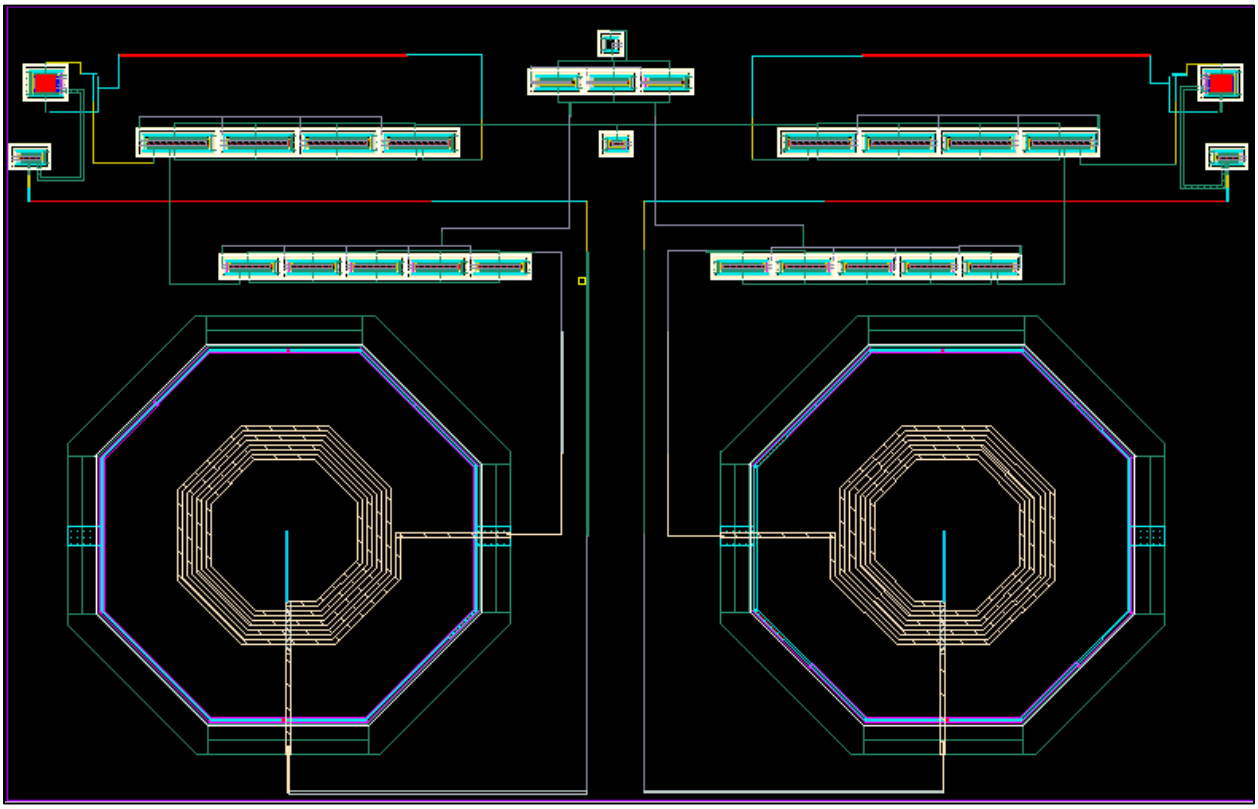


Figure 4.9 : LNA Layout

As we can see it's almost fully symmetric, and the outputs are taken straight from the 2 wire at the top the layout.

It consists of 2 inductors, 27 Transistors, 4 resistors and 2 capacitors .

Then before running DRC test on the LNA we decided to design the MIXER design first , and in the same manner we wanted everything to be fully symmetric , and we actually got a better compact design than the LNA as we see in (Figure 4.10)

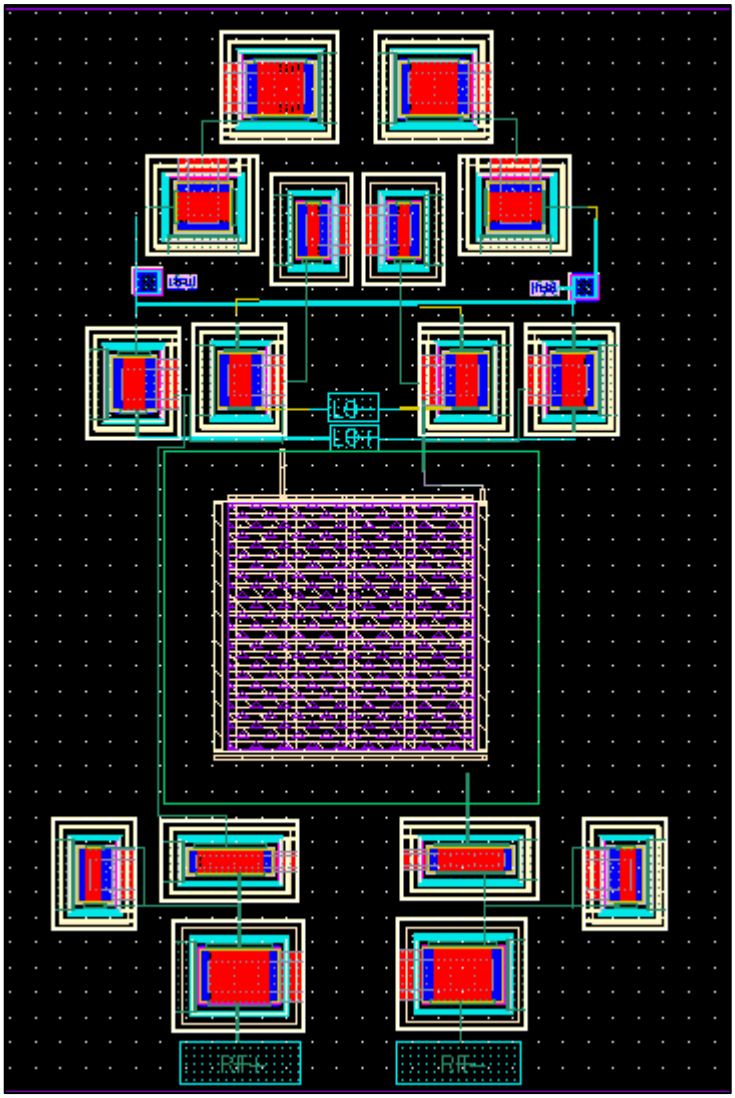


Figure 4.10 : Mixer's Layout

Obviously it’s more compact and almost fully symmetric. It consists of 16 Transistors, 2 resistors and 3 capacitors.

So after we finished both designs, we started running the DRC on the MIXER Layout first, and we got some errors and most of them were:

1. Density error: where the density of some materials has to have a minimum value , and if not then we will have to add some extra material of the layer to achieve the required density.
2. Spacing error: because there is a minimum value of the spacing between different components and also between wires (same type or different type) so that the signal on one wire doesn't affect the signal on the other wire. So all we have to do increase the spacing until it reaches the minimum spacing.
3. Width error: because each wire of a specific material has to have a minimum width. So we will have to increase the width.
4. Area error: where the area of some layer or materials is less than the minimum area required, so we should increase that material area.
5. Some errors called CSR and CBM that doctor Faisal told us to do take them into considerations, and that they are caused by the presence of capacitors in the layout.

So we solved all the errors that we could solve, we disregarded CSR, CMB and Density errors, and we considered the layout DRC free as shown in (Figure 4.11)excluding those errors.

So by now we have a DRC free layout of Mixer, but instead of doing the same thing to the LNA's layout , we decided to check and run the LVS on the Mixer , to see if everything is as we was expecting or not , and we decided to come back to the LNA after we finish the LVS of the Mixer.

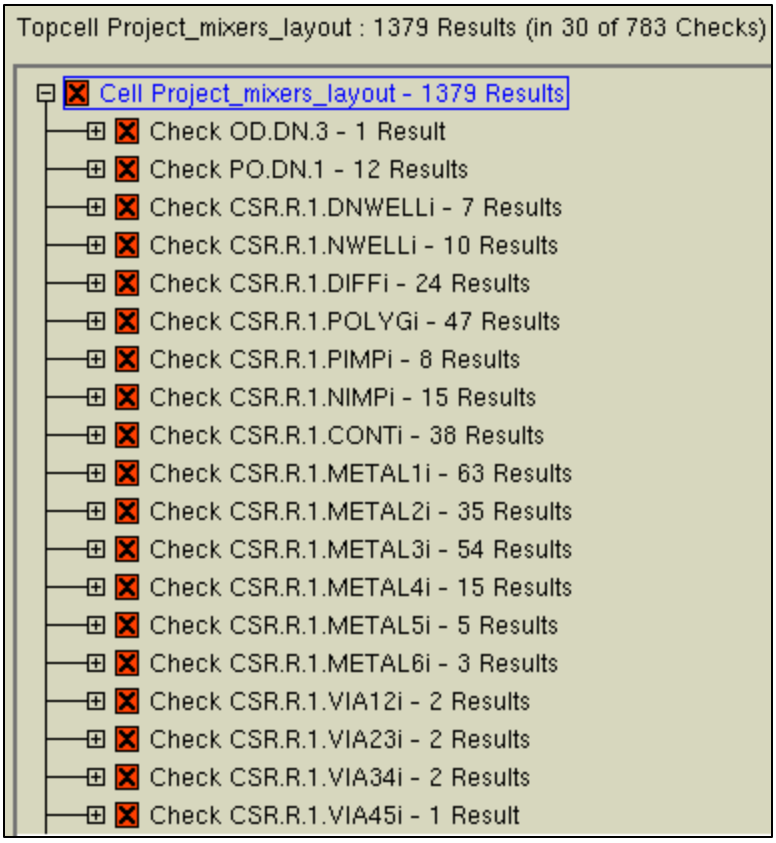


Figure 4.11 : After finishing the DRC of Mixer

Now, after initiating LVS and running it , we had a huge problem , Source file of layout cannot be read by Calibre , and it's refusing to deal with RFNMOS and RFPMOS as shown (Figure 4.12)As far as we understand , this error means that the extractor doesn't understand what RFNMOS

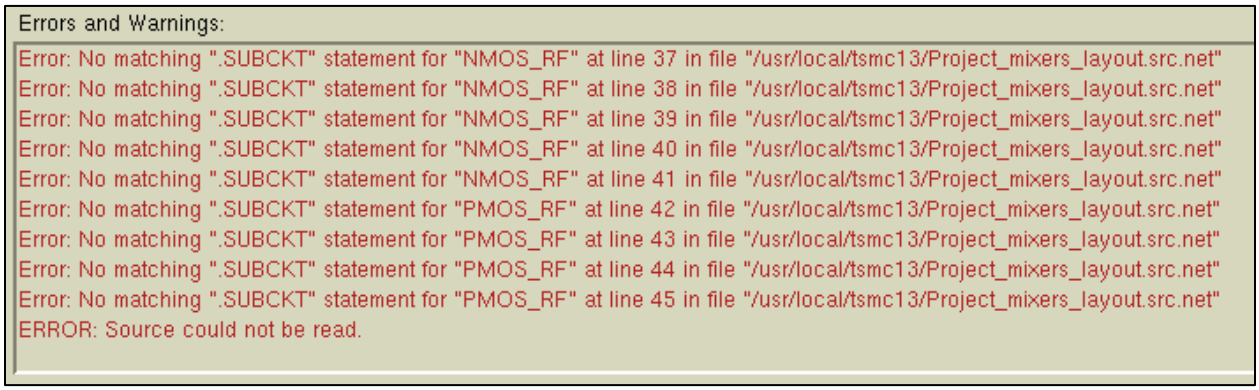


Figure 4.12 : Errors in LVS

is , because we checked the source netlist (/usr/local/tsmc13/Project_mixer_layout.src.net) shown in (Figure 4.13), and obviously it's rejecting the RFNMOS and RFPMOS .

```
XM0 net20 net9 GND GND rnos_rf lr=180.0n wr=4u nr=22 m=1
XM1 net15 net15 GND GND rnos_rf lr=180.0n wr=10u nr=5 m=1
XM2 net9 net9 GND GND rnos_rf lr=180.0n wr=10u nr=5 m=1
XM3 net65 net15 GND GND rnos_rf lr=180.0n wr=4u nr=22 m=1
XM17 net76 LO+ net20 GND rnos_rf lr=180.0n wr=10u nr=8 m=1
XM7 net21 LO- net20 GND rnos_rf lr=180.0n wr=10u nr=8 m=1
XM8 net76 LO- net65 GND rnos_rf lr=180.0n wr=10u nr=8 m=1
XM9 net21 LO+ net65 GND rnos_rf lr=180.0n wr=10u nr=8 m=1
XM10 Vdd net76 IF+ GND rnos_rf lr=180.0n wr=10u nr=10 m=1
XM12 Vdd net21 IF- GND rnos_rf lr=180.0n wr=10u nr=10 m=1
XM13 IF- Vbo GND GND rnos_rf lr=180.0n wr=10u nr=16 m=1
XM11 IF+ Vbo GND GND rnos_rf lr=180.0n wr=10u nr=16 m=1
XM4 net9 RF+ Vdd Vdd pmos_rf lr=180.0n wr=10u nr=20 m=1
XM5 net15 RF- Vdd Vdd pmos_rf lr=180.0n wr=10u nr=20 m=1
```

Figure 4.13 : the source netlist (/usr/local/tsmc13/Project_mixer_layout.src.net)

To understand why it's not accepting it , we made a simple nmos circuit and checked it source netlist , and the difference was that nmos transistors are defined as N and P as shown in(Figure 4.14)and we ran the LVS and it worked fine .

```
MM0 bb bb bb bb N M=1 L=130n W=2u
```

Figure 4.14 : source netlist of NMOS

We tried different solutions that we found on edaboard forum to solve this problem but we failed, and it wasted a lot of our time, so we contacted Doctor Faisal and Doctor Mohamed Abu Dina to help us in the issue.

They gave us some ideas, for example we tried to change all RFNMOS into NMOS in the schematic and run LVS without updating the netlist but also this didn't work.

So Finally just 2 days before the deadline we decided to switch back into normal NMOS and perform the LVS and PEX for the sake of completeness of the design cycle.

4.6 Layout using Ordinary Mosfet rather than rf-Mos

After Running the LVS (Layout Versus schematics) , errors were produced due to that the rf_Noms and the rf_Pmos were not well mapped between the Layout and the Netlist Produced from the schematics. We Tried to change the names in the text file but the same error remained. Then, we Decided to switch to ordinary Mosfets, we knew that time was too critical so the parasitics will be ignored till an Extracted layout is present. Also the Gard Ring and all other layers that were contouring the rf_mos will also left till we finish the complete cycle for Layout. First, as we see in (Figure 4.15) , here are the connections for the NMOs with many fingers

1) Connect all the Gates (Poly) then Contact them with a metal 1 Layer

2) Connect the Drain Subtrates Together with a metal 2 Layer

3) Connect all the Source Together with a Metal 2 Layer

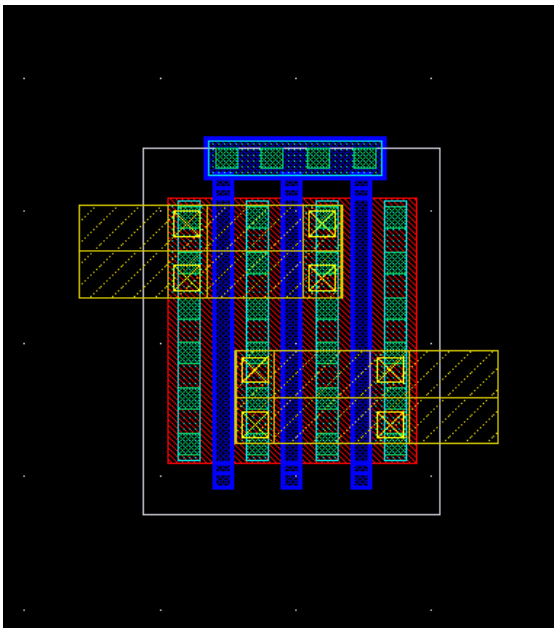


Figure 4.15 Ordinary Nmos Connections

As we can see in (Figure 4.16) , this is the final Layout for the Mixer.

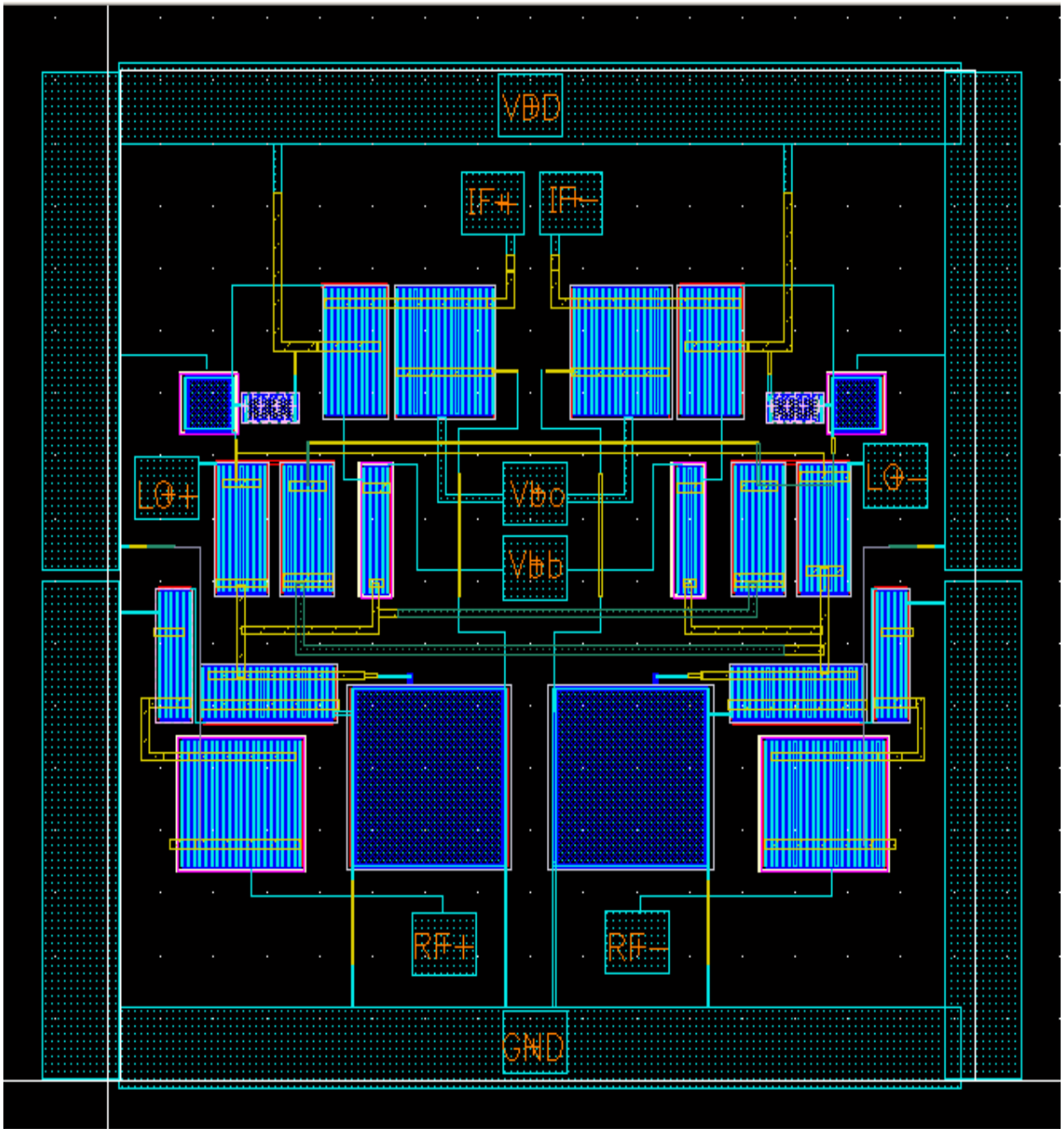


Figure 4.16 Mixer's Layout with ordinary Mosfet

After that, we have made this design DRC(Design Rule Check) free as we can see in (Figure 4.17)

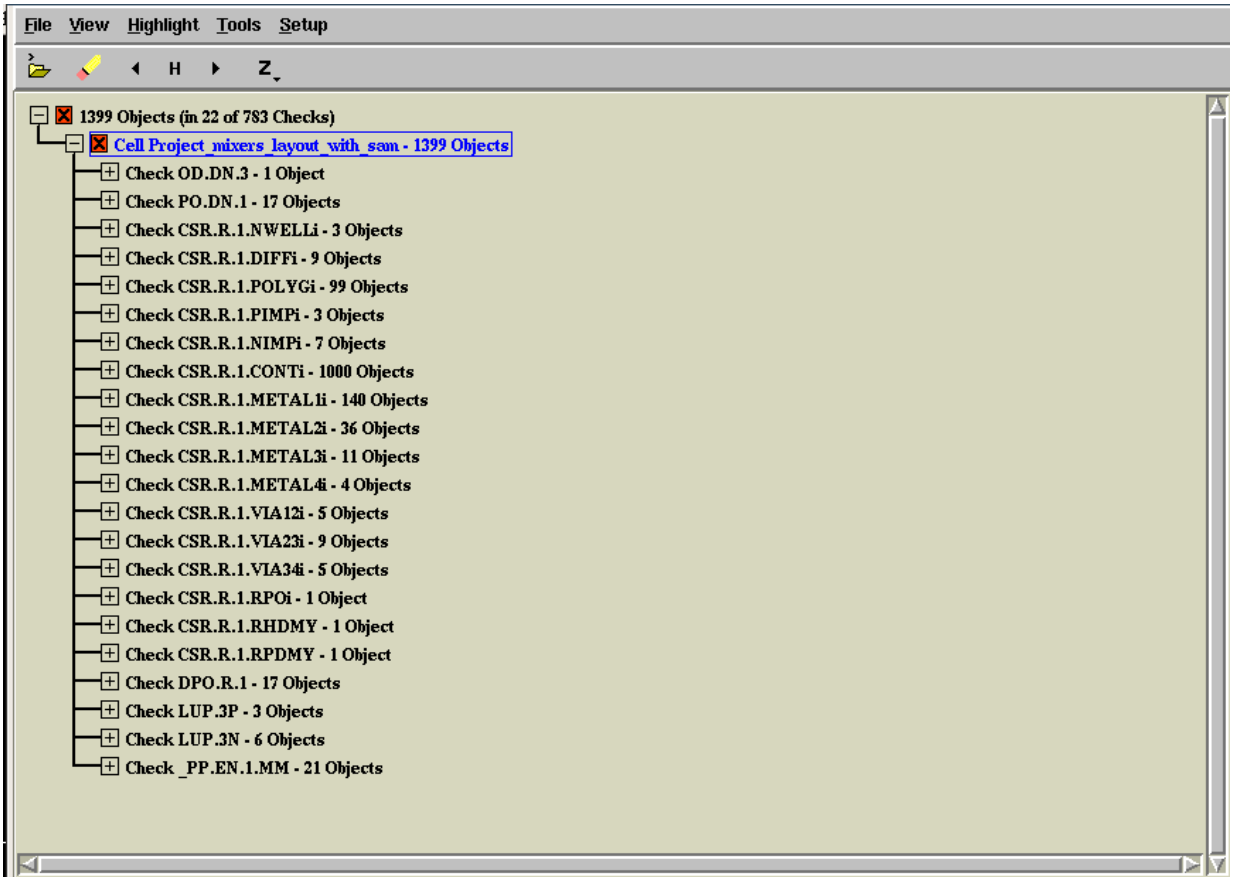


Figure 4.17 Mixer's Layout DRC Check

Note : There remaining errors like Density errors and CSR errors are neglected.

After That , we are going to make an LVS Check then Parasitic Extraction but due to the Shortage of time , any other Updates will be included in the Presentation or in a Soft-Copy which will be available with our Supervisor.

5 Conclusion

After Discussing How to Design a Wide Band Low Noise Amplifier and the main wideband Challenges, Also how to achieve a Good Mixer's Design Requirements in a Wide Band Range. Not only Circuit Design was discussed, but also how to make a well-designed layout of the proposed schematic in a way that the parasitics produced due to the layout could be minimized to the Maximum. It was a Really Nice Knowledge to know how to deal with Cadence as a simulation tool and Calibre for the Layout Process. Also, It was a nice experience to know how to deal with Research papers, How to simulate it and find out the main concepts or the main idea that makes this paper different than other ones .

Now, The Question that rises is what's Next to Do? What are the main challenges that still exist in the future of RF-Design? It's Now time to research for knowing how to make Optimizations for Our Design, try to find out the bottleneck of the Design and Try to figure out some new solutions. Try to simulate new Methods related to Noise enhancement and Power Minimization. Now, The Future of electronics is subject to Power Control, the Perfect Design is a Design that ensures Best Specifications with minimum Power Consumption. The Field of Analog and RF Design is a Sea of Knowledge that can't be absorbed in a single year , it remains the whole life and its science still remains and Open Ended Science.

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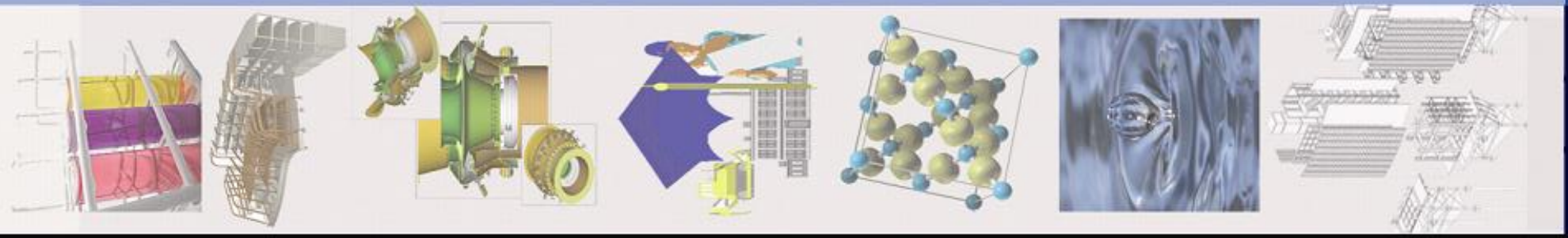
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